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Video Recording and Decoding of Test-Bed Ocean Surveillance Radar Data

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ABSTRACT

A scaled-down test-bed model of a satellite-borne ocean surveillance radar has been developed and aircraft-flight-tested. To provide a permanent record of these flight tests that would be suitable for subsequent analysis, the resulting radar data were recorded on video magnetic tape. The PRF pulse, radar video, and antenna azimuth angle were formatted and coded as necessary for recording on a single video channel. The decoding circuitry used on playback of the taped data isolates the PRF pulse and the antenna angle data. The PRF pulse is used to synchronize the timing of a digital signal processor, which provides signal-to-clutter-plus-noise enhancement, with data on the tape to provide for processing of the radar video from tape. The decoded antenna angle data are visually displayed and are converted to synchro format to provide the sweep for a PPI display. The data displayed on the PPI can be selected as unprocessed or processed radar video.

PROBLEM STATUS

This is a final report on this phase of the problem; work on other phases of the ocean surveillance radar satellite problem is continuing.

AUTHORIZATION

NRL Problem R02-46
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VIDEO RECORDING AND DECODING OF TEST-BED OCEAN SURVEILLANCE RADAR DATA

INTRODUCTION

The Aerospace Radar Branch has developed and flight-tested a test-bed ocean surveillance radar. The characteristics of this system were determined by scaling (1) based on the results of an exhaustive parametric study, using computer analysis (2), of various types of satellite-borne ocean surveillance radars. The test-bed system includes a digital signal processor (3) which operates on the radar video from the receiver to provide the enhancement of signal-to-noise-plus-clutter characteristics that is required for automatic target detection.

Some form of permanent record of the flight tests of the test-bed radar was required for subsequent analysis. To satisfy this requirement and also to provide means by which the digital signal processor could be repeatedly exercised and evaluated in the laboratory, using actual radar data, the output of the video amplifier, in the radar receiver, was recorded on video magnetic tape. The resulting video tapes then provide a library of radar data which can be repeatedly analyzed to determine various target and sea-clutter characteristics and can also be used to test future generations of digital signal processors for ocean surveillance radars.

To be able to synchronize the data on the video tape with the timing in the digital signal processor, it was necessary to also record the PRF pulse of the radar. Since the antenna of the test-bed radar was being rotated continuously to simulate the sweep of a moving satellite with respect to a point on the earth's surface, it was also desired to continuously record the antenna azimuth angle to provide the sweep information for a PPI display of the radar data from the tape.

To satisfy the video recording needs, a recording system consisting of an airborne record-only unit and a ground-based record/playback unit were purchased. At the time of purchase, the funds available were sufficient for a single video channel recording system only. Bandwidth requirements of the PRF and antenna azimuth angle data prevented their recording on auxiliary audio channels and required that they be recorded on the same channel with the radar video. In time sequence, the PRF pulse precedes the radar video, which is gated on for approximately 2 milliseconds, and the antenna azimuth data follows the radar video in serial pulse-width-modulated format.

The overall data recording system to be described here consists of two subsystems that perform two major functions. The first subsystem uses coding, formatting, and interfacing circuitry operating with the airborne recorder to accomplish data recording. The second subsystem applies interface and decoding circuitry to regain the data from the video recordings using the ground-based record/playback unit. This latter circuitry

also includes the capability of synchronizing the digital signal processor timing to the PRF timing on the tape recordings, permitting the radar video to be processed in the same manner as during flight testing. The logic circuitry used in this application is generally transistor-transistor logic (TTL) of the 54/74 type in plastic dual-in-line packages mounted on printed circuit boards.

RADAR DATA CODING, FORMATTING, AND RECORDING

(U) Figure 1 gives the overall procedure followed in preparing the various types of radar data for video recording. Each of the significant components that are illustrated will now be discussed in detail.

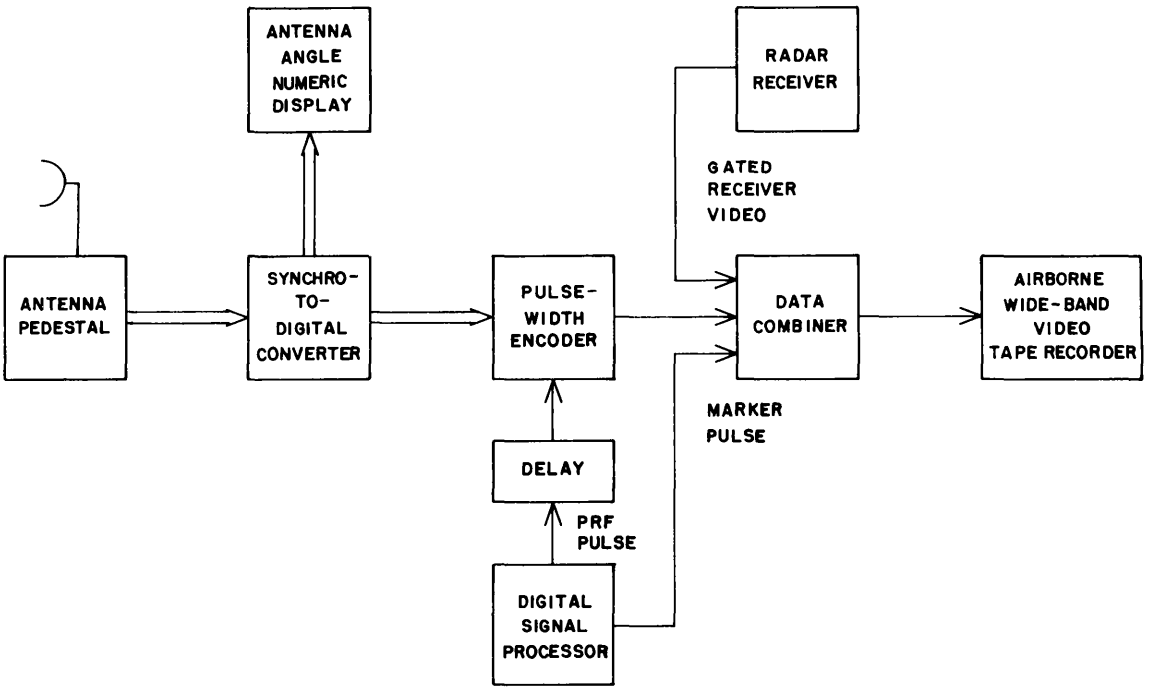


Fig. 1—(U) Radar data coding, formatting, and recording

Synchro-To-Digital Converter

(U) The antenna azimuth angle in three-wire synchro format is presented by the antenna pedestal to a synchro-to-digital converter with numeric display (Fig. 2). The synchro signal is converted within this unit to a DC voltage level in the range of ±1.800 V directly representative of ±180.0°. This DC voltage is sensed in millivolts by a digital voltmeter in the converter which presents the antenna azimuth angle in the 14-bit binary coded decimal (BCD) format shown in Fig. 3. These digital data are presented to a numeric display for visual readout of the antenna azimuth angle, to tenths of a degree.

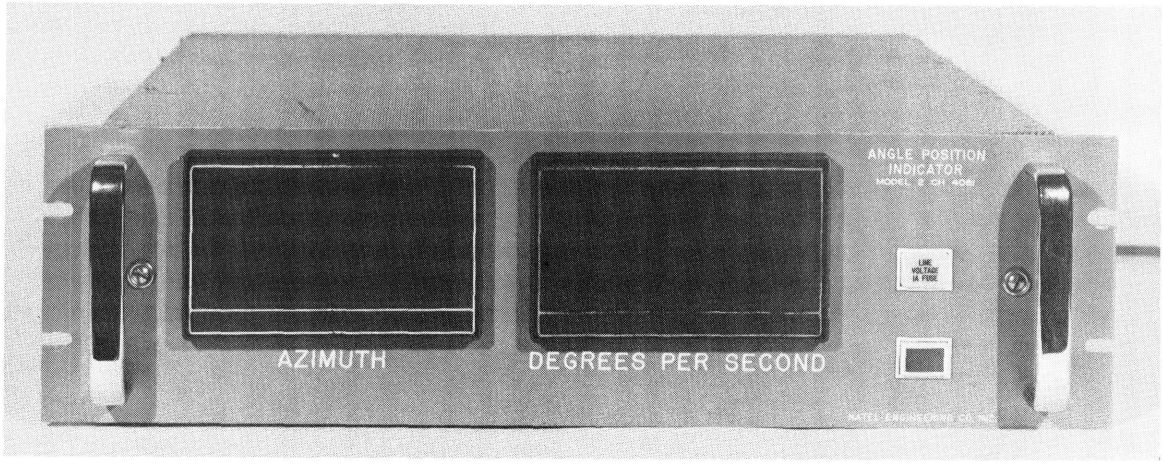


Fig. 2— Synchro-to-digital converter

Fig. 3— Digital format of synchro-to-digital converter output

	BIT	WEIGHT	
MSB	1	±	POLARITY
	2	100	HUNDREDS OF DEGREES
	3	80	TENS OF DEGREES
	4	40	
	5	20	
	6	10	
	7	8	UNITS OF DEGREES
	8	4	
	9	2	
	10	1	
	11	0.8	TENTHS OF DEGREE
	12	0.4	
	13	0.2	
LSB	14	0.1	

Pulse-Width Encoder

The output of the synchro-to-digital converter is presented to the pulse-width encoder. This unit converts the 14-bit, parallel-format, antenna azimuth data to a 14-bit, serial, pulse-width modulated signal. The detailed logic diagram* of the encoder is shown in Fig. 4. A corresponding timing diagram is shown in Fig. 5. The timing pulses are supplied to the encoder from the basic system timing circuitry in the digital signal processor in the form of a 1-μ sec-wide PRF pulse and a 100-ns-wide continuous clock pulse at a 100-kHz rate. The operation of the encoder is initiated by each PRF pulse which at its leading edge triggers a 3.5-ms one-shot† and at its trailing edge parallel-loads the 14-bit azimuth angle data into the parallel/serial register.

* It should be noted that all logic and timing diagrams in this report are intended to clarify the logical function performed and do not necessarily reflect in detail the exact operations performed in the actual implementation.

† The one-shot circuits used throughout this application are such that, with input A at a logical "0," triggering occurs on the positive-going edge of a trigger pulse at input B; with input B at a logical "1," triggering occurs on the negative-going edge of a pulse at input A. The true or positive-going output of the one-shot is available at Q while its complement is available at $\overline{Q}$.

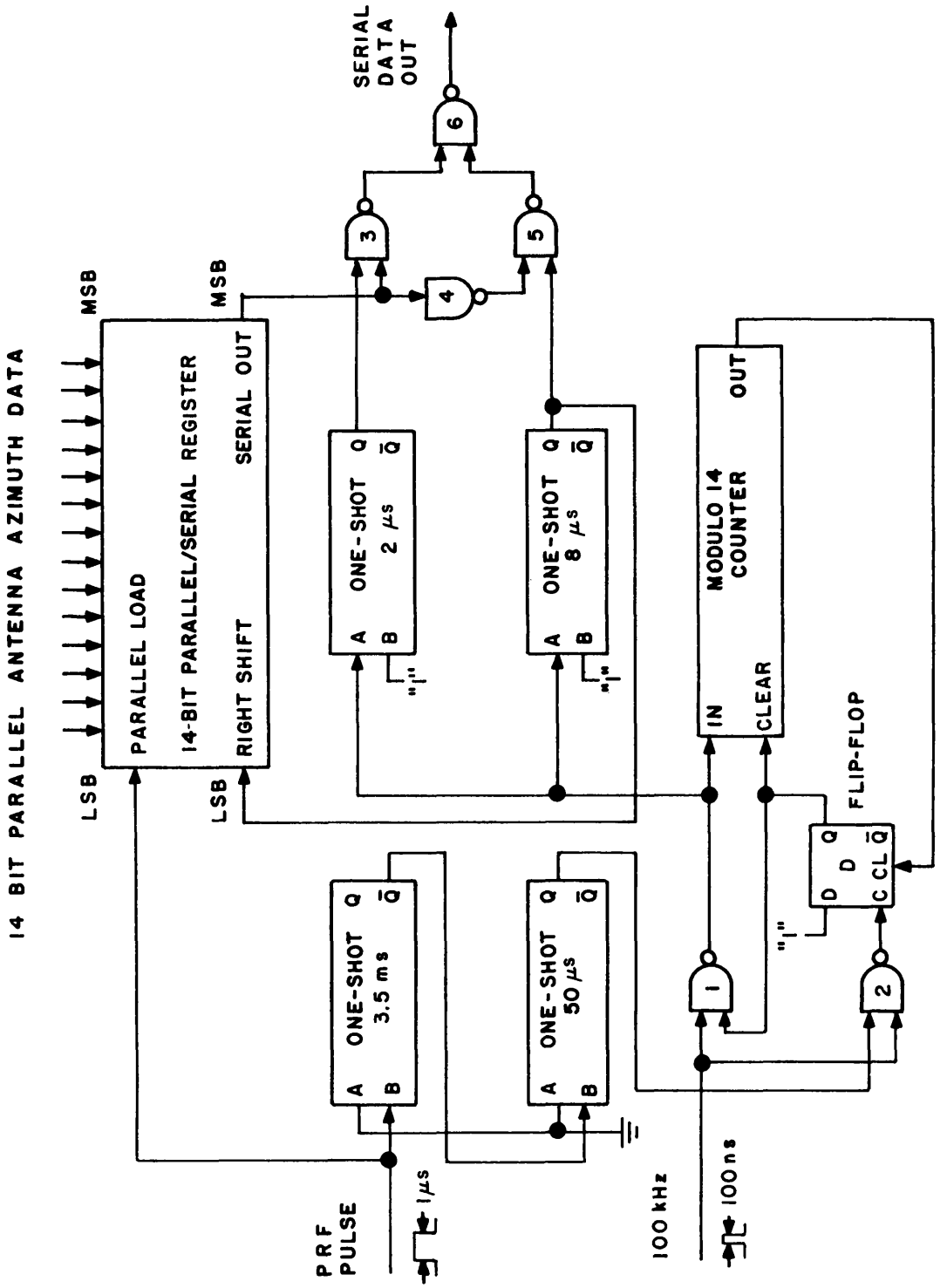


Fig. 4— Pulse-width encoder

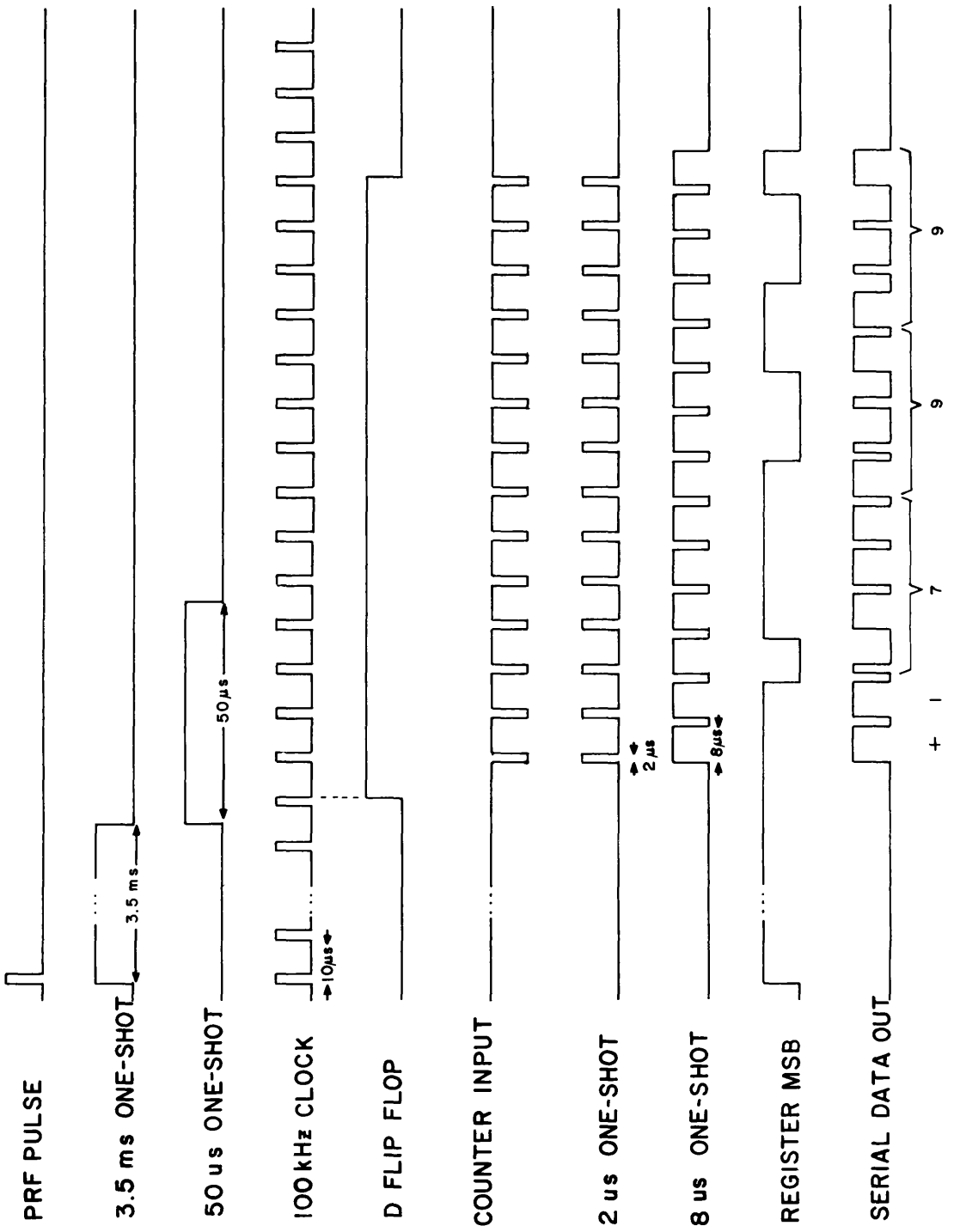


Fig. 5— Pulse-width encoder timing diagram

The purpose of the 3.5-ms one-shot is to delay the generation of the serial azimuth angle code until some time sufficiently beyond the end of the gated radar video. The trailing edge of the 3.5-ms one-shot triggers a 50-μs one-shot. The 50-μs output pulse width was established to overlap several periods of the 100-kHz clock and to permit the modulo 14 counter to count over exactly 14 clock intervals as will be described. The Q output from the 50-μs one-shot gates the 100-kHz clock through NAND gate 2 to the clock (C) input of the D flip-flop.* Since the clock pulses are inverted, the D flip-flop, which was reset at the completion of the previous encode cycle, is thus triggered to the logical "1" state at a point in time corresponding to the first trailing edge of the 100-kHz clock to occur during the 50-μs one-shot pulse. The Q output of the D flip-flop goes to a logical "1," gates the 100-kHz clock to the counter input through NAND gate 1, and enables the modulo 14 counter by taking a logical "0" off its clear input. Since these clock pulses are inverted, the counter, which counts on the positive-going edge of input pulses, commences counting at the trailing edge of the first 100-kHz clock pulse to occur after the D flip-flop output Q goes to a logical "1." The counter proceeds to count the next 14 inverted 100-kHz clock pulses. After the 14th count, at the trailing edge of a 100-kHz clock pulse, the D flip-flop is cleared, disabling the counter and NAND gate 1.

The 14 clock pulses, which are gated through NAND gate 1 to the counter, each trigger both a 2-μs and an 8-μs one-shot on their leading or negative going edges. The output of the most significant bit (MSB), or the serial output of the register which contains the azimuth angle data loaded in at the PRF pulse, is gated with each of the Q outputs of these one-shots in NAND gates 3, 4, 5, and 6 in such a manner that either a 2-μs or an 8-μs pulse appears at the serial data output, depending on whether the bit in the MSB position is a logical "0" or logical "1" respectively. At the trailing edge of the Q output of the 8-μs one-shot, by which time either a 2-μs or an 8-μs data pulse has already been generated, the parallel/serial register is shifted right one position, which shifts the next MSB to the MSB position or serial output. This then permits a pulse-width-modulated data pulse to be generated, for the next MSB, at the next gated clock pulse. This continues for each of the clock pulses until after 14 pulses the azimuth angle data have been converted to serial pulse-width-modulated format. This entire operation is shown in Fig. 5 for the azimuth angle +179.9°.

Data Combiner

To aid in the decoding of the radar data during playback of the video tape, specifically in the detection of the PRF pulse, a 1-μs-wide marker pulse was generated 10 μs prior to the PRF pulse. This was accomplished in the data combiner, shown in Fig. 6, by gating of the required counter states from the system timing circuitry in the signal processor. The inverted marker pulse, PRF pulse, and pulse-width-modulated antenna azimuth data are NAND gated together and amplified by a line driver. These digital data are then combined with the gated radar video in a resistive amplitude mixer. By means of the indicated potentiometers in Fig. 6, the signal levels are individually adjusted

* The D flip-flop as used here is clocked to the logic state present at its D input by the positive-going edge of a pulse at input C. It is reset to its logical "0" state by applying a logical "0" at input CL and is preset to a logical "1" state by a logical "0" at input $\overline{P}$. The true state of the flip-flop is available at output Q with the complement available at output $\overline{Q}$.

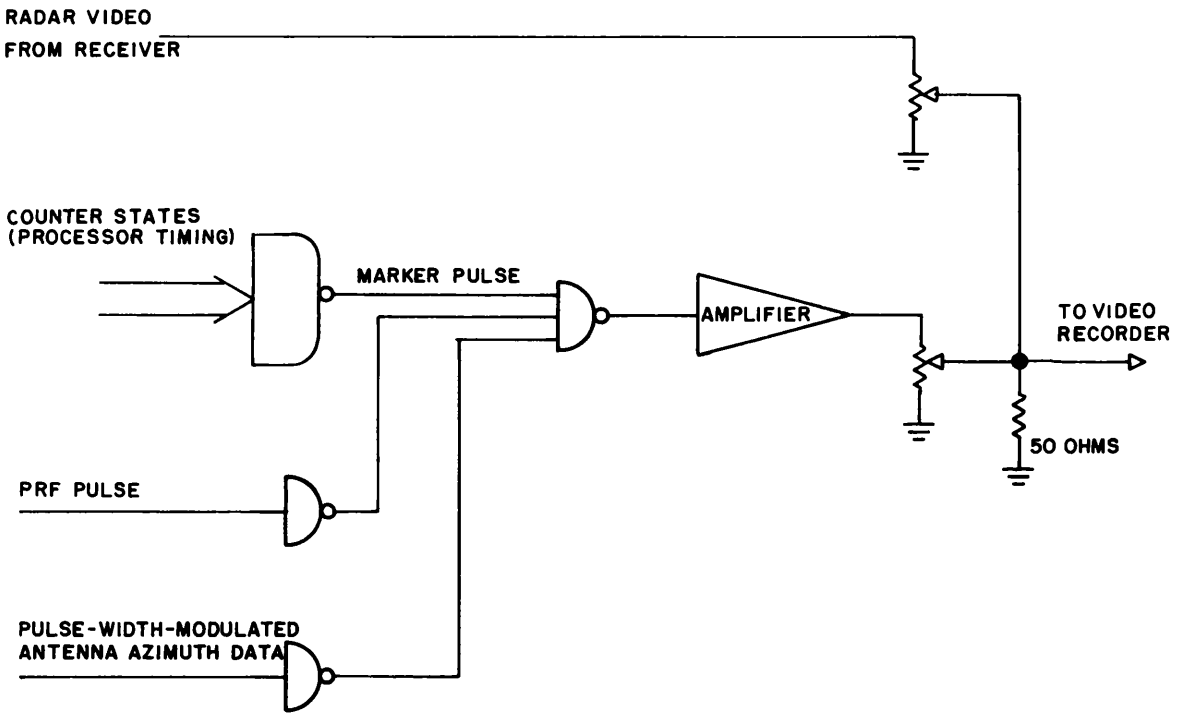


Fig. 6- Date combiner

so that the logical "1" level of the digital data as well as the peak of the radar video are at +5.0 V. The format of these data which are presented to the airborne video recorder is shown in Fig. 7.

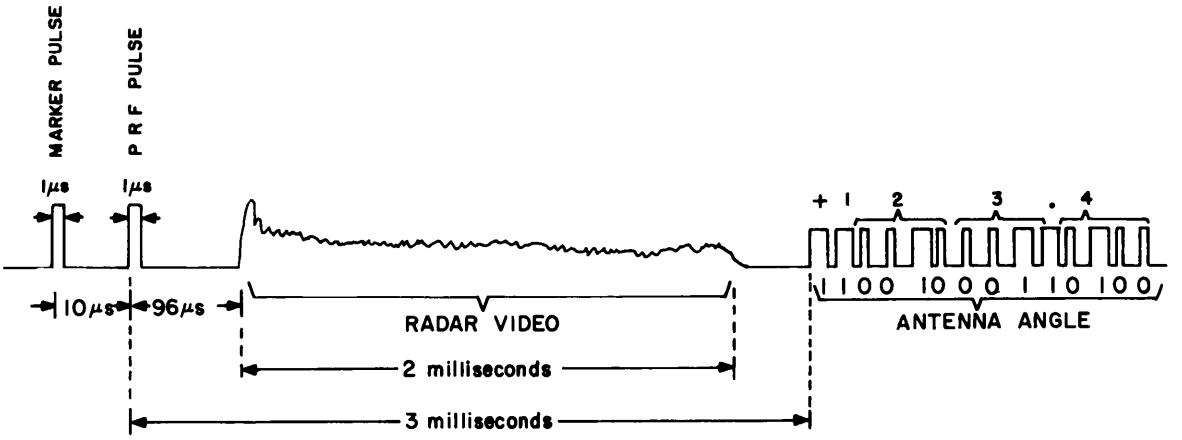


Fig. 7 Format of data recorded on video tape

Airborne Video Recorder

The airborne video recorder, AMPEX model AR-500A, shown in Fig. 8 is used to record the radar data. The recorder consists of a transport assembly (with shock mounts), an auxiliary assembly to provide required vacuum and cooling, and a control unit. The overall recorder weighs 78.5 pounds, requires 400 Hz and 28 V DC power, and is capable of up to 40 minutes of record time. It has a rotary record head assembly and provides one signal data channel with a 3-dB frequency response of 1 Hz to 6.0 MHz referenced to 1 MHz with 1 V peak-to-peak (p-p) normal input and output record levels. The p-p signal-to-rms noise ratio is 40 dB referenced to a 1 V p-p signal, and the time-base stability is ±25 ns p-p with respect to the system timing reference for an entire continuous recording.

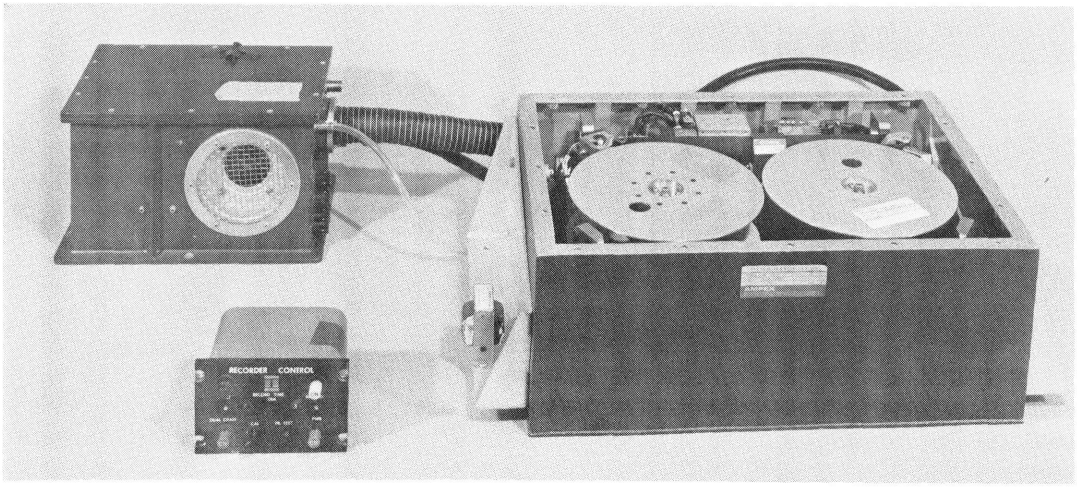


Fig. 8 Airborne Video recorder

The recorder also has two auxiliary channels of 1 V rms normal input and output levels each with a 3-dB frequency response of 300 Hz to 30 kHz referenced to 1 kHz. The signal-to-rms noise on these auxiliary channels is 30 dB. One of these channels was used extensively during flight tests for an audio record of the radar operators' observations.

VIDEO PLAYBACK AND DIGITAL DECODING

Figure 9 gives the steps performed in the playback and decoding of radar data stored on video tape, as previously described. The wide-band playback unit (Fig. 10) is an AMPEX 900 A-1 recorder/reproducer. This unit weighs 809 pounds, operates on AC power of nominally 115 V, 60 Hertz, has a rotating head assembly, and possesses signal and auxiliary channel characteristics identical to the AR-500A machine described earlier.

The output of the video playback unit is presented to two amplifiers with DC level control. These amplifiers restore the radar data voltage levels, which were limited to 1 V p-p at the recorder video channel input and output terminals, to their normal 5-V levels. One amplifier provides radar data from the tape to the decoding circuitry while

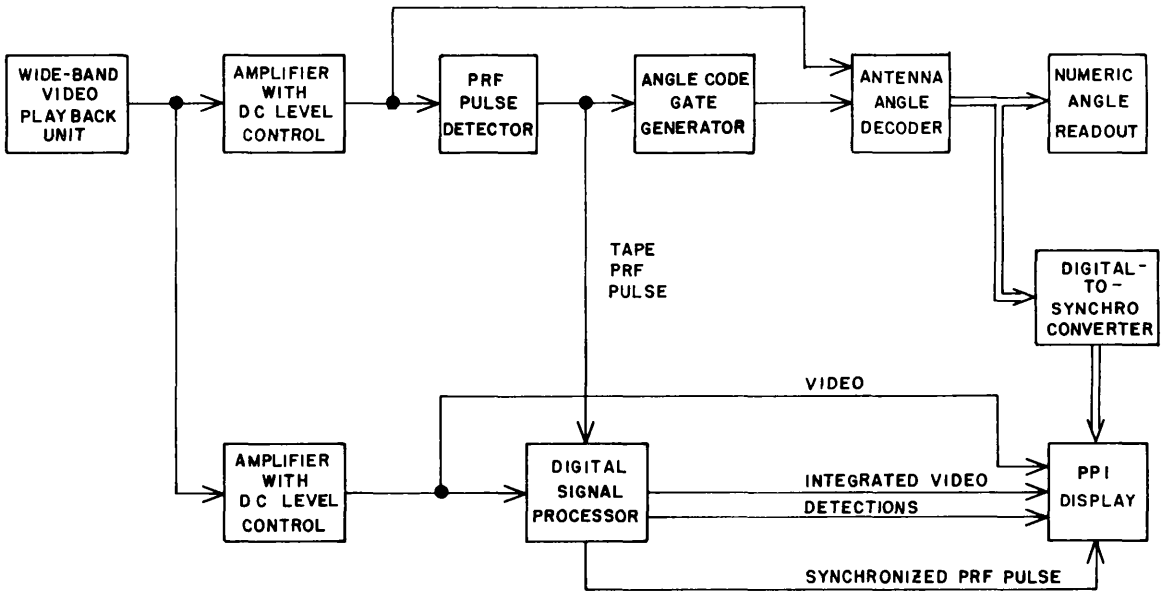


Fig. 9 Video playback and digital decoding

The second amplifier provides data for processing by the digital signal processor and for PPI display. Each of these applications of the radar data can be optimized by the DC level controls on these amplifiers.

PRF Pulse Detector

The radar data to be decoded during each PRF interval contain a marker pulse, the PRF pulse, radar video, and antenna azimuth angle data in the format described earlier and shown in Fig. 7. From these composite data it is required to detect the PRF pulse and to isolate and decode the antenna angle information. The detection of the PRF pulse permits synchronization of the digital signal processor timing with the radar video portion of the data on the tape to permit radar signal processing. The decoded antenna angle data are displayed numerically and are used to derive synchro sweep data for a PPI display.

The PRF pulse, in the radar data from the tape, is of 1-μs duration and occurs 10 μs after a marker pulse of 1-μs duration. This marker pulse aids in the recognition of the PRF pulse which is accomplished as shown in the logic diagram in Fig. 11. The associated timing diagram is shown in Fig. 12. The data from the tape are presented to NAND gate 1 which is enabled by the $\overline{Q}$ output of the 4-ms one-shot initially at a logical "1." The output of NAND gate 1 is inverted by NAND gate 2 and presented to the input of the pulse-width detector* (4). If a pulse of width 1 μs ±100 ns is presented at its input, the pulse-width detector generates a negative-going detection pulse of 100-ns duration

*U.S. Patent Application filed October 26, 1971, Lawrence M. Leibowitz, Navy Case Number 53182.

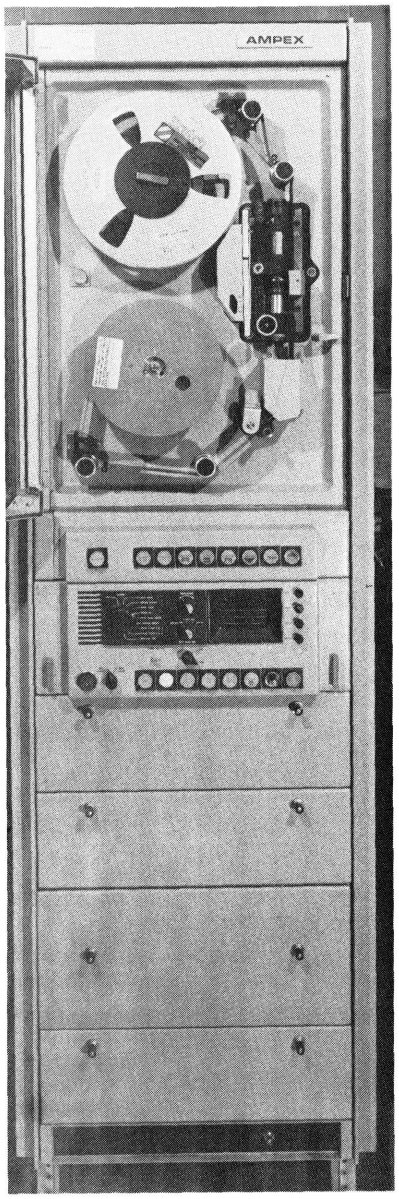
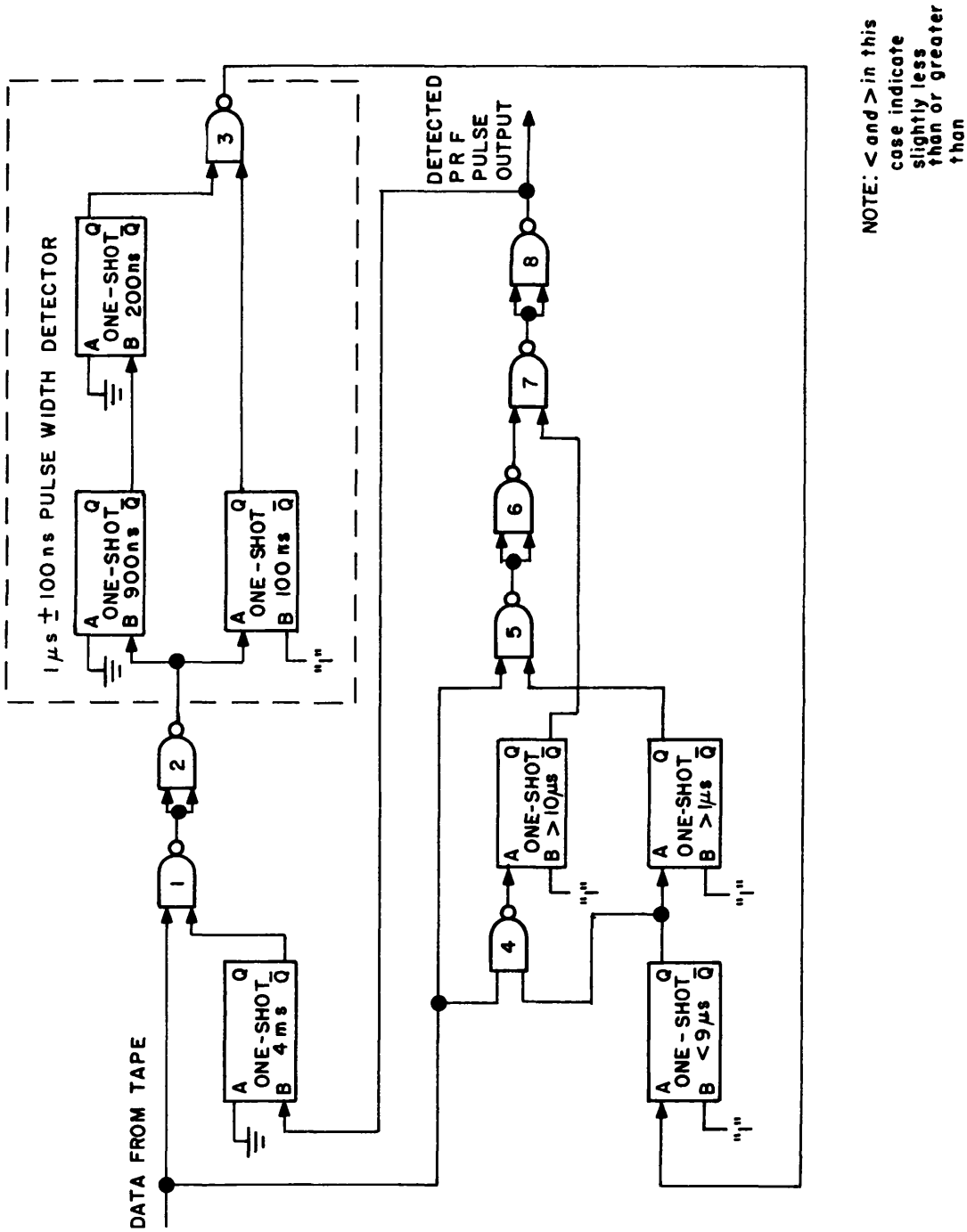


Fig. 10 Video playback unit

whose leading edge is coincident with the trailing edge of the detected pulse. The detection pulse is presented to the A input of a one-shot which generates a pulse of slightly less than 9-μs duration whose leading edge is coincident with the trailing edge of the detected pulse. The trailing edge of this slightly-less-than 9-μs pulse triggers a one-shot which generates a positive-going pulse of slightly-more-than 1-μs duration at its Q input. This Q output enables NAND gate 5 which gates the data from the tape. If it is assumed that the marker pulse was the 1-μs-wide pulse detected by the pulse-width detector, the Q output of the $>$1-μs one-shot forms a window pulse which gates the PRF pulse through NAND gate 5. The output of NAND gate 5 is inverted by NAND gate 6 and presented to NAND gate 7.



NOTE: < and > in this case indicate slightly less than or greater than

Fig. 11 PRF—pulse detector

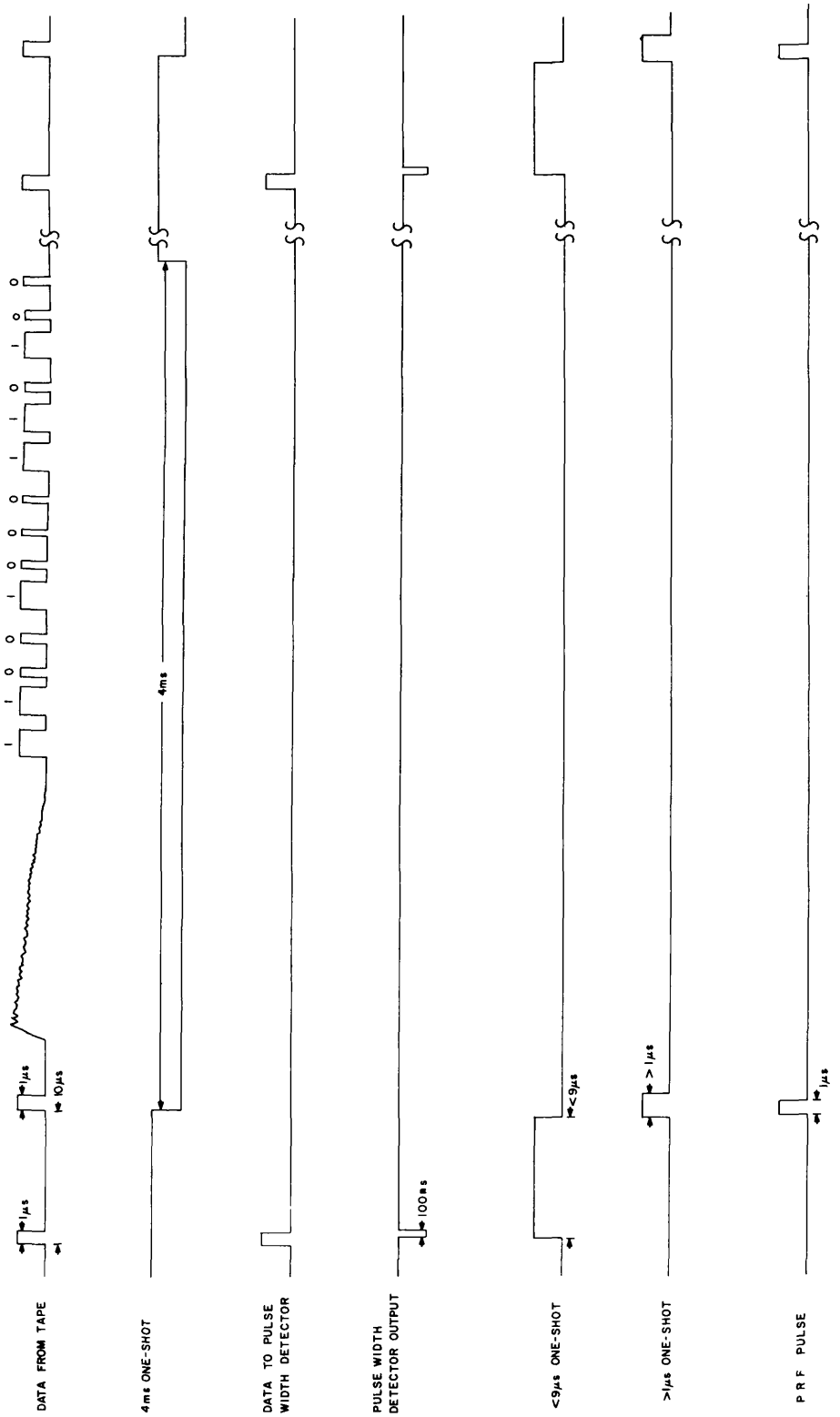


Fig. 12 PRF—pulse detector timing diagram

It should be noted that the recorder can be turned on at such a time that the PRF pulse detector begins its interrogation during a radar video portion of the tape data. Since the radar video contains broad bandwidth data including signal, clutter, and noise, more than likely the pulse width detector will emit a detection pulse resulting in the generation of the >1-μs window pulse enabling NAND gate 5. If any pulse, including that due to any part of the radar video, occurs in the data between the trailing edge of the marker pulse and the leading edge of the PRF pulse, or equivalently during the positive pulse at the Q output of the <9-μs one-shot, it is gated through NAND gate 4 and triggers a one-shot that generates a negative-going pulse of slightly-greater-than 10-μs duration at its $\overline{Q}$ output. This pulse disables NAND gate 7. If no noise pulse occurs between the marker and PRF pulses, NAND gate 7 is enabled and the PRF pulse is gated to NAND gate 8 and the output. Thus, to be generated, a PRF pulse must be preceded by a 1-μs marker pulse followed by 9 μs of dead time.

The leading edge of a detected PRF pulse triggers the 4-ms one-shot which disables input NAND gate 1. For any given PRF pulse, 4 ms exceed the total time extent of the radar video and antenna azimuth data. Thus, following the detection of a PRF pulse, the PRF pulse detector is disabled until a time sufficiently beyond the radar data, for the particular PRF interval, but well before the next PRF pulse. Thus, the PRF pulse detector operation will be automatically resynchronized to the data from the tape.

Angle Code Gating Pulse Generator

The antenna azimuth angle data appear on the tape as a serial pulse-width-modulated binary code. The first bit in this code is displaced in time by more than 3.5 ms beyond the leading edge of the PRF pulse. Since the total extent of the radar data for a given PRF is less than 4 ms, the antenna angle code will, upon playback, be located in time between 3.5 and 4 ms after the leading edge of the PRF pulse.

The angle code gate generator circuitry produces a gating pulse which locates the angle code data in time and gates it to the antenna angle decoder. The logic and timing diagrams of this circuitry are shown in Fig. 13. At the leading edge of the PRF pulse detected from the video tape, the 4-ms and 3.5-ms one-shots are triggered. The positive-going pulse from the Q output of the 4-ms one-shot and the negative-going pulse from the $\overline{Q}$ output of the 3.5-ms one-shot are combined by NAND gate 1 and inverted by NAND gate 2. The output of the circuit is a positive-going pulse which extends from 3.5 ms to 4.0 ms after the leading edge of the PRF pulse and overlaps the time extent of the antenna angle code.

Antenna Angle Decoder

The angle code gating pulse enables the antenna angle decoder as shown in the logic diagram of Fig. 14. The timing diagram associated with this circuitry is shown in Fig. 15. By means of NAND gates 1 and 2, the angle code gating pulse isolates the serial angle code from the tape data. The serial angle code is presented to the serial input of the 14-bit parallel/serial register as well as the B input of a 5-μs one-shot. The one-shot is thus triggered on the leading-edges of the 2-μs and 8-μs pulses which comprise the logical values "0" and "1", respectively, of the serial angle code. The register accepts an input bit

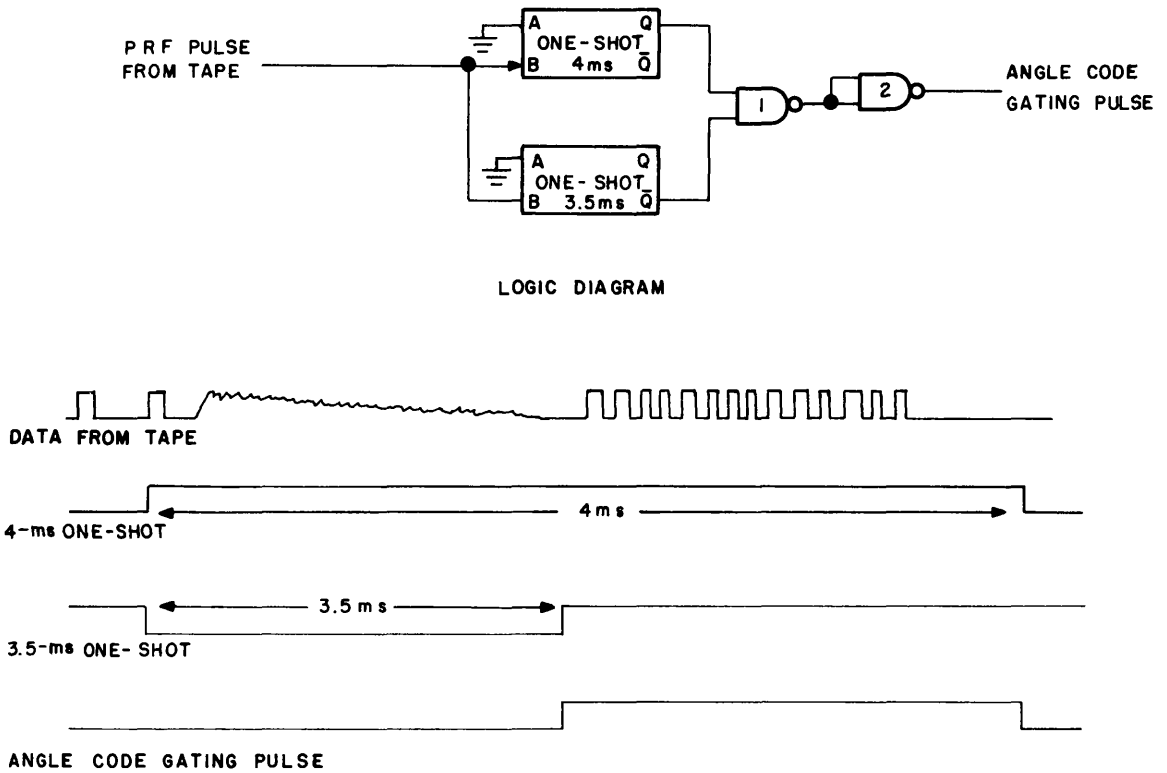


Fig. 13—(U) Angle code gating pulse generator

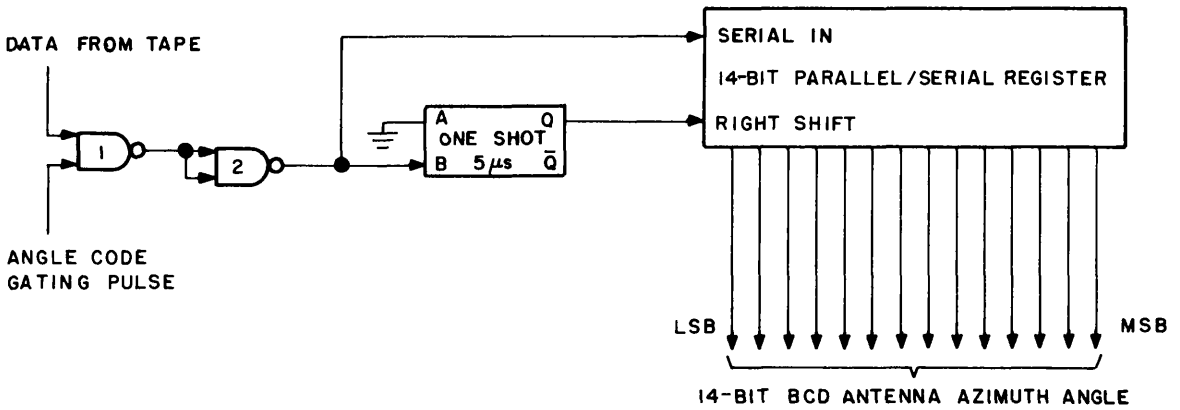


Fig. 14 Antenna angle decoder

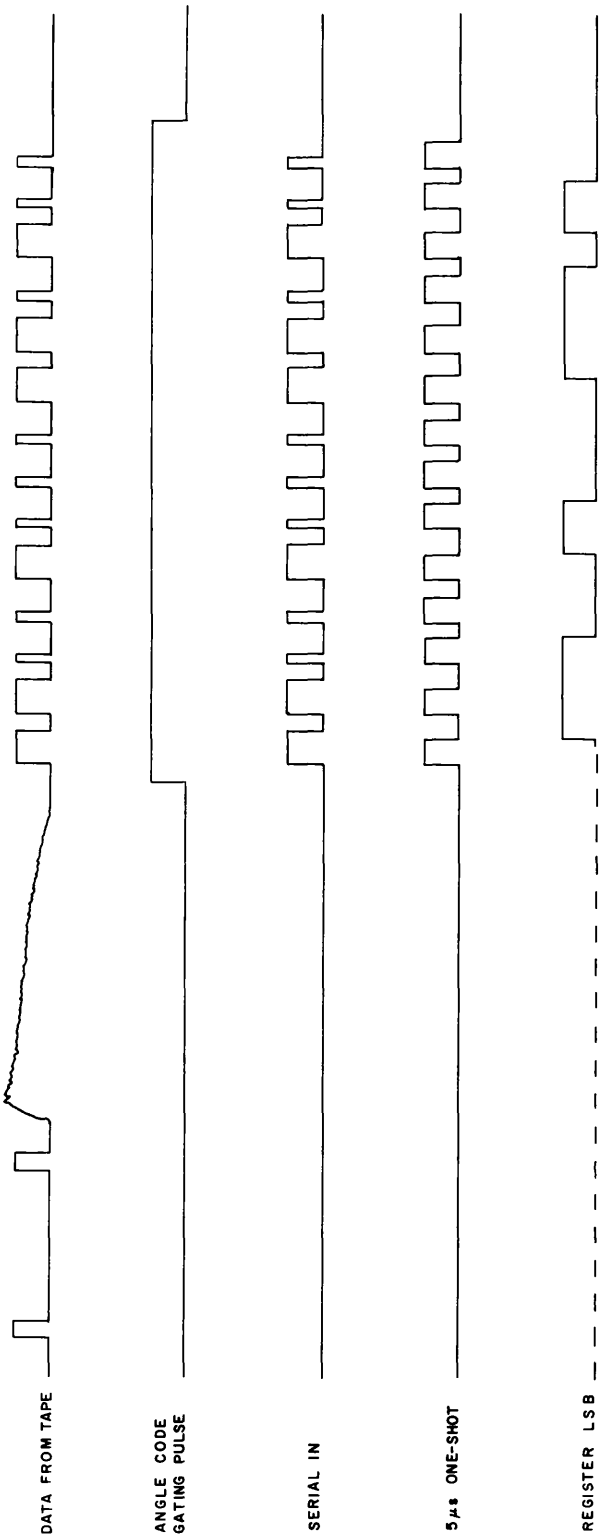


Fig. 15 Antenna angle decoder timing diagram

and shifts all its data to the right one-bit position at the negative going or trailing edge of a pulse at its right shift input. Thus, any given pulse from the serial angle code generates a 5-μs shift pulse which at its trailing edge shifts the data then present at the serial-in terminal into the LSB position of the register. If the bit is a logical "0" or 2-μs pulse, it will no longer be present when the right shift occurs and a logical "0" will be shifted into the register LSB. If the bit is a logical "1" or 8-μs pulse, it will still be present at the occurrence of the right shift; thus, a logical "1" will be shifted into the shift register LSB. It should be noted that the advantage of the pulse-width-modulated code is that knowledge of the exact position in time of each bit is not required for decoding because the code is self-synchronous, providing its own decode timing at the leading edge of each bit.

The 14-bit parallel BCD results of the antenna angle decoding are presented to a numeric angle readout for visual display to tenths of a degree on numeric indicator tubes. The data are also presented to the digital-to-synchro converter shown in Fig. 16. The converter translates the binary representation of the angle code to a three-wire, 60-Hz, 90-V synchro signal. This synchro signal supplies the sweep data to a PPI display.

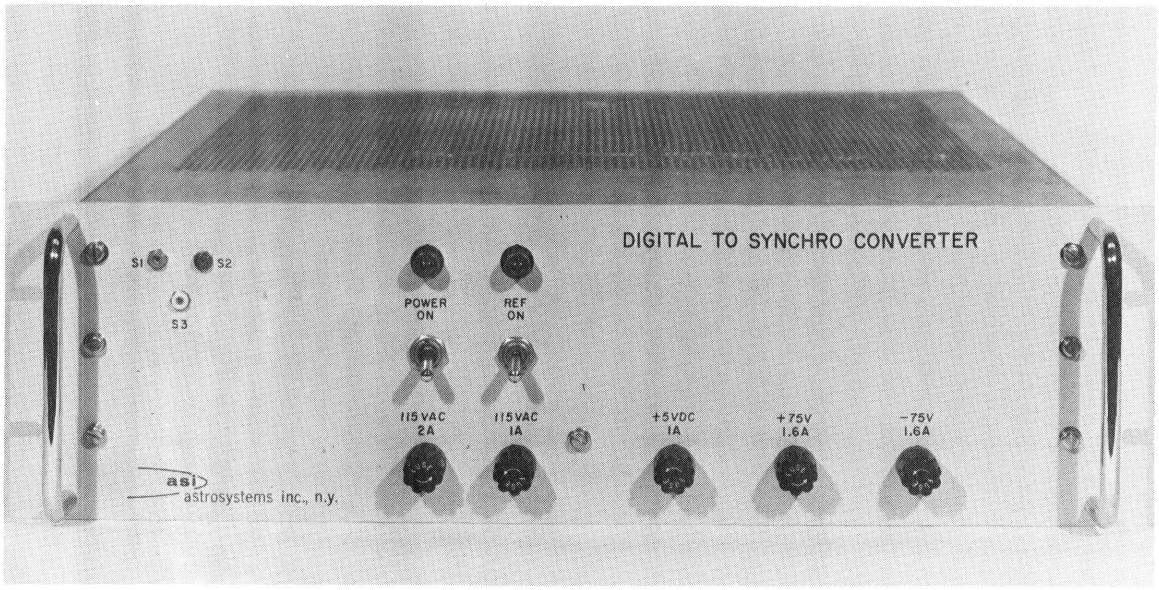


Fig. 16 Digital-to-synchro converter

Signal Processor Timing Synchronizer

The radar data from the tape, after suitable amplifying and DC level adjustment, are presented to the digital signal processor. To permit processing in the same manner as during the actual flight tests, when the radar data were recorded, the processor timing must be synchronized with the timing of the data on the tape. The logic circuitry used to accomplish this synchronism is shown in Fig. 17. The timing diagram associated with the synchronizer is shown in Fig. 18.

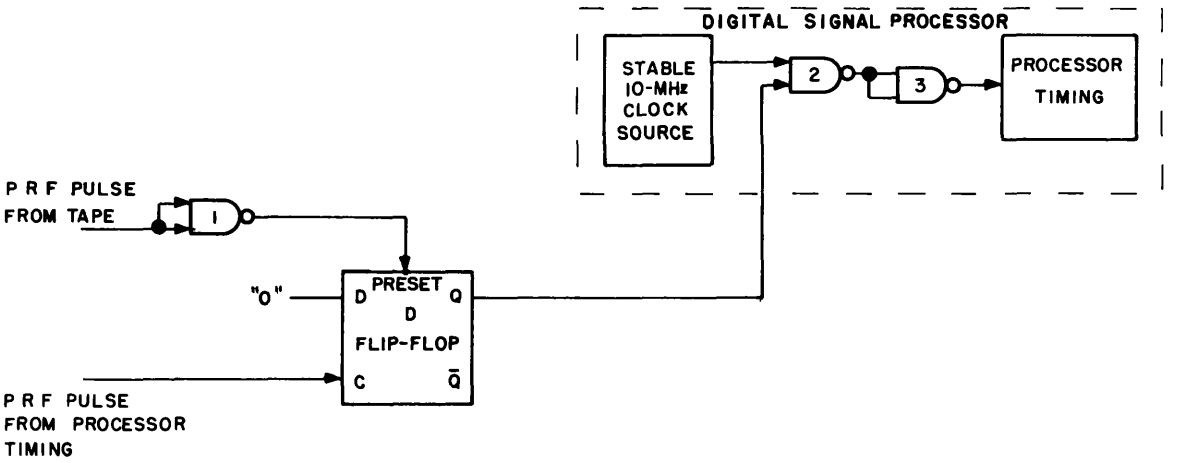


Fig. 17 Signal processor timing synchronizer logic diagram

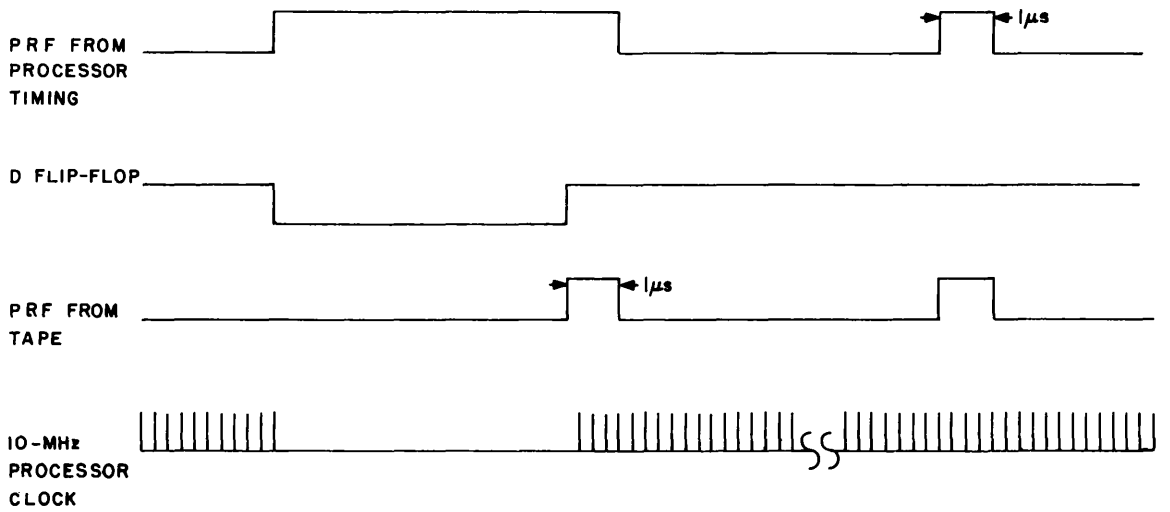


Fig. 18 Signal processor timing synchronizer timing diagram

To describe the operation of this circuitry, the processor timing is assumed to be out of synchronism with the data on the tape. One of two conditions are then possible. First, the *D* flip-flop is in a logical "1" state and the processor timing is enabled; second, the *D* flip-flop is reset and the processor timing is disabled. Under the first condition, the processor timing counts until the generation of a PRF pulse. The leading edge of this PRF pulse sets the *D* flip-flop to its logical "0" state. This inhibits NAND gate 2, preventing 10-MHz clock pulses from reaching the processor timing circuitry. All processor timing is now inhibited, and the PRF pulse from the processor remains high at its logical "1" state. When the PRF pulse from the tape occurs, it is inverted by NAND gate 1 and presets the *D* flip-flop to its logical "1" state, enabling NAND gate 2 and the processor timing. The processor timing then proceeds to count off the 1-μs processor PRF pulse duration. The trailing edge of this PRF pulse occurs in coincidence with that of the PRF pulse from tape. Processor timing is then in synchronism with the PRF timing on the tape until

another asynchronous condition occurs at which time another correction will automatically occur. Under the second condition, the PRF pulse from the tape presets the *D* flip-flop to a logical "1," creating the first condition, and the operation proceeds as described above.

With the signal processor timing synchronized to the timing on the tapes, the radar video data can be processed for enhancement of signal-to-noise-plus-clutter characteristics. The same data can be repeatedly processed under varying conditions, such as feedback factor, range, and detection threshold. The synchronized PRF pulse from the processor supplies the trigger pulse to a PPI display which receives its sweep data from the video tape as described earlier. The intensity-modulated data to the PPI display can be unprocessed video from the tape or processed video before or after detection thresholding as selected.

CIRCUIT IMPLEMENTATION

All the logic circuitry used in this application is TTL integrated circuitry in plastic dual-in-line packages. The packages are mounted on printed circuit boards with twelve packages per board. Three boards (Fig. 19) were required to implement the logic circuitry described here and are mounted in one of the digital signal processor chassis. It should be noted that circuitry was saved in the actual implementation, as compared to the logic diagrams described here, since common circuitry can be used in the encoding and decoding of the radar data. As an example the same 14-bit parallel/serial register circuitry is used for both encoding and decoding antenna angle data.

SUMMARY

The video recording and decoding system described here has proven to be a vital tool in the analysis of ocean-surveillance data gathered as a result of airborne tests. It has provided a substantial library of video tapes of radar data which can be repeatedly analyzed and used to test and evaluate, in the laboratory, present and future signal processors for ocean surveillance radars. This greatly reduces the amount of time required for costly airborne testing.

By using these tapes, the various parameters of the signal processor can be varied and circuits modified to determine optimum conditions for processing various types of radar data, such as at near and far range and for different size ship targets. Unprocessed radar data samples for particular range bins from the tape recordings have been digitized and stored on punched-paper-tape. By using these paper tapes with the CDC 3800 computer at NRL, analyses of the radar data have been performed, resulting in determination of autocorrelation coefficients, discrete Fourier transforms, and signal processor signal-to-noise-plus-clutter improvement factors. The detailed results of these analyses are documented (5).

The satellite-borne ocean surveillance radar research program requires the development of ship detection algorithms for the determination of ship targets from processed radar detection data as well as the investigation of land-mass-blanking techniques. The video-taped radar data with the playback system described here provide an extremely useful

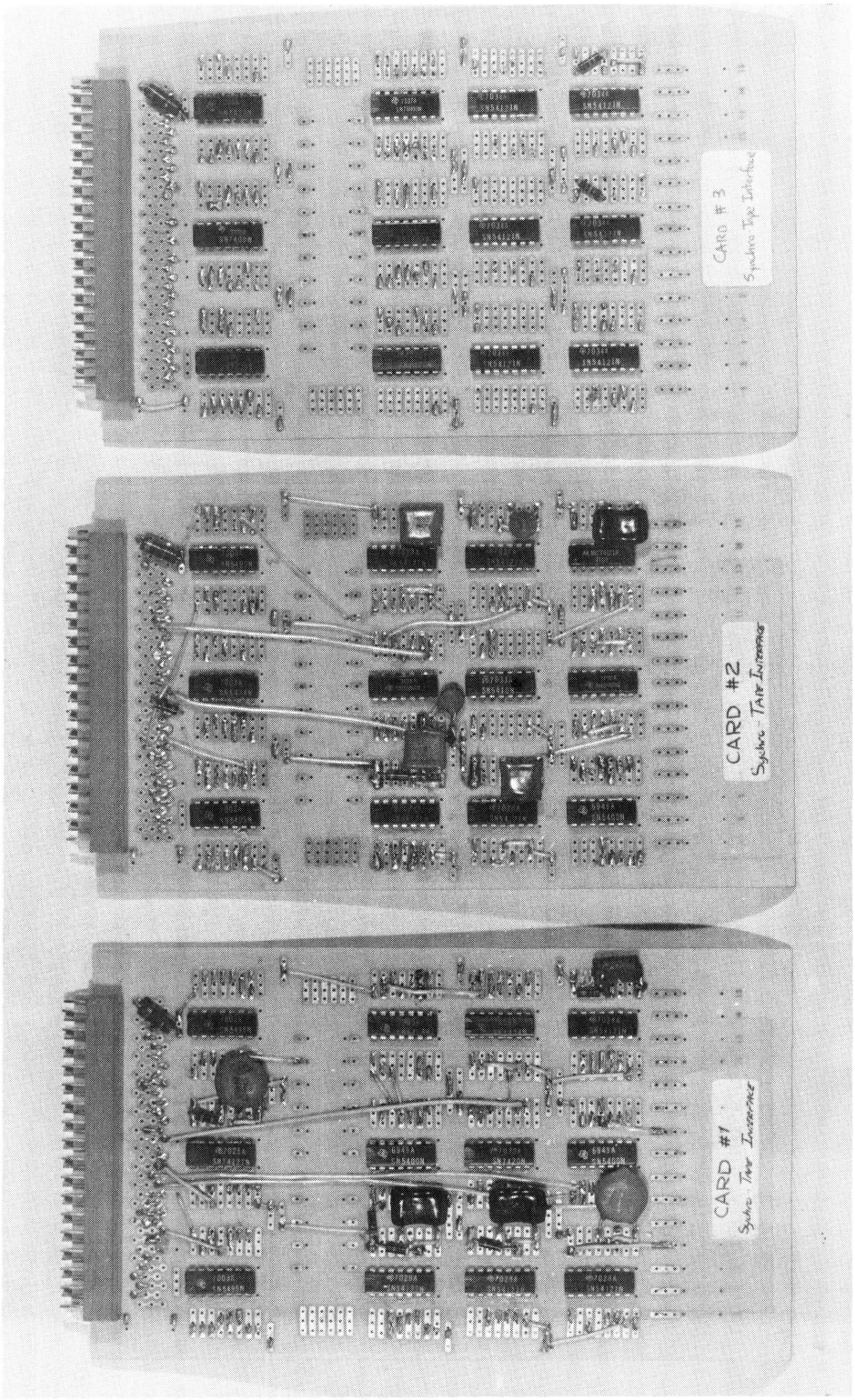


Fig. 19 Radar data recording and decoding circuitry

means of experimenting repeatedly with many types of ship detection and land-mass-blanking software and hardware algorithms on various known targets under various conditions to determine the optimum algorithms to be used.

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13. ABSTRACT

A scaled-down test-bed model of a satellite-borne ocean surveillance radar has been developed and aircraft-flight-tested. To provide a permanent record of these flight tests that would be suitable for subsequent analysis, the resulting radar data were recorded on video magnetic tape. The PRF pulse, radar video, and antenna azimuth angle were formatted and coded as necessary for recording on a single video channel. The decoding circuitry used on playback of the taped data isolates the PRF pulse and the antenna angle data. The PRF pulse is used to synchronize the timing of a digital signal processor, which provides signal-to-clutter-plus-noise enhancement, with data on the tape to provide for processing of the radar video from tape. The decoded antenna angle data are visually displayed and are converted to synchro format to provide the sweep for a PPI display. The data displayed on the PPI can be selected as unprocessed or processed radar video.

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Video recorder						
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Pulse-width detector						
Antenna azimuth data						
TTL logic circuitry						