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Performance and Analysis of Sonar Transmitter Using Parallel Inverter Unit

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ABSTRACT

A solid-state sonar transmitter using silicon-controlled rectifiers in a parallel inverter circuit has been developed. The transmitter has an output power of three kilowatts, with an efficiency of 85 to 90 percent at low audio frequencies. An ac equivalent circuit for the parallel inverter and load combination has been analyzed to obtain equations for inverter input resistance, commutation ratio, and peak voltage. The equivalent circuit assumes that the inverter components are lossless and that the input current is constant.

The transmitter was used to drive a 36-element array of variable-reluctance transducers which have a resonant frequency of 960 cycles per second. The distorted driving voltage from the inverter circuit did not adversely affect the acoustic performance of the projector array. Comparison of the measured and calculated performance of the inverter circuit indicates that the ac model gives sufficiently accurate results to allow prediction of inverter performance with a known load.

PROBLEM STATUS

This is an interim report on this project; work is continuing on this and other phases.

AUTHORIZATION

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PERFORMANCE AND ANALYSIS OF SONAR TRANSMITTER USING PARALLEL INVERTER UNIT

INTRODUCTION

Inverters using silicon-controlled rectifiers (SCR's) are now being widely used for dc-to-ac power conversion because they are capable of efficient operation at high power levels and require a relatively small number of circuit components. An SCR inverter unit can best be used as a sonar transmitter where the prime requirements of the transmitter are high efficiency, high output power, and reliable operation. Presently, SCR's are available with current ratings up to 200 amperes and voltage ratings to 800 volts. With these SCR's inverter units can be built with output power up to 50 kilowatts and conversion efficiencies of 90 percent with operation up to frequencies of several kilocycles. At frequencies above several kilocycles, SCR switching losses become significant, causing the output-power capability of inverter units to decrease with increasing frequency. The turn-off time of the SCR determines an upper frequency limit of operation which, for high-power inverter units, is between 10 and 20 kilocycles. Reliability of SCR inverters is due in part to the small number of components involved in the circuit. Also, the switching mode of operation does not lead to instability, which often occurs in high-gain linear amplifiers.

The critical point in the operation of inverters using controlled rectifiers is the stopping of current flow through the controlled rectifier; this is done by application of a negative voltage on the anode for a certain duration of time, called the commutation time. There is a class of inverters which delivers power to a load having established voltages; this class of inverters is not of interest in this discussion, however. Of interest here is the class of inverters, called self-excited, which can deliver ac power to a passive load such as a sonar projector. These inverters contain at least one inductive and one capacitive element, which together provide the negative voltage across the controlled rectifier necessary for the stopping of current flow. There are two basic types of inverters, the series and the parallel. In the series inverter the inductance and capacitance are in series with the load, and in the parallel inverter the inductance and capacitance are effectively in parallel with the load. A number of modifications of these basic circuits can be made. However, their characteristics are usually similar to one of the two basic circuits.

Inverters with fixed components are sensitive to changes in both load and frequency. An exact determination of this dependence is difficult, but a few qualitative comments can be made. With respect to load changes the series and parallel inverters have opposite behavior. The series circuit fails to develop sufficient commutation time or voltage when very lightly loaded, while on heavy overloads it develops extremely large voltages and nearly a quarter of the cycle is devoted to commutation time. The parallel circuit fails to develop sufficient commutation time or voltage on heavy overloads, while on light loads an increasing fraction of the cycle is available for commutation time and voltage increases. To maintain a useful output-current waveform from the series inverter, the inductance and capacitance are selected to be resonant at the desired operating frequency and of such size that the series circuit is underdamped. This limits the possible range of operation to frequencies near the resonant frequency. The parallel inverter can provide a usable output current at frequencies far away from its natural resonant frequency, and there is no requirement that the circuit be underdamped. It has the capability of operating over a large range of frequencies.

Series inverters have a definite advantage over parallel inverters at high operating frequency, where a large fraction of the cycle must be allowed for commutation time. With a well-matched load the series inverter can be operated with nearly a quarter of the cycle used for commutation time without developing excessive voltages. Thus, at frequencies above five kilocycles series inverters are used because they can convert more power for a given volt-ampere rating of SCR's. At lower frequencies the parallel inverter does not develop large voltages and, because it makes more effective use of the current ratings of the SCR's, it can convert a greater amount of power in terms of the volt-ampere ratings of the SCR's used. At low frequencies the size of the inductance required by the series inverter is an important factor in limiting the use of this type of inverter. The volt-ampere rating of the inductor, which determines its physical size, is approximately twice the volt-ampere rating of the load. The large size of the inductor may be in part compensated by the fact that the series inverter can be directly coupled to the load. In most applications, however, this is not possible, because a transformer is required either for impedance matching or isolation. The output impedance of high-power inverters is a few ohms or less. The parallel inverter has no such rigid requirement on the size of the inductance required.

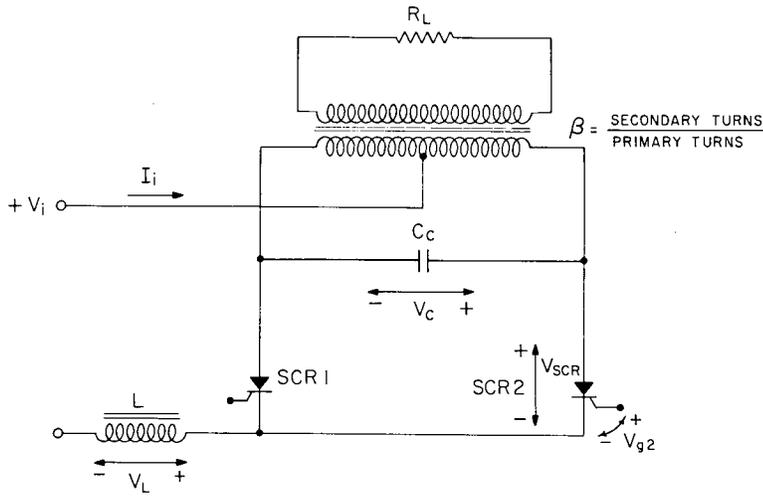
The parallel inverter was chosen for development as a low-audio-frequency sonar transmitter because it appeared to make more effective use of the volt-ampere ratings of the controlled rectifiers, be capable of operation over a wider range of frequencies, and be smaller in size than the series inverter. Some characteristics of the parallel inverter (they also apply to all inverters using controlled rectifiers) need to be emphasized to distinguish them from linear amplifiers, which are commonly used as sonar transmitters. The ac output voltage or current level of the inverter is proportional to the dc input voltage. For fixed values of circuit components the only means of controlling the output level is by changing the input voltage. The frequency of the output waveform is established by low-level pulses applied to the gates of the SCR's and can be easily controlled. The output waveform is determined by the reactive elements in the inverter and the impedance of the load and can be expected to contain an appreciable amount of harmonic distortion. Since the load impedance and the impedance of the reactive elements in the inverter are functions of frequency, the inverter output will have a strong dependence on frequency.

This report describes the design of a parallel inverter unit to which auxiliary circuits have been added to control its starting and stopping and to make it otherwise more suitable to be used as a sonar transmitter. Simple equations have been derived under the assumption that the inverter input current can be considered to be constant. The calculated performance of the inverter is compared with the measured performance of the inverter driving an array of variable-reluctance transducers.

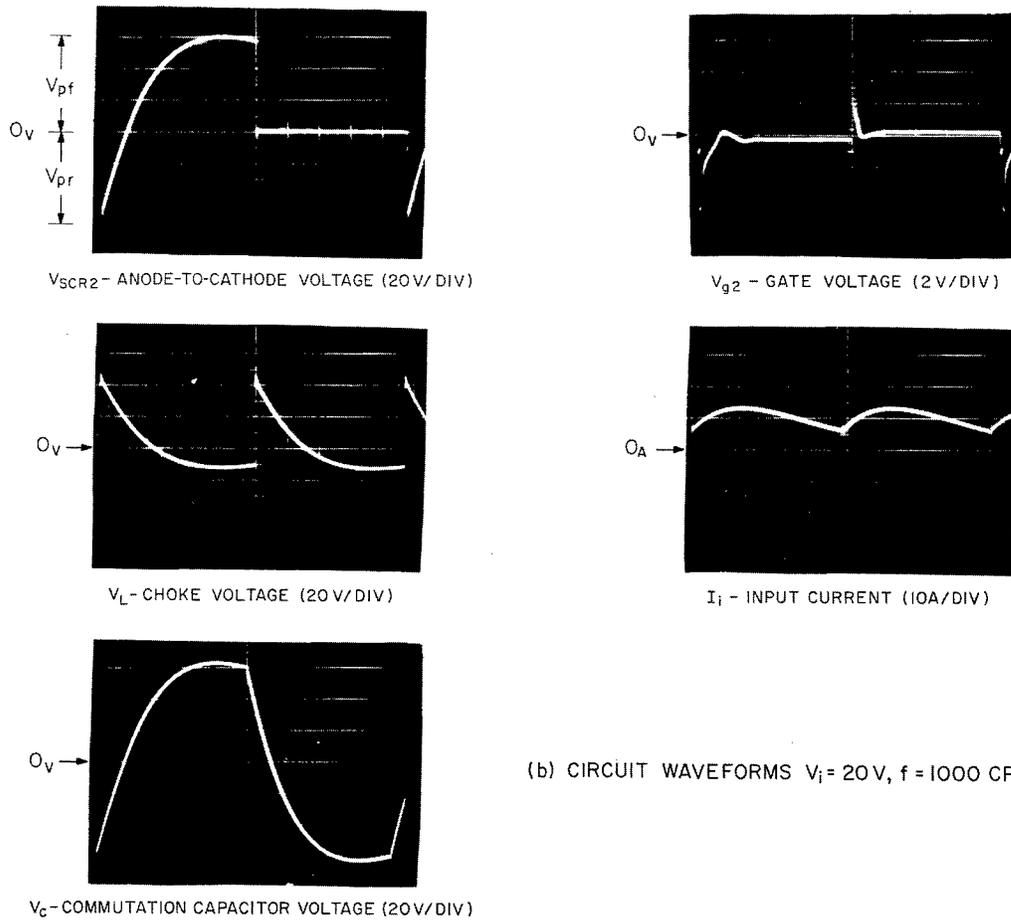
PARALLEL INVERTER CIRCUIT AND LOAD

Inverter Circuit

The parallel inverter circuit (Fig. 1a) consists of a pair of silicon-controlled rectifiers, an iron-core choke of inductance L , a commutation capacitor of value C_c , and a center-tapped output transformer with secondary-to-primary turns ratio of β . The dc input voltage is inverted to an ac output voltage by allowing the SCR's to conduct current alternately. The duration an SCR conducts is $T/2$, with T being the period of the output voltage across the load. The SCR's are driven into their conducting state by applying a positive voltage pulse to their gate terminals for a few microseconds. They then continue to conduct as long as a positive voltage is on the anode. A reliable drive for the SCR gates in this circuit is obtained from the differentiated output of the two sides of a driven flip-flop circuit. In the off state only a few milliamperes of current can flow through the SCR with either a positive or negative voltage on the anode. In the on state the SCR conducts in the forward direction with about a one-volt drop.

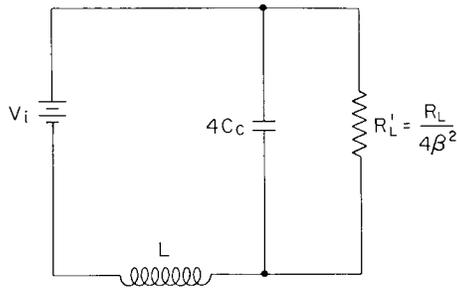


(d) PARALLEL INVERTER CIRCUIT



(b) CIRCUIT WAVEFORMS $V_i = 20\text{ V}$, $f = 1000\text{ CPS}$

Fig. 1 - Parallel inverter circuit, waveforms, and equivalent circuit



(c) EQUIVALENT CIRCUIT

Fig. 1 - Parallel inverter circuit, waveforms, and equivalent circuit (Continued)

Figure 1b shows waveforms in the parallel inverter circuit operating at 1000 cps with an input voltage V_i of 20 volts. During the first half cycle, SCR1 is conducting and SCR2 is off and has across it the transformer primary voltage minus the one-volt forward drop of SCR1. The negative voltage on SCR2 at the beginning of the half cycle is the peak reverse voltage V_{pr} . It is due to the charge stored on the commutation capacitor. The voltage across the commutation capacitor decreases due to its being charged by the voltage supply V_i and, after a duration T_c , the voltage passes through zero. The time T_c during which SCR2 is reverse biased is the commutation time, which must be greater than the turn-off time of the SCR. The commutation-capacitor voltage increases and, depending on the nature of the load, may reach a maximum value, V_{pf} , before the half cycle is over. The next half cycle begins with a positive voltage pulse applied to the gate terminal of SCR2. SCR2 conducts with a one-volt drop, and the capacitor voltage is applied across SCR1; SCR1 is then back-biased, which allows it to turn off. The inverter input current I_i drawn from the power supply is the same for both half cycles. The voltage across the choke is the same for both half cycles and is the difference between half the commutation capacitor voltage and the supply voltage.

The output of the inverter (Fig. 1a) with a resistive load could be determined by making a half-cycle equivalent circuit (Fig. 1c). All components are considered to have ideal characteristics and to be lossless. The commutation capacitor and load resistance have been reflected across half of the transformer primary. The network equations for this equivalent circuit can be written and solved under the proper boundary conditions. Boundary conditions are that the current in the inductor must be the same at the beginning and end of the half cycle, and that the voltage on the capacitor must be equal in magnitude but opposite in sign at beginning and end of a half cycle. Even such a simple problem as this requires much calculation to determine the output from the inverter. For a load of the complexity of a sonar projector, which contains a number of reactive elements, the calculations involved to determine the output of the inverter become extremely long. There is a further difficulty in performing such a calculation, since a linear model for the projector load is required. Even for a simple projector, adequate linear models are difficult to obtain, and for a number of projectors interacting acoustically usually no adequate linear model will be available. Because of the length of the calculations and the difficulty in obtaining linear models for the projector, the determination of the inverter output by solving the transient problem has not been done.

For an actual inverter circuit, it is desirable to characterize performance in terms of quantities which are easily measured. These quantities are: the conversion efficiency η , the average value of the inverter input current \bar{I} , the peak forward voltage appearing on the SCR's V_{pf} , and the commutation time T_c . It is convenient to express \bar{I} and V_{pf} in terms of the input voltage and T_c in terms of the period of the output. The operation of the inverter circuit will be described in terms of the following ratios:

$$R_i = \frac{V_i}{\bar{I}} = \text{input resistance}$$

$$\frac{V_{pf}}{V_i} = \text{peak voltage ratio}$$

$$\frac{T_c}{T} = \text{commutation ratio.}$$

AC Model for Parallel Inverter and Load

The following symbols refer to the model for the inverter and load which is to be described.

V_i	dc input voltage
\bar{I}	average input current
P_i	average input power
P_o	average output power
η	conversion efficiency
V_{pf}	peak forward voltage across SCR
V_{pr}	peak reverse voltage across SCR
T_c	commutation time
T	inverter period
$f = \frac{1}{T}$	inverter operating frequency
C_c	capacitance of commutation capacitor
L	inductance of series choke
β	secondary-to-primary turns ratio of output transformer
R_L	real part of load impedance
X_L	imaginary part of load impedance
$R_L^i = \frac{1}{4\beta^2} R_L$	reflected real part of load impedance
$X_L^i = \frac{1}{4\beta^2} X_L$	reflected imaginary part of load impedance
$Z_L = R_L^i + jX_L^i$	reflected load impedance
$X_c = \frac{1}{4(2\pi f)C_c}$	reflected impedance of commutation capacitor

The inverter and load combination can be looked at as an ac circuit and, if the form of the inverter input current is assumed, simple equations are obtained for the quantities \bar{I} , V_{pf} , V_{pr} , and T_c . In Fig. 2 are drawn equivalent circuits for the two half-periods of the inverter and load, as was done in Fig. 1c. The voltage V_{ab} in the equivalent circuits is the voltage appearing across half of the transformer primary of the actual inverter circuit. The current i_{ab} is the actual inverter input current. The two half-cycle equivalent circuits can be replaced with a single ac equivalent circuit in which a current generator i_{ab} is across the terminals a and b. The symmetry of equivalent circuits requires that

$$i_{ab}(t) = -i_{ab}(t + \frac{T}{2}).$$

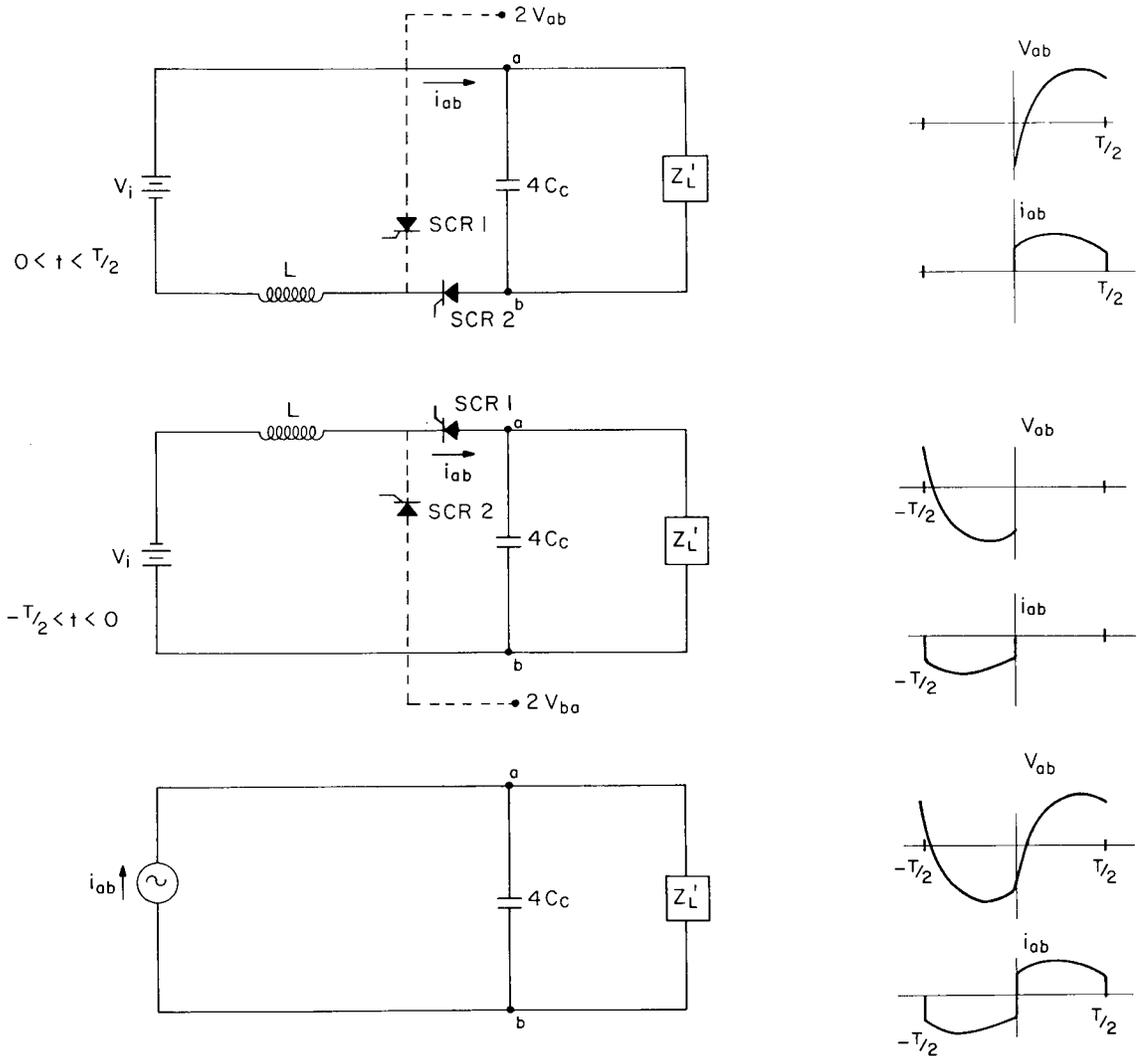


Fig. 2 - Equivalent circuit of parallel inverter

The current and voltage waveforms drawn show that i_{ab} crosses the zero axis an increment of time (which is T_c) before V_{ab} . In order for the current to lead the voltage, the impedance across terminals a and b must have a leading power factor. It can be expected that regardless of what the reflected load impedance Z_L' may be, with a large enough value of commutation capacitance, a sufficient value of T_c can be obtained for the circuit to work. The relation between the power factor and T_c illustrates the meaning of the statement that inverters must operate into leading power-factor networks. For the self-excited parallel inverter, it is customary to consider C_c as part of the inverter circuit and the load as the impedance on the secondary of the output transformer to which real power is delivered.

The inverter input current will be nearly constant if the reactance of the choke, $2\pi fL$, is much greater than the impedance across terminals a and b . Assuming that the inductance is large enough that the input current can be considered a constant, I , the ac current generator in the equivalent circuit is

$$i_{ab}(t) = \sum_{n \text{ odd}} \frac{4\bar{I}}{n\pi} \sin(2\pi nft) \quad n = 1, 3, 5 \dots \quad (1)$$

with only odd harmonics of the fundamental appearing. The impedance appearing between the terminals *a* and *b* can be written in terms of the reflected real and imaginary components of the load impedance, R'_L and X'_L , and the commutation capacitor. The reflected impedances across terminals *a* and *b* are:

$$\begin{aligned} R'_L &= (1/4\beta^2)R_L \\ X'_L &= (1/4\beta^2)X_L \\ X_C &= 1/[4(2\pi f) C_C]. \end{aligned}$$

The magnitude of the reflected impedance across terminals *a* and *b* is

$$|Z(f)| = \left[\frac{(R'_L)^2 + (X'_L)^2}{\left(1 - \frac{X'_L}{X_C}\right)^2 + \left(\frac{R'_L}{X_C}\right)^2} \right]^{1/2}, \quad (2a)$$

and phase angle ϕ is

$$\phi(f) = \tan^{-1} \left[\frac{X'_L}{R'_L} \left(1 - \frac{X'_L}{X_C}\right) - \frac{R'_L}{X_C} \right]. \quad (2b)$$

The voltage v_{ab} in the equivalent circuit is the sum of voltage due to each of the harmonic components of the current generator, and is

$$v_{ab}(t) = \frac{4\bar{I}}{\pi} \sum_{n \text{ odd}} \frac{|Z_n|}{n} \sin(2\pi nft + \phi_n). \quad (3)$$

The subscripts *n* on magnitude and phase angle of the impedance indicate these are evaluated at a frequency of *nf*.

The average power delivered into the impedance across terminals *a* and *b* is

$$P_o = \frac{1}{T} \int_{-T/2}^{T/2} i_{ab} v_{ab} dt. \quad (4)$$

Substituting the current and voltage from Eqs. (1) and (3) into Eq. (4) gives

$$P_o = \frac{8}{\pi^2} \bar{I}^2 \sum_{n \text{ odd}} \frac{|Z_n| \cos \phi_n}{n^2} \quad (5)$$

as the average output power.

For the actual inverter circuit the power from the input-voltage supply for an average input current \bar{I} is

$$P_i = v_i \bar{I}. \quad (6)$$

Assuming 100-percent efficiency, equating the input and output powers gives inverter input current as

$$\bar{I} = \frac{V_i}{\frac{8}{\pi^2} \sum_{n \text{ odd}} \frac{|Z_n| \cos \phi_n}{n^2}} \quad (7)$$

The inverter input resistance R_i is

$$R_i = \frac{8}{\pi^2} \sum_{n \text{ odd}} \frac{|Z_n| \cos \phi_n}{n^2} \quad (8)$$

The power converted by the inverter is

$$P_o = P_i = \frac{V_i^2}{R_i} = \frac{V_i^2}{\frac{8}{\pi^2} \sum_{n \text{ odd}} \frac{|Z_n| \cos \phi_n}{n^2}} \quad (9)$$

Substituting the value of \bar{I} into Eq. (3) gives

$$V_{ab}(t) = \frac{\pi V_i}{2 \sum_{n \text{ odd}} \frac{|Z_n| \cos \phi_n}{n^2}} \sum_{n \text{ odd}} \frac{|Z_n|}{n} \sin(2\pi m f t + \phi_n) \quad (10)$$

as the voltage waveform.

The peak reverse voltage on the SCR occurs at the beginning of the half cycle, which is

$$V_{pr} = 2 V_{ab}(0) \quad (11)$$

The peak forward voltage, if different from V_{pr} , can be found by differentiating Eq. (10) and setting it equal to zero to find the time, t_m , the maximum voltage occurs and evaluating V_{ab} at that time. Thus,

$$V_{pf} = 2 V_{ab}(t_m) \quad (12)$$

The commutation time T_c is found by setting V_{ab} equal to zero to determine the time of the zero crossing. The equation for T_c is

$$V_{ab}(T_c) = 0 \quad (13)$$

Both the equations for T_c and V_{pf} require the determination of the root of a function containing an infinite number of sine terms. It can be expected that only the first several terms will be appreciable, because the factors $1/n$ and $|Z_n|$ become small for large values of n . A truncated series can be used for the function and the roots found by using Newton's method or some other numerical method.

In the model just discussed, it was assumed that all inverter components were lossless and that the input current was constant. Obviously, these conditions cannot be met by an actual inverter. The actual efficiency of a fully loaded inverter at low audio frequencies is typically 90 percent. Size and weight considerations limit the inductance of

the input choke, and therefore input current will not have the exact form which has been assumed. Even with these limitations, the model is useful because it yields simple equations for \bar{I} , V_{pf} , V_{pr} , and T_c which will be seen to give a good estimate of the measured values over a large range of conditions.

SONAR TRANSMITTER

Design Specifications

The output power and operating frequency of the sonar transmitter which was built were dependent on the sonar projector available for testing it. With this consideration, a decision was made to build a transmitter capable of continuous output power of three kilowatts at a frequency of 1000 cps. Knowing the power and frequency, it was then possible to state a consistent set of specifications for an inverter circuit and its performance.

Maximum input voltage	120 volts dc
Maximum input current	30 amperes dc
Efficiency	85 percent
Input resistance	4 ohms
Peak voltage ratio	less than 4
Commutation ratio	greater than 0.02

Selection of Inverter Components

Silicon-Controlled Rectifiers: Two 2N689's—The 2N689 SCR has an average current rating of 16 amperes for a 180-degree conduction angle at frequencies up to 400 cps. Switching losses are still small at 1000 cps, so a 15-ampere average current rating at 1000 cps is reasonable. The pair of 2N689's can carry a maximum inverter input current of 30 amperes. A heat sink with thermal resistance of less than 2°C per watt working to an ambient of 25°C is sufficient to keep the junction temperature of the SCR below the maximum rating of 125°C . With a peak-voltage ratio of less than four, the voltage on the SCR's will not exceed their repetitive voltage rating of 500 volts. The turn-off time for the 2N689 is nominally 20 to 30 microseconds.

Commutation Capacitors: Three 10-microfarad, 1000-wvdc—In selecting the commutation capacitor, it is necessary to consider both the current and voltage rating. Current depends on the time rate of change of voltage across the capacitor. In inverter operation, the capacitor voltage waveform may have a steep slope, which results in an appreciably higher current than would be calculated by just considering the rms value of the voltage and frequency. Exceeding the current the capacitor is designed for causes internal heating, resulting in a shortened capacitor life. To allow for the large current, capacitors with a 1000-wvdc rating were used, although the maximum voltage was less than 500 volts peak. In retrospect, both for size and reliability considerations, it would have been desirable to have used capacitors especially designed to handle the large current expected.

Choke: 0.002 Henry, NRL #11143—The basic specifications for a choke are inductance, dc current, rms voltage, and frequency. The maximum dc current has been given as 30 amperes. A large value of inductance is desirable, but a compromise must be made to keep the size of the inductor down. Since the size of a choke is proportional to the maximum energy stored in it, if the current is nearly constant, size will be proportional to the inductance. A value of inductance of 0.002 henry was chosen, which gives a reactive impedance of three times the expected inverter input resistance. The fundamental frequency of the voltage across the inductor is 2000 cps, or twice the inverter

frequency. From measurements on previous inverter circuits, and considering the worst case of operation, an rms voltage rating equal to the inverter input voltage was specified. The choke voltage waveform contains a large harmonic content, which can be expected to contribute most of the losses in the choke. Twelve-mil, grain-oriented, silicon steel laminations were used for the choke. The choke contained a large air gap, so there was no problem of residual magnetism.

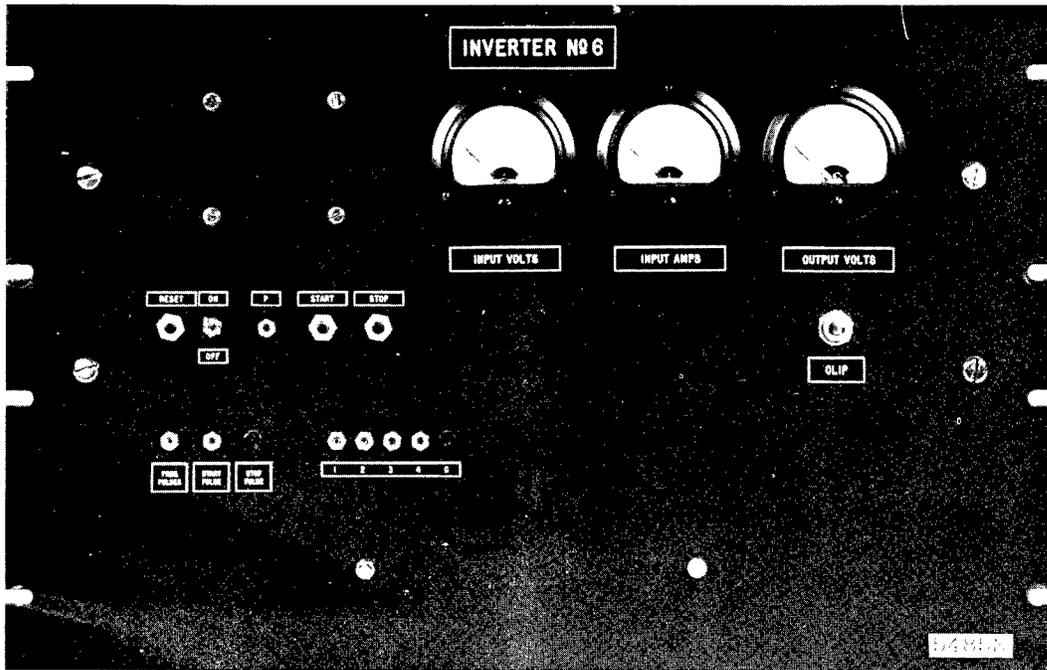
Output Transformer: 25 Ohms Center-Tapped to 3 Ohms, NRL #11181—The secondary impedance of the output transformer is determined by the load impedance, which was given as three ohms. The primary impedance was chosen so that it, together with the reflected commutation capacitor impedance, will give an inverter input impedance of four ohms. Using a value for C_c of 3.3 microfarads, the primary impedance was determined to be 25 ohms. The primary winding carries, in addition to the reflected load current, the reactive current of the commutation capacitor, and this was stated in the transformer design. It is possible that when the inverter is stopped the transformer core may be left in a state of high residual magnetism. To prevent the transformer from saturating when the inverter is started again, it is necessary to design the transformer so that the peak flux in the core is well below the saturation level during normal operation. This increases the size of the transformer but also increases the efficiency and eliminates the problem of saturation with turn on of the inverter.

Transmitter Circuit

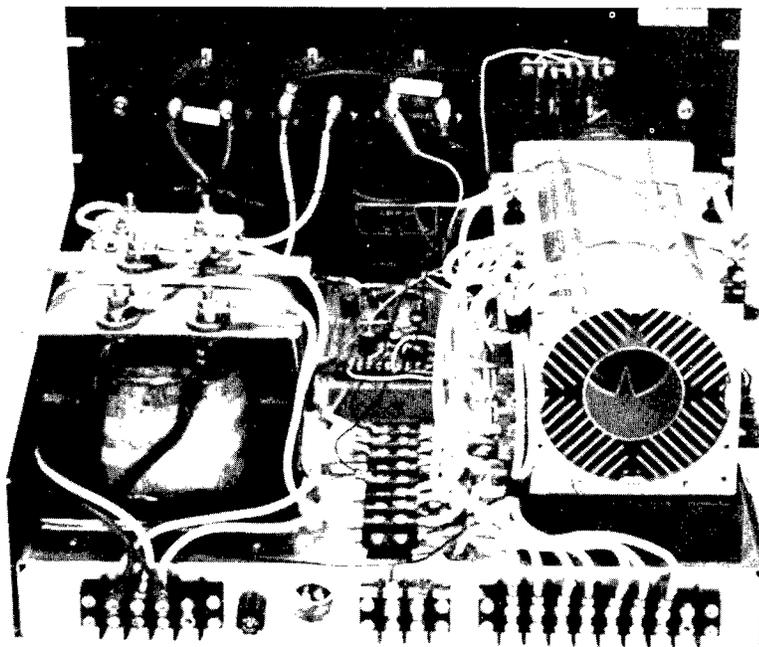
The complete transmitter consists of the parallel inverter circuit, already described, and additional circuits to control the operation of the inverter. The additional circuits include, a gating circuit for starting and stopping the inverter, a driver stage for the inverter, an overcurrent detecting circuit, and a three-phase bridge and filter rectifier. The rectifier and filter were included so that a three-phase ac voltage line could provide a dc input voltage for the inverter. The output level of the transmitter can be changed by changing the level of the three-phase ac input voltage. It might be desirable in the future to include as part of the transmitter a variable dc power supply so that the output level of the transmitter could be controlled. The design of such a power supply is an independent problem and is not considered in this report. There are three types of low-level signals entering the transmitter to control its operation. First is a train of pulses to the driver stage which determines the output frequency of the inverter. Second are pulses to start the inverter, and third are pulses to stop the inverter. All these signals are generated by a circuit external to the transmitter.

The transmitter constructed was an experimental unit, and no attempt was made to package it in the smallest possible size. Because of the switching mode of operation of all the circuits the operation of the transmitter is not expected to be affected by the physical layout of the components. The inverter-circuit output transformer was not included on the chassis with the rest of the transmitter. Because it is used for matching to a particular load impedance and frequency range, it was not convenient to mount it with other components. Figure 3 shows two views of the transmitter mounted on a chassis behind a 12-inch relay-rack panel. On the front panel are three meters for monitoring the inverter unit, jacks for input signals, and switches for manually controlling the transmitter. All of the power semiconductor components are mounted on a forced-air-cooled heat sink on one side of the chassis. On the other side of the chassis are the inverter choke and three 10-microfarad commutation capacitors. The power for the transmitter is brought in at the back of the chassis: three-phase 60-cps voltage for the inverter unit, 110 volts ac for fan motor, and 15 volts dc for control circuits.

Figure 4 shows the schematic of the transmitter. The three-phase input voltage is rectified by a full-wave bridge using 1N2156 rectifiers. The 1800-microfarad electrolytic capacitor smooths the rectifier output voltage and provides the inverter unit with a



(a) Front panel, showing meters, input signal jacks, and manual control switches



(b) Back view of chassis; heat sink for semiconductor on right, choke and commutation capacitors on left

Fig. 3 - Experimental transmitter

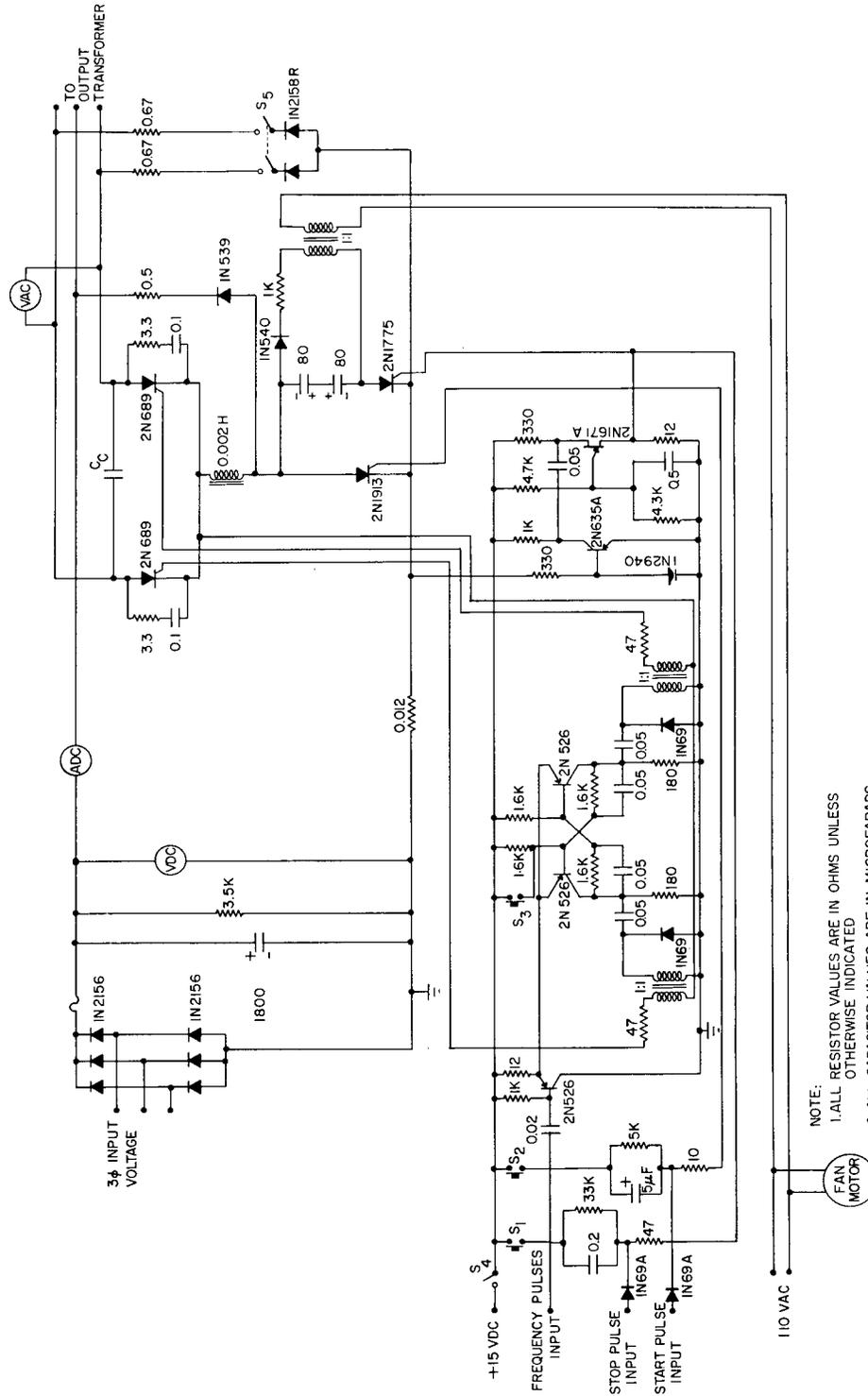


Fig. 4 - Complete transmitter circuit

low-impedance source of dc voltage. The three-phase voltage can be varied from 10 to 85 volts rms to control the output power of the inverter unit. Panel meters measure the dc current and voltage to the inverter unit. On the back of the chassis are three terminals for a connecting cable running to the output-transformer primary. A panel meter across the transformer primary gives an indication of the peak voltage on the SCR's. Three 10-microfarad, 1000-wvdc commutation capacitors are available which can be connected in series or parallel to give values of C_c of 3.3, 5.0, 10, 15, 20, and 30 microfarads. Across the SCR's are series RC networks to suppress voltage transients caused by the steep current waveform when the SCR turns off. A switch, S_5 , is provided to connect rectifiers to the transformer primary; these rectifiers clip the output voltage at roughly twice the inverter input voltage.

The gating circuit which controls the starting of the inverter unit consists of a 2N1913 and a 2N1775 SCR, an 80-microfarad capacitor, and a charging circuit for the capacitor. The path of the inverter input current is through the 2N1913 and, when it is off, only a few milliamperes of leakage current can flow. The voltage across it is the output voltage V_i of the bridge rectifier. The 80-microfarad capacitor is kept charged to 150 volts by a half-wave rectifier working through an isolation transformer from the 110-volt ac line. The 2N1775 voltage is 150 volts plus V_i . The inverter unit is started by applying a voltage pulse to the gate of the 2N1913 through the start-pulse input jack on the front of the panel, or the manual pushbutton S_2 . With the 2N1913 SCR on, the inverter input current flows through it. The inverter is stopped by a voltage pulse to the gate of the 2N1775, either through the stop-pulse input jack or manual pushbutton switch S_1 . The 80-microfarad capacitor is dumped across the 2N1913, backbiasing it, and allowing it to turn off. The capacitor voltage begins to oscillate but, when it becomes equal to the bridge rectifier voltage V_i , it is clamped by the 1N539 diode and the 2N1775 can turn off. After about 0.2 second, the 80-microfarad capacitor is recharged and the inverter is again ready to be turned on.

The pulses controlling the inverter operating frequency enter the transmitter through the frequency-pulse input jack on the front of the panel. They are capacitively coupled to an emitter follower which drives a flip-flop circuit using a pair of 2N526's. The output of the two sides of the flip-flop is differentiated to obtain pulses which are transformer coupled to the gates of the SCR's. The gates of the inverter SCR's can be driven continuously with the starting and stopping of the inverter being controlled by the 2N1913. One side of the flip-flop circuit has a reset switch, S_3 . Before the input-frequency pulses are applied, S_3 resets the flip-flop so that it will start with a known state. This reset operation is required only when driving a number of transmitters in phase from the same frequency input.

All dc-to-ac inverters using controlled rectifiers have the problem that failure of commutation results in a short-circuit current being drawn from the voltage supply through the SCR's. In the parallel inverter, failure of commutation can result from interruption of the gate signal to the inverter SCR's, or a load impedance change, which results in insufficient commutation time for the SCR's. Excessive or short-circuit currents are sensed across the 0.012-ohm resistor after the 2N1913 SCR. When the voltage across this resistor rises above 400 millivolts, the 1N2940 tunnel diode switches to its low-resistance state, turning on the 2N635A transistor. This triggers a one-shot uni-junction transistor, 2N1671A, which applies a voltage pulse to the 2N1775 to stop the inversion process.

COMPARISON OF MEASURED AND CALCULATED PERFORMANCE OF TRANSMITTER

Experimental Procedure

Testing of the sonar transmitter was performed at the U.S. Navy Electronics Laboratory, Pend Oreille Calibration Station, in October 1962. The load for the transmitter

consisted of a 36-element planar array of variable-reluctance transducers having a resonant frequency of 960 cps. The characteristics of the array were first measured by driving it with a sinusoidal voltage from a linear amplifier. Measurements included electrical input impedance, response at constant driving current, beam pattern, and acoustic efficiency. These data are given in the appendix.

In taking data on the variable-reluctance projectors, it has been customary to keep the driving current constant. This was done in these tests at a value of 25 amperes, which gave a maximum power into the array of 2100 watts. Keeping the driving current constant, while operating at various frequencies about the resonance, required varying the three-phase input voltage to the transmitter.

Because of losses in the magnetic components in the inverter, the efficiency of the transmitter has a dependence on output waveshapes and power factor which is difficult to state quantitatively. There is also a dependence of transmitter efficiency on input voltage. This is a nearly linear dependence, because it is due to the forward voltage drop of the semiconductor through which the dc current flows. The dc current flows through two rectifiers in the bridge rectifier unit, one SCR in the inverter circuit, and the SCR in the gate circuit. This gives a total forward voltage drop of approximately five volts. Figure 5 shows the measured efficiency of the transmitter (conversion of three phase input power to single phase output power) as a function of input voltage to the inverter unit V_i . Each point represents the efficiency of the transmitter delivering 25 amperes driving current to the array at undefined frequency and tuning. The plot is presented to show the strong dependence of efficiency on input voltage. Operating near full voltage, an efficiency of from 85 to 90 percent is obtained.

Data on performance of the transmitter-project combination were taken at discrete frequencies for six combinations of inverter and array tuning. These represented two values of series-tuning capacitance for the projector, $C_T = 72$ and 108 microfarads, and

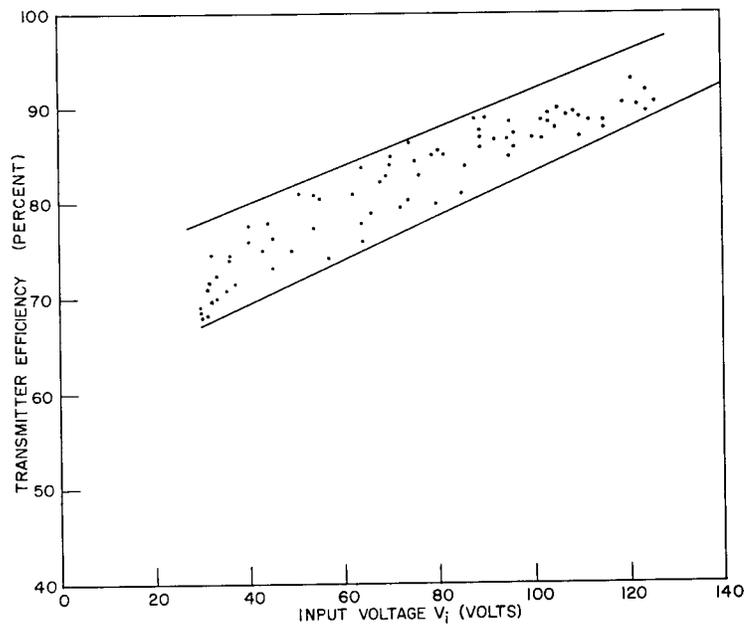


Fig. 5 - Measured transmitter efficiency versus inverter input voltage V_i

three values of commutation capacitance in the inverter, $C_c = 3.1, 4.6,$ and 9.2 microfarads. Data were taken over the frequency range for which the commutation time was greater than 20 microseconds.

Having established the load on the inverter (the projector impedance given in Appendix A), calculation of $R_i, V_{pf}/V_i,$ and T_c/T can be done using Eq. (8), (12), and (13). They were derived with the assumption that input current was constant. It will be seen from the waveforms that this assumption is not met exactly. Also, the efficiency of the inverter varies from about 70 to 90 percent. For these two reasons, fine agreement between calculated values of $R_i, V_{pf}/V_i,$ and T_c/T and measured values was not expected. However, even approximate agreement is significant.

Before calculating these quantities, consider the impedance Z appearing across half the transformer primary. For frequencies above 2000 cps, the load impedance is due to the clamped inductance of the array, which is about 400 microhenries. At these frequencies, the impedance Z is due to reflected clamped inductance in parallel with reflected commutation capacitance $4C_c$. The calculated value of this impedance is in Table 1 for the first three odd harmonics of the resonant frequency and the three values of C_c .

Table 1
Impedance at Harmonic Frequencies of 960 cps

Harmonic	$C_c = 3.1 \mu f$		$C_c = 4.6 \mu f$		$C_c = 9.2 \mu f$	
	$ Z_n $	ϕ_n	$ Z_n $	ϕ_n	$ Z_n $	ϕ_n
3rd	5.9	$-\pi/2$	3.5	$-\pi/2$	1.6	$-\pi/2$
5th	2.8	$-\pi/2$	1.8	$-\pi/2$	0.9	$-\pi/2$
7th	1.9	$-\pi/2$	1.3	$-\pi/2$	0.6	$-\pi/2$

At frequencies near resonance, the impedance seen by the fundamental component of the current is greater than the impedance seen by the harmonics. Using these results, the expression for the input resistance is simplified. From Eq. (8),

$$R_i = \frac{8}{\pi^2} \sum_{n \text{ odd}} \frac{|Z_n| \cos \phi_n}{n^2}$$

Since for $n > 1, |Z_n| < |Z_1|,$ and $\phi_n = -\pi/2,$ Eq. (8) may be simplified to

$$R_i = \frac{8}{\pi^2} |Z_1| \cos \phi_1 \tag{14}$$

From Eq. (10),

$$V_{ab}(t) = \frac{\pi V_i}{2} \sum_{n \text{ odd}} \frac{|Z_n| \cos \phi_n}{n^2} \sum_{n \text{ odd}} \frac{|Z_n|}{n} \sin(2\pi n f t + \phi_n)$$

and again using $|Z_n| < |Z_1|$ and $\phi_n = -\pi/2,$ we have

$$V_{ab} \approx \frac{\pi V_i}{2 \cos \phi_n} \left[\sin(2\pi f t + \phi_1) + \frac{1}{3} \left| \frac{Z_3}{Z_1} \right| \sin(6\pi f t + \phi_3) + \text{smaller terms} \right]$$

where the first two terms would give an approximation for v_{ab} . For a rough estimate that can easily be calculated, only the first term is used,

$$v_{ab} = \frac{\pi V_i}{2 \cos \phi_1} [\sin (2\pi ft + \phi_1)]. \quad (16)$$

The peak forward voltage using this approximation is, from Eq. (12),

$$V_{pf} = \frac{\pi V_i}{\cos \phi_1}, \quad (17)$$

and the peak voltage ratio is

$$\frac{V_{pf}}{V_i} = \frac{\pi}{\cos \phi_1}. \quad (18)$$

Similarly the commutation time becomes, from Eq. (13)

$$T_c = -\frac{\phi_1}{2\pi} T, \quad (19)$$

and the commutation ratio

$$\frac{T_c}{T} = -\frac{\phi_1}{2\pi}. \quad (20)$$

These approximations for R_i , V_{pf}/V_i , and T_c/T will be compared with the measured values.

Test I, Array Tuning of 108 Microfarads

In the first test of the transmitter, a capacitor of 108 microfarads was placed in series with the projector array to cancel in part the inductive component of the array impedance. The three-phase input voltage to the transmitter was adjusted to give a driving current to the array of 25 amperes rms. Data on the performance of the transmitter and projector array were taken at a number of frequencies over the range of frequencies for which operation was possible. This range was determined by the requirements that the commutation time in the inverter be greater than 20 microseconds. Three values of commutation capacitance were used: $C_C = 3.1, 4.6$ and 9.2 microfarads.

Figure 6 is a plot of T_c/T versus frequency for the three values of C_C used. Here T_c/T , which is a fraction of a period, is also expressed in degrees as an equivalent phase angle. The plot shows that increasing C_C increases the commutation ratio and extends the frequency range over which it is possible to operate the inverter. Figure 7 is a plot of the input resistance, showing that the effect of increasing C_C is to decrease the input resistance. Figure 8 shows the peak-voltage ratio. The three curves in this figure are not separated to the extent they were in the previous two figures. The principal effect of increasing C_C is to increase the peak-voltage ratio, at least near the resonance of the load.

Using the known value of array impedance at 25 amperes and the value of 108 microfarads series tuning, the reflected impedance for the three values of commutation capacitance was calculated. Its magnitude $|Z_1|$ and phase angle ϕ_1 are plotted in Figs. 9 and

Fig. 6 - Measured value of commutation ratio of inverter unit, also expressed in degrees; $C_T = 108$ microfarads

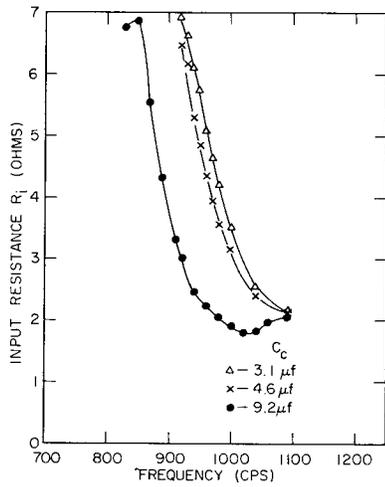
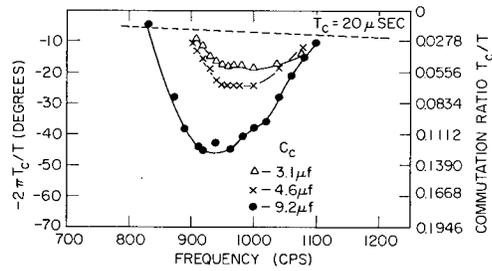


Fig. 7 - Measured value of inverter input resistance; $C_T = 108$ microfarads

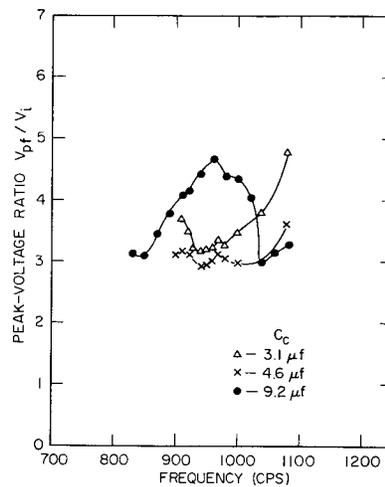


Fig. 8 - Measured value of peak-voltage ratio of inverter; $C_T = 108$ microfarads

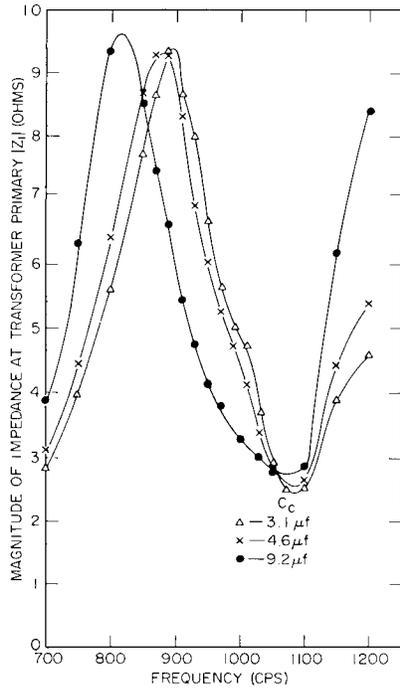


Fig. 9 - Calculated magnitude of impedance across transformer primary half $|Z_1|$; $C_T = 108$ microfarads

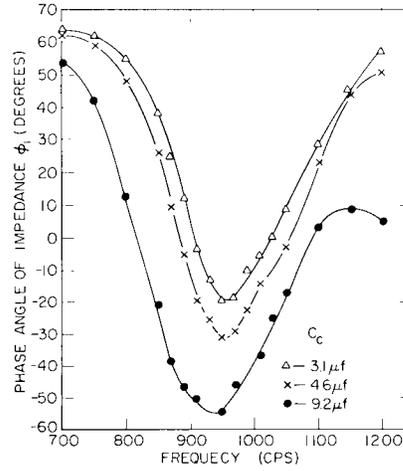


Fig. 10 - Calculated phase angle of impedance across transformer primary half ϕ_1 ; $C_T = 108$ microfarads

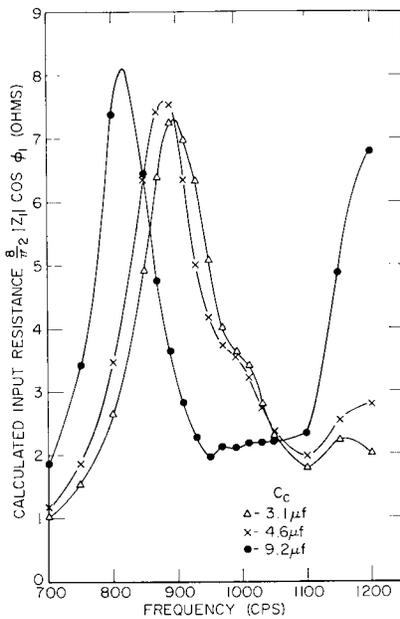


Fig. 11 - Calculated inverter input resistance $\frac{8}{\pi^2} |Z_1| \cos \phi_1$; $C_T = 108$ microfarads

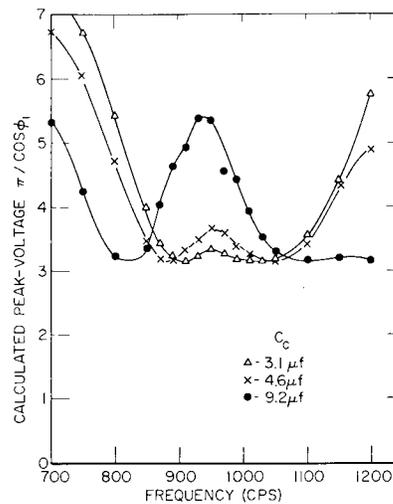


Fig. 12 - Calculated inverter peak voltage ratio $\pi / \cos \phi_1$; $C_T = 108$ microfarads

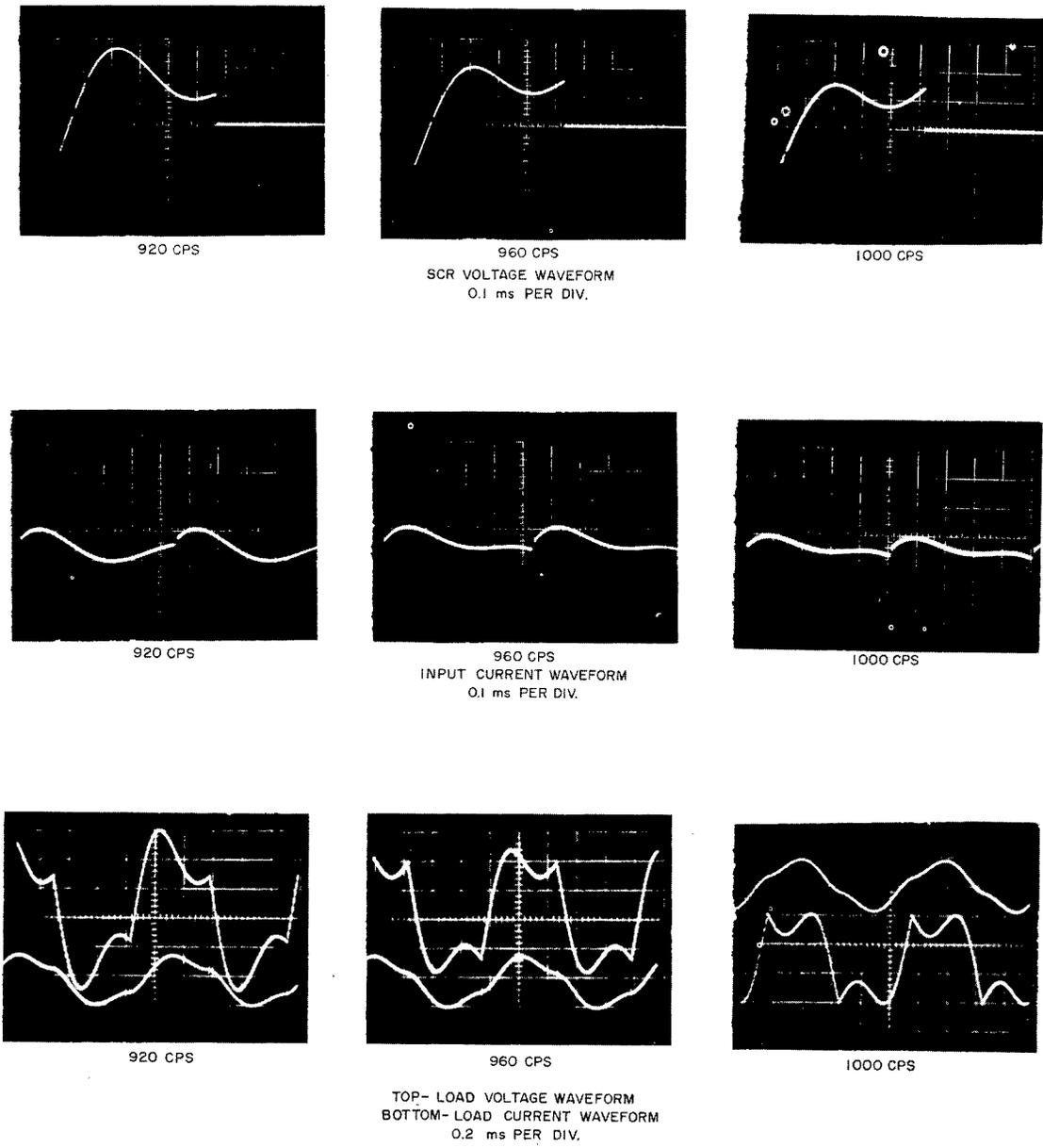


Fig. 13 - Inverter and load, voltage and current waveforms;
 $C_c = 3.1$ microfarads, $C_T = 108$ microfarads

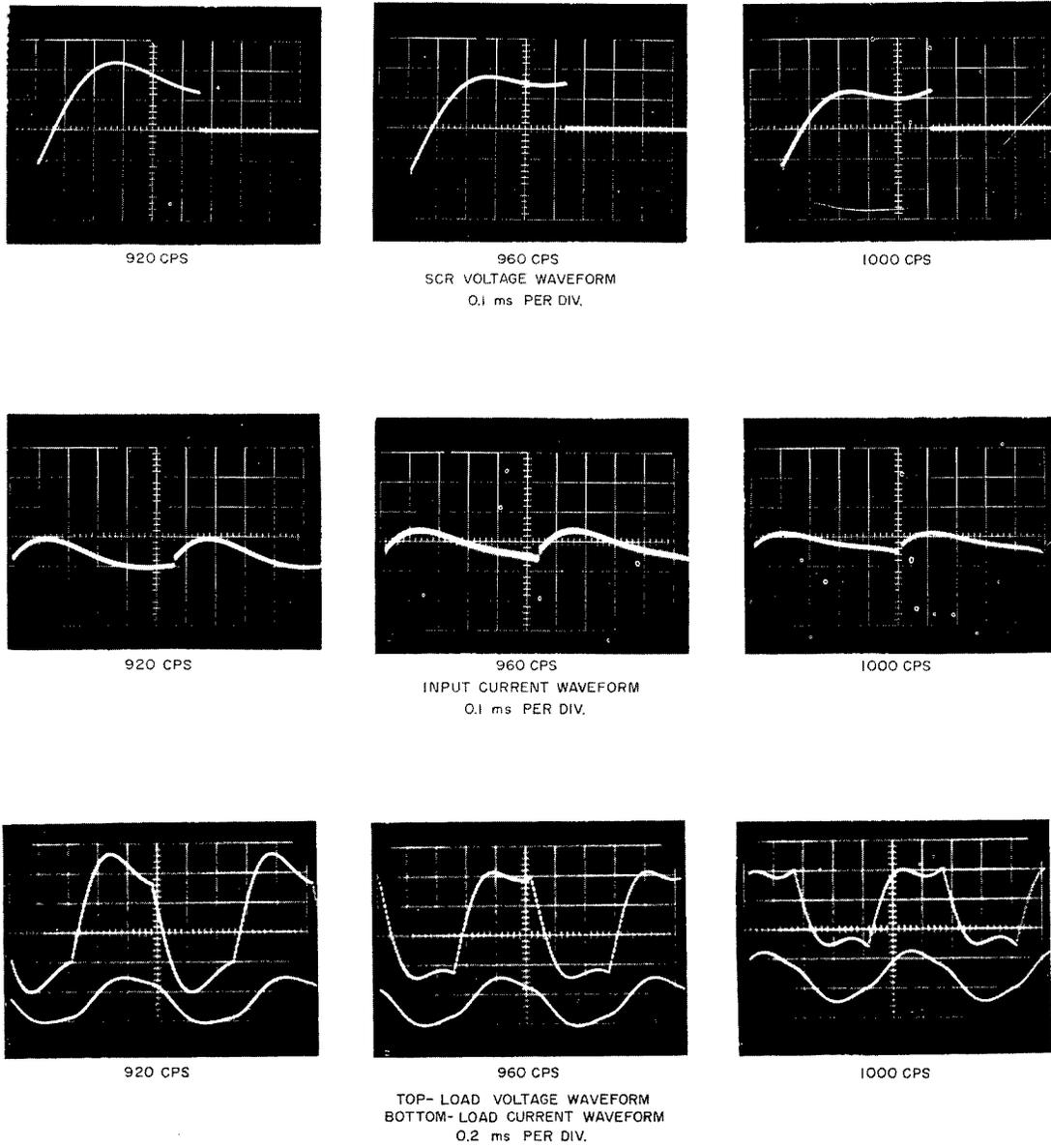


Fig. 14 - Inverter and load, voltage and current waveforms;
 $C_c = 4.6$ microfarads, $C_T = 108$ microfarads

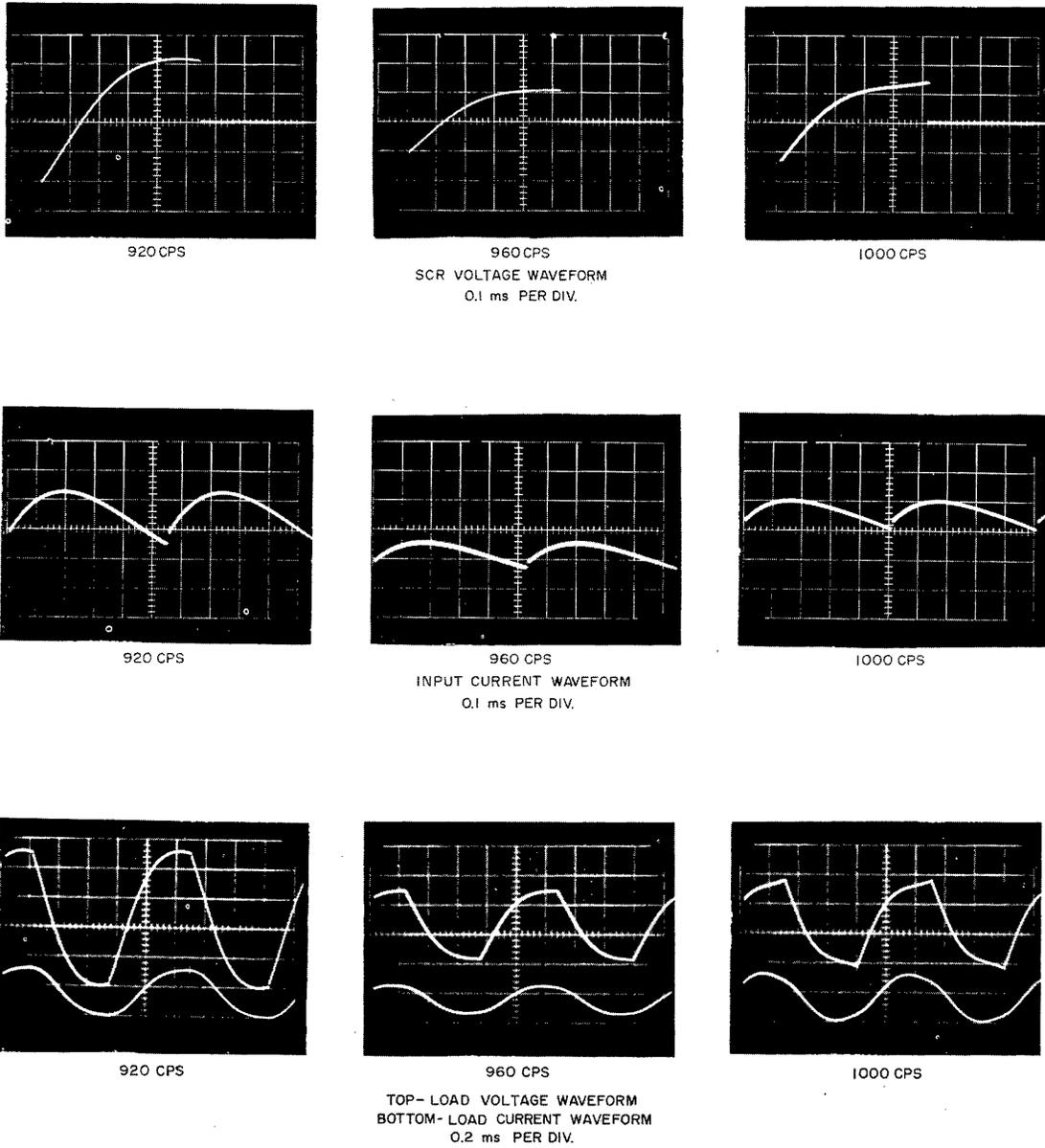


Fig. 15 - Inverter and load, voltage and current waveforms;
 $C_c = 9.2$ microfarads, $C_T = 108$ microfarads

10. The calculated input resistance $8/n^2 |Z_1| \cos \phi_1$ and peak voltage ratio $\pi/\cos \phi_1$ are plotted in Figs. 11 and 12. A comparison of Fig. 10 with Fig. 6 shows that the calculated commutation ratio is in fair agreement with the measured value of the ratio for frequencies near and below resonance. Figure 10 gives a close estimate of the low-frequency limit of the inverter. At higher frequencies, above 1000 cps, the agreement is poor, with the measured value of T_c/T being larger than the calculated value, especially for the smaller values of C_c . Comparing Figs. 11 and 7, it is seen that the form of the calculated and measured input resistance plots is similar. The measured value is slightly higher (about 10 to 20 percent) than the calculated value. Comparing Figs. 12 and 8, the peak-voltage ratio, there is seen to be some similarity, but not as much as in the previous two quantities. The calculated value of peak-voltage ratio is greater than the measured value.

Waveforms in the transmitter for the three values of C_c are shown in Figs. 13, 14, and 15. Pictures of the waveforms were taken at the resonant frequency (960 cps) and frequencies where acoustic response is down 1.5 decibels (920 and 1000 cps). The top pictures are the SCR voltage, from which T_c and V_{pf} could be determined. The middle row of pictures is the inverter input current, with zero current being the lowest horizontal grid line. These pictures show the extent to which the current was held constant during the cycle. The bottom pictures are the load current and voltage waveforms. The load voltage is seen to contain a large amount of distortion. However, the load or driving current has relatively little distortion because of higher impedance of the array at harmonic frequencies.

Test II, Array Tuning of 72 Microfarads

Tests of the transmitter were performed in the same manner as described in Test I, except that a value of series tuning of 72 microfarads was used. The measured values of commutation ratio, input resistance, and peak-voltage ratio are plotted in Figs. 16, 17, and 18. The calculated value of reflected impedance magnitude and phase angle are plotted in Figs. 19 and 20, and the calculated value of input resistance and peak-voltage ratio in Figs. 21 and 22. The comments in the previous test regarding the form of the similarity between the calculated and measured values of the quantities in the plots still hold. There is, however, an increased difference between the absolute value of calculated and measured quantities. In Test I, the difference was 10 to 20 percent, and in this test the difference is 20 to 40 percent.

Figures 23, 24, and 25 show the transmitter waveforms for the three values of commutation capacitance used.

In Fig. 26 are shown the buildup waveforms of the load current and voltage when the transmitter is started at a frequency of 960 cps. It took about seven cycles before the current and voltage reached their steady-state values. This seven-cycle buildup time can be assigned as due to the underdamped nature of the projector array and is independent of the commutation capacitance. The shape of the voltage during this buildup time depends on the value of commutation capacitance, and for the lowest value, 3.1 microfarads, there is an appreciable overshoot at about the third cycle. This points out the fact that inverters operating into an underdamped load may operate successfully in steady state, but conditions during buildup after turn on may be such that the voltage may overshoot or the commutation time may be too small. Theoretical calculations of the waveforms during this interval are necessarily lengthy and have not been done. Practically, it appears that using a large value of commutation capacitance should prevent an overshoot of the output voltage and at the same time provide enough commutation time. If a large value of commutation capacitance cannot be used, it is possible to eliminate voltage overshoot by introducing voltage clipping at an appropriate level.

Fig. 16 - Measured value of commutation ratio of inverter unit, also expressed in degrees; $C_T = 72$ microfarads

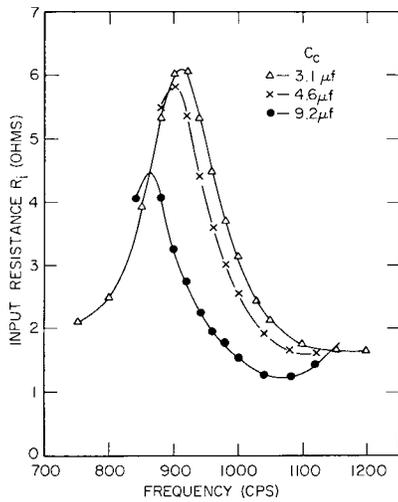
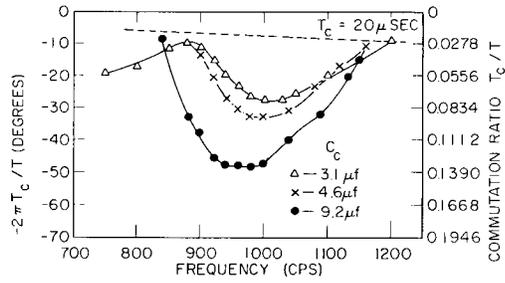


Fig. 17 - Measured value of inverter input resistance; $C_T = 72$ microfarads

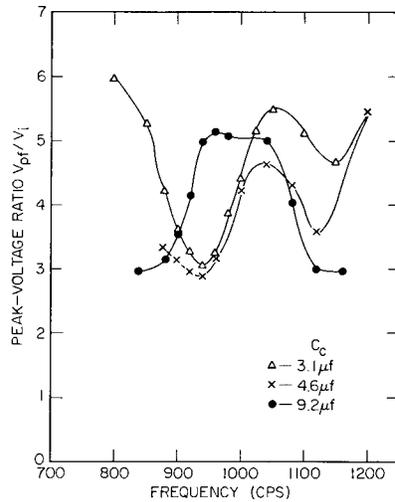


Fig. 18 - Measured value of peak-voltage ratio of inverter; $C_T = 72$ microfarads

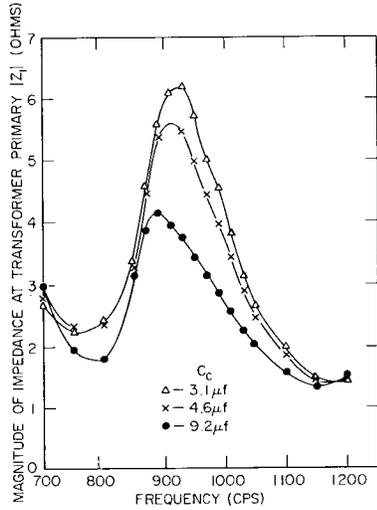


Fig. 19 - Calculated magnitude of impedance across transformer primary half $|Z_1|$; $C_T = 72$ microfarads

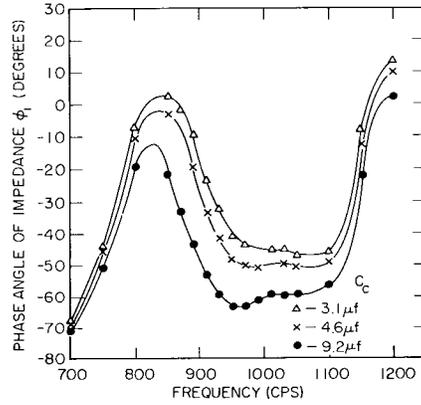


Fig. 20 - Calculated phase angle of impedance across transformer primary half ϕ_1 ; $C_T = 72$ microfarads

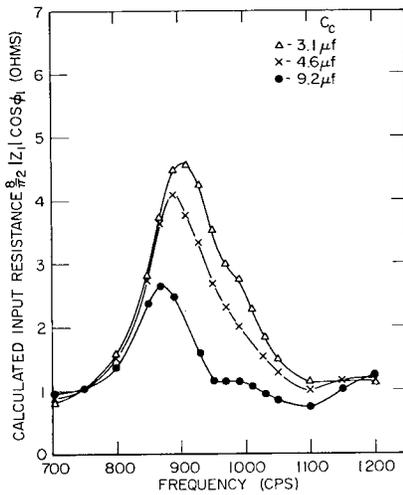


Fig. 21 - Calculated inverter input resistance $\frac{8}{\pi^2} |Z_1| \cos \phi_1$; $C_T = 72$ microfarads

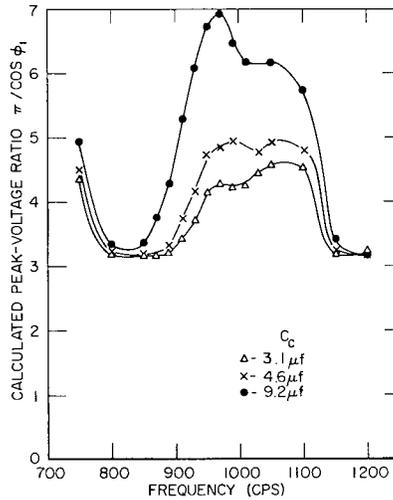


Fig. 22 - Calculated inverter peak-voltage ratio $\frac{\pi}{\cos \phi_1}$; $C_T = 72$ microfarads

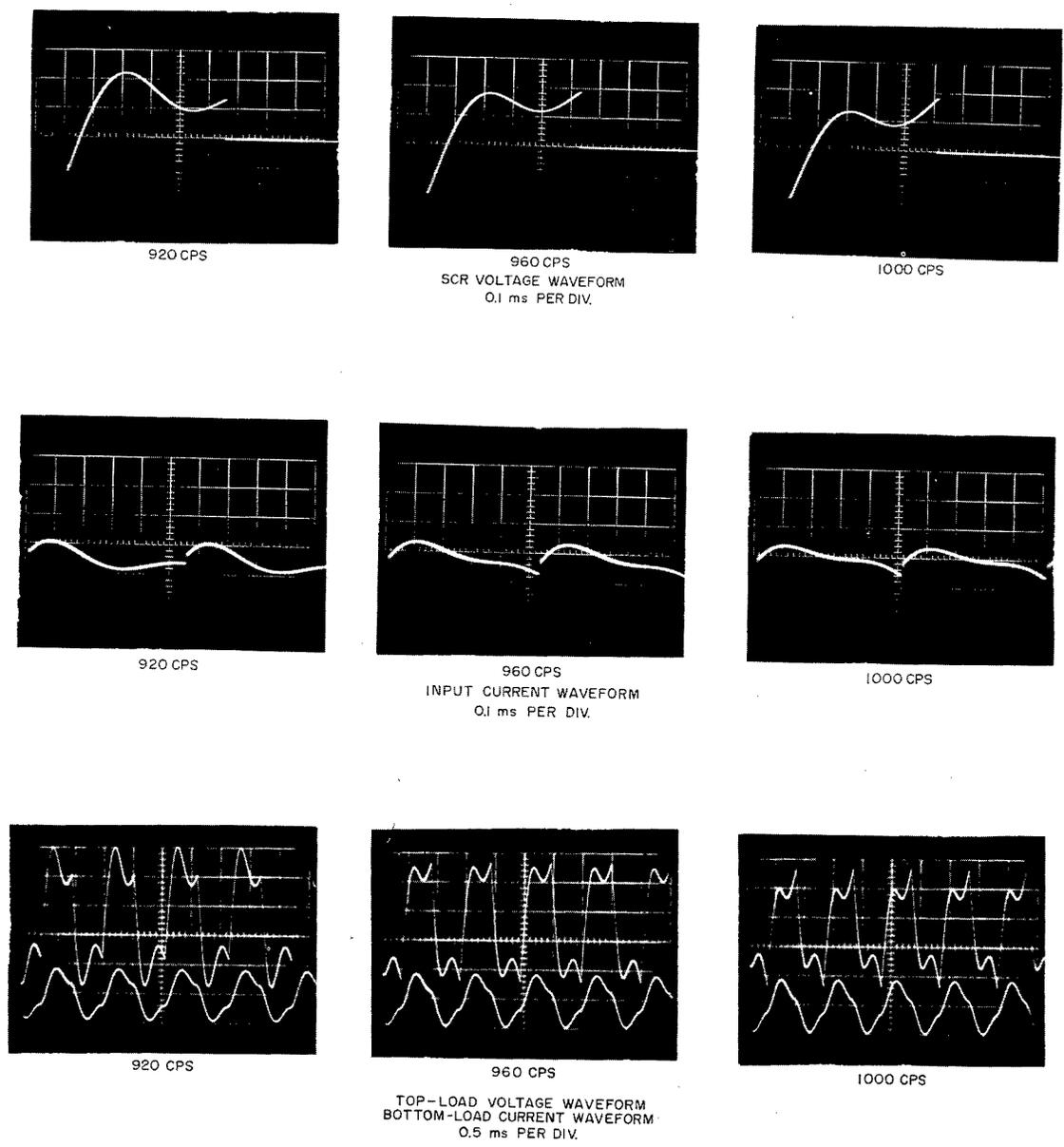


Fig. 23 - Inverter and load, voltage and current waveforms;
 $C_c = 3.1$ microfarads, $C_T = 72$ microfarads

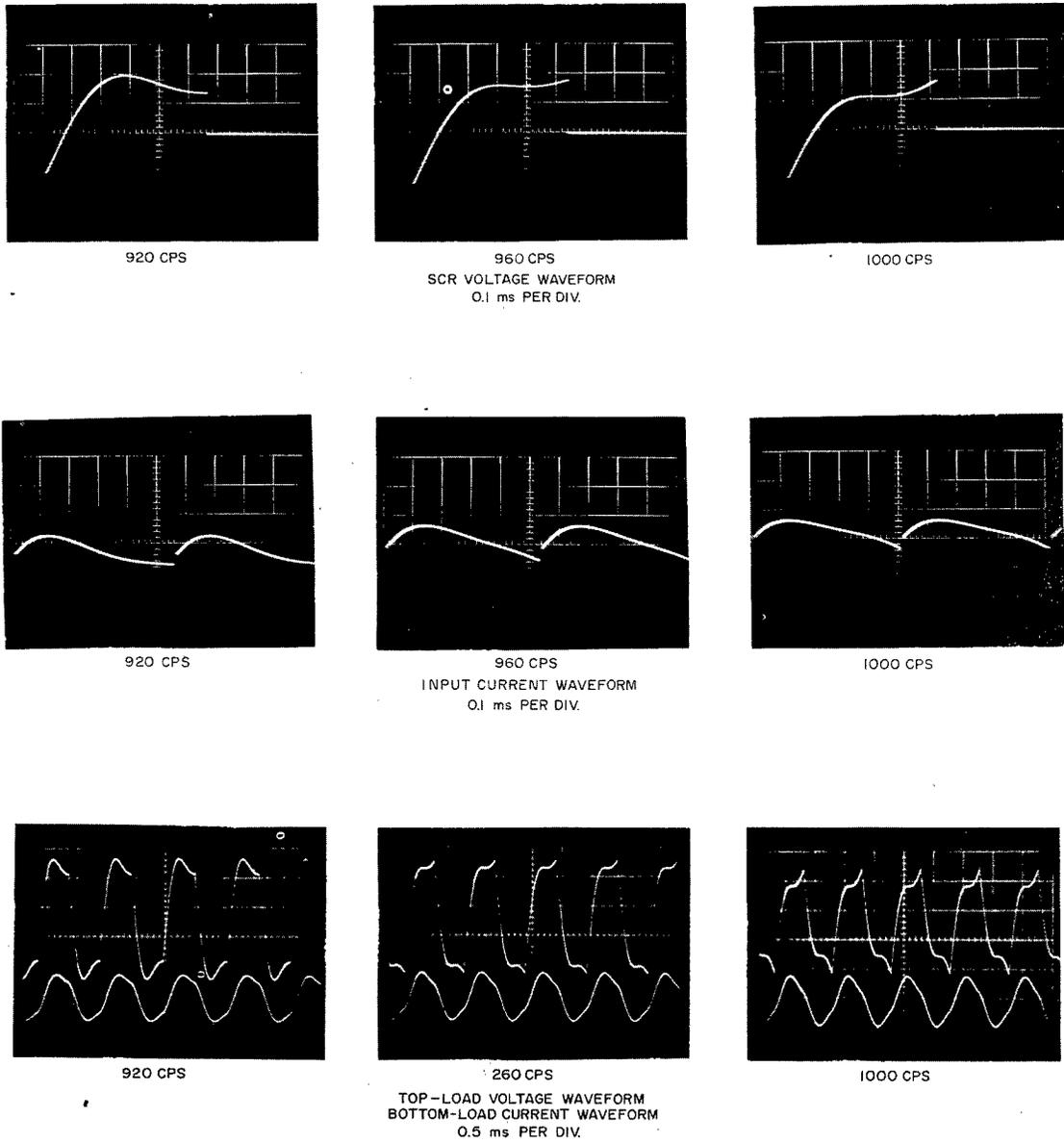
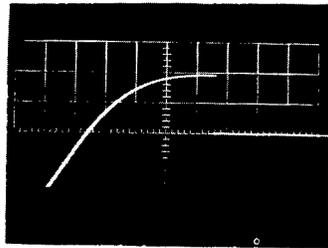
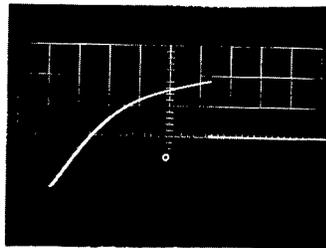


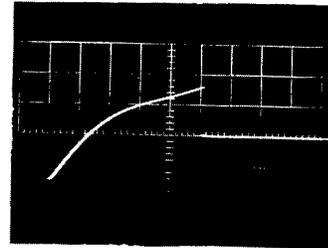
Fig. 24 - Inverter and load, voltage and current waveforms;
 $C_c = 4.6$ microfarads, $C_T = 72$ microfarads



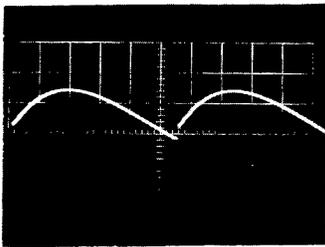
920 CPS



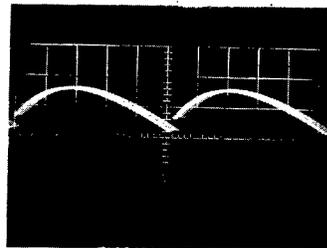
960 CPS
SCR VOLTAGE WAVEFORM
0.1 ms PER DIV.



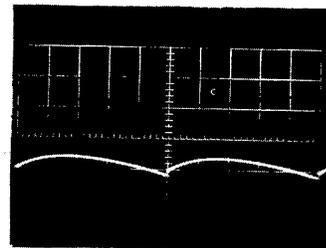
1000 CPS



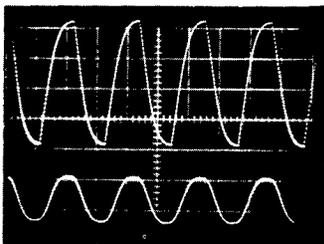
920 CPS



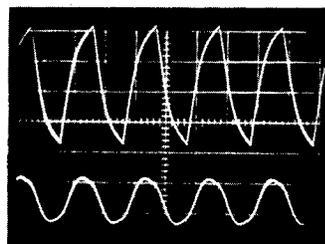
960 CPS
INPUT CURRENT WAVEFORM
0.1 ms PER DIV.



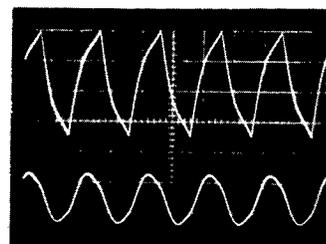
1000 CPS



920 CPS



960 CPS
TOP-LOAD VOLTAGE WAVEFORM
BOTTOM-LOAD CURRENT WAVEFORM
0.5 ms PER DIV.



1000 CPS

Fig. 25 - Inverter and load, voltage and current waveforms;
 $C_c = 9.2$ microfarads, $C_T = 72$ microfarads

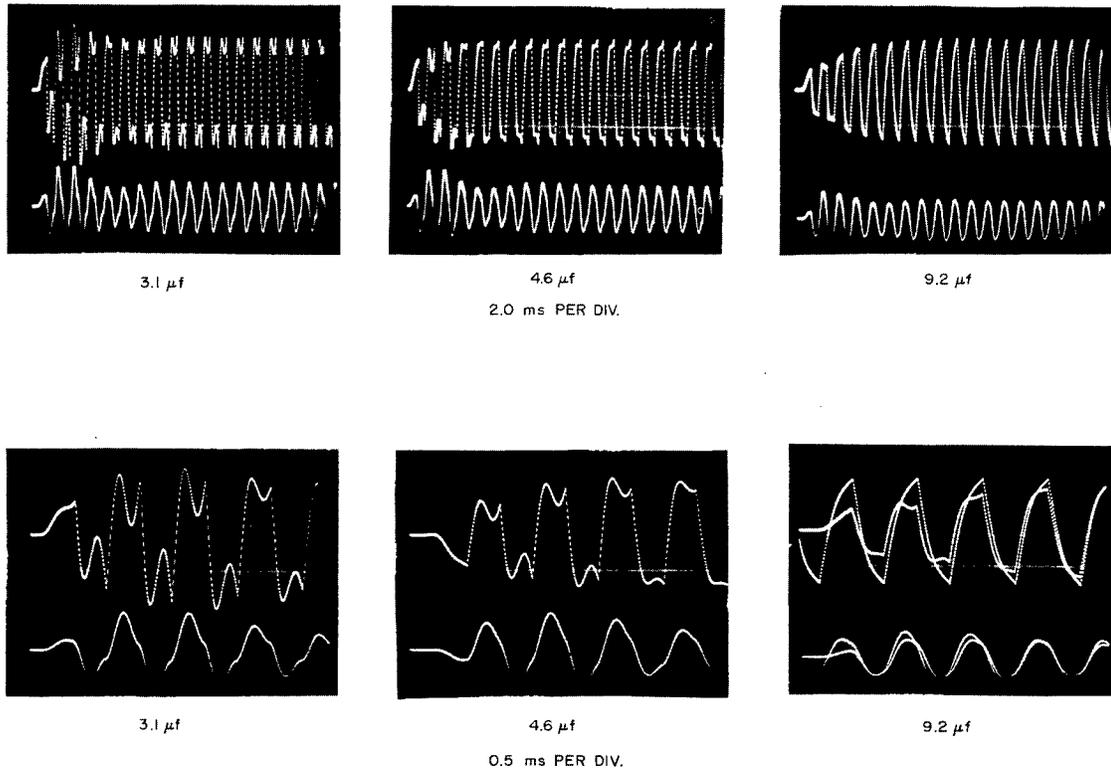


Fig. 26 - Load voltage (upper waveform) and current (lower waveform) after turning on the inverter at frequency of 960 cps. Values of C_c are 3.1, 4.6, and 9.2 microfarads; $C_T = 72$ microfarads

Test III, Clipped Output Voltage

In Test III the output voltage of the transmitter was clipped at a level of about twice the dc input voltage to the inverter. Clipping the output voltage provides the transmitter with voltage regulation which the parallel inverter does not have. Referring to the transmitter circuit (Fig. 4) when switch S_c is closed, 1N2158 rectifiers are connected to the primary terminals of the output transformer. These rectifiers conduct when the voltage across the primary is greater than twice the dc input voltage. The reactive energy stored in the inverter and load, which tends to increase the output voltage above $2V_i$, is dissipated in the 0.67-ohm resistors in series with the rectifiers.

Performance data were taken using a value of C_c of 4.6 microfarads and C_T of 72 microfarads. Conditions were identical with those in the second run of Test II. The efficiency of the transmitter (Fig. 27) at resonance is slightly above 70 percent. This is appreciably lower than efficiency measured without clipping (85 to 90 percent). Figures 28 and 29 show the commutation ratio and input resistance. Figure 30 shows that the peak-voltage ratio can be held to less than three over almost all of the frequency range of operation.

Figure 31 shows the transmitter waveforms.

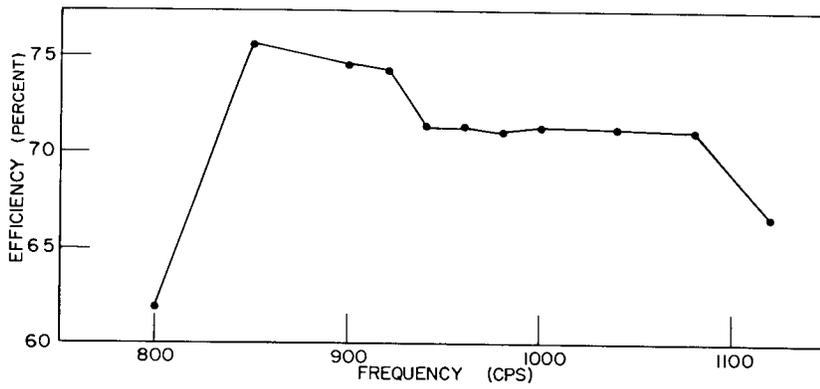


Fig. 27 - Measured transmitter efficiency with clipped output voltage; $C_c = 4.6$ microfarads, $C_T = 72$ microfarads

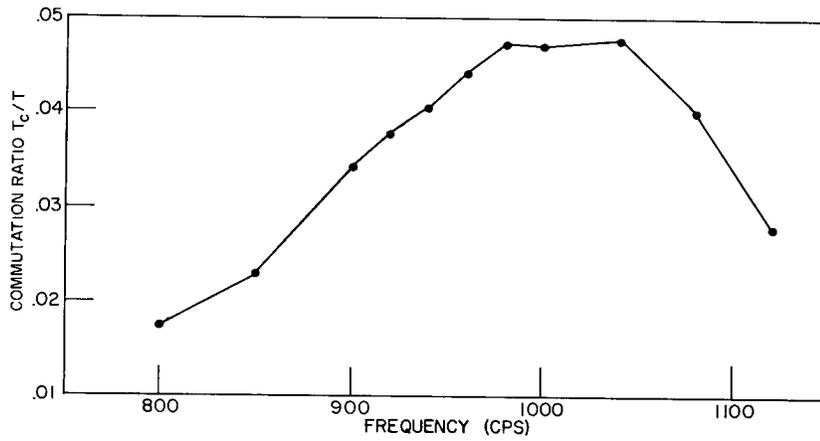


Fig. 28 - Measured commutation ratio of inverter with clipped output voltage

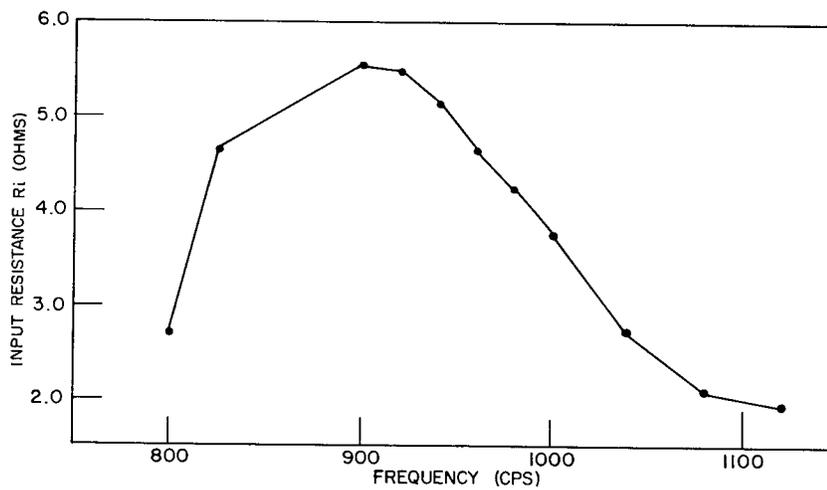


Fig. 29 - Measured inverter input resistance with clipped output voltage

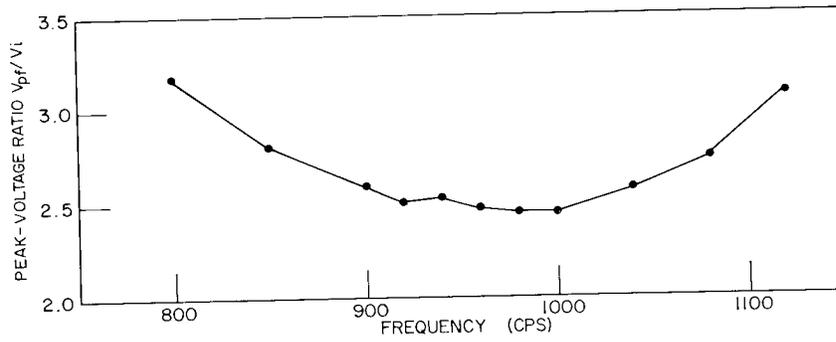


Fig. 30 - Measured value of peak-voltage ratio of inverter with clipped output voltage

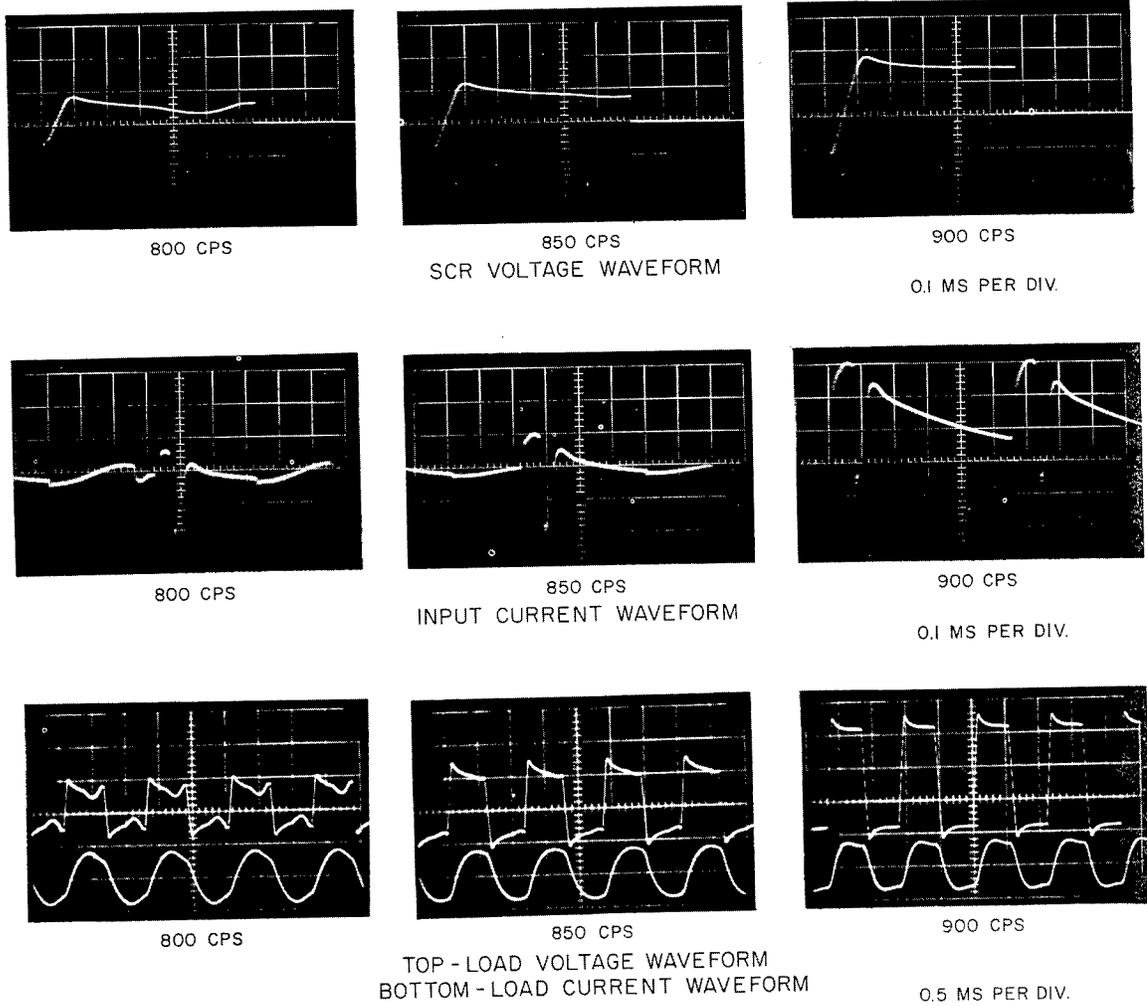


Fig. 31 - Inverter and load, voltage and current waveforms; clipped output voltage, $C_c = 4.6$ microfarads, $C_T = 72$ microfarads

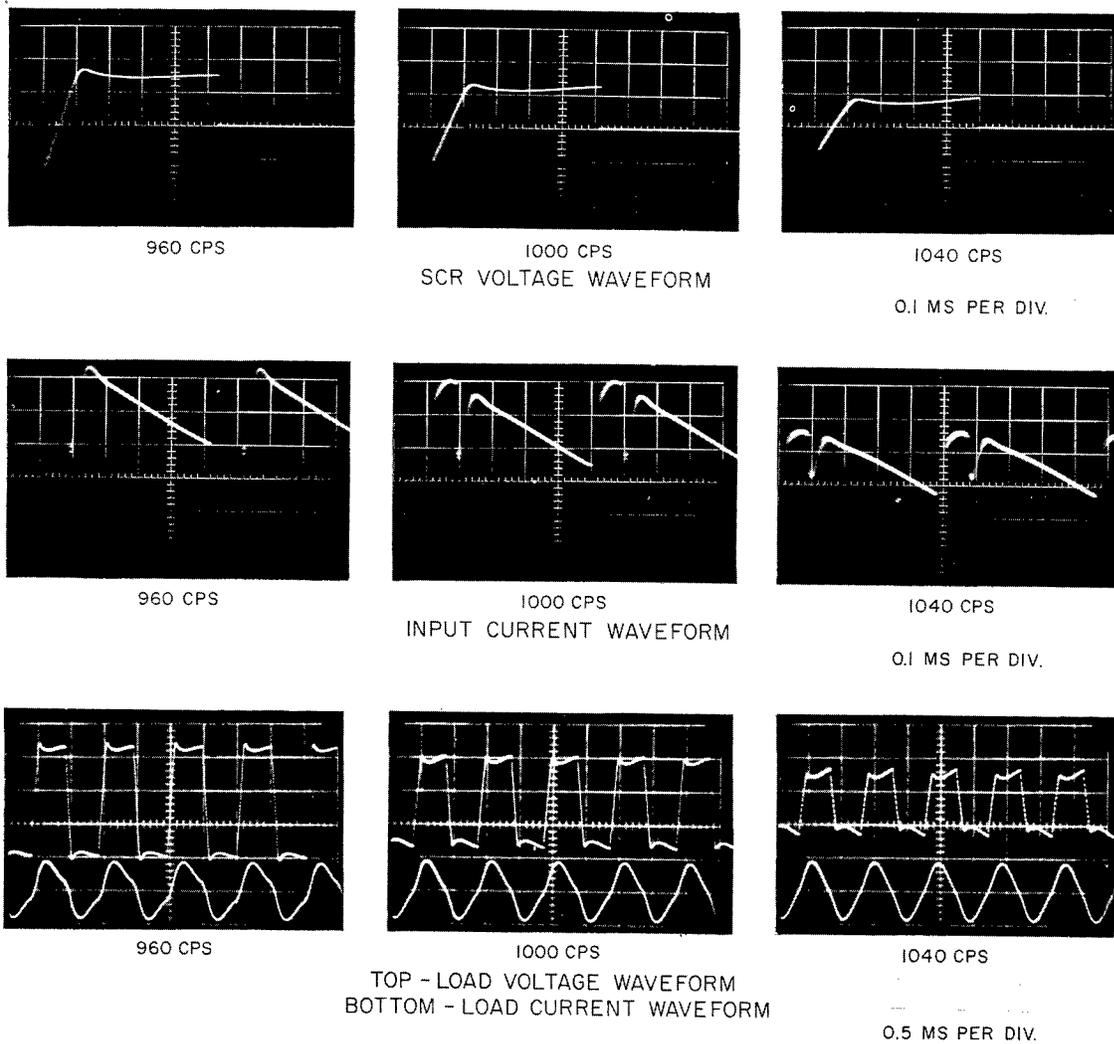


Fig. 31 (Continued) - Inverter and load, voltage and current waveforms; clipped output voltage, $C_c = 4.6$ microfarads, $C_T = 72$ microfarads

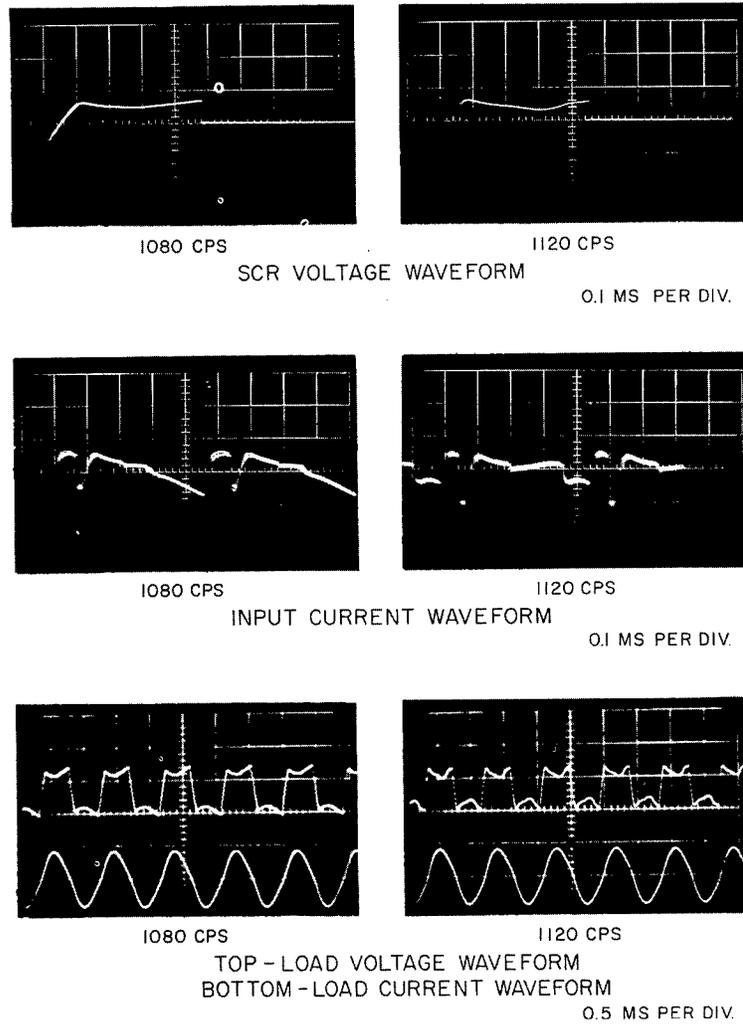


Fig. 31 (Continued) - Inverter and load, voltage and current waveforms; clipped output voltage, $C_c = 4.6$ microfarads, $C_T = 72$ microfarads

Acoustic Performance of the Projector Array

The acoustic performance of the projector array was of interest because it was anticipated that the distorted driving voltage from the transmitter might have an adverse effect. The acoustic pressure of radiated sound was measured for each frequency at 25 amperes rms driving current with both the inverter transmitter runs and linear-amplifier calibration runs. The acoustic pressure with the inverter transmitter drive averaged 0.3 decibel less than the acoustic pressure with the linear-amplifier drive. Most of this 0.3-decibel difference when using the inverter transmitter is due to the presence of third and fifth harmonic in the driving current, to which the projector array does not respond. No difference was noted in beam patterns obtained with the two different types of drives.

The signal received at the hydrophone was analyzed to determine its harmonic content. This was done using a crystal filter with a 50-cps bandwidth while driving the array at the resonant frequency of 960 cps at a level of 25 amperes. The level of the harmonics relative to the fundamental is listed in Table 2 for six combinations of load and inverter tuning, for the clipped-output operation, and for a linear-amplifier drive. The second-harmonic distortion is inherent in the variable-reluctance transducer, and its level is the same for both the linear amplifier and inverter drive. With the inverter drive, the third harmonic is from three to seven decibels higher than with the linear amplifier. This is due to the fact the inverter drive does have an appreciable third harmonic of the current, which may be seen in the photographs of the current waveforms. For all types of drives the fifth harmonic was more than 48 decibels below the fundamental.

Table 2
Harmonic Content of Acoustic Pressure at 960 cps and 25 Amperes
Driving Current (In Decibels Relative to Fundamental)

Transmitter and Tuning	Second Harmonic	Third Harmonic	Fifth Harmonic
Inverter $C_c = 3.1 \mu f$ $C_T = 72 \mu f$	-35.8	-37.4	Less than -48
Inverter $C_c = 4.6 \mu f$ $C_T = 72 \mu f$	-36.7	37.0	"
Inverter $C_c = 9.2 \mu f$ $C_T = 72 \mu f$	-37.1	-41.8	"
Inverter $C_c = 3.1 \mu f$ $C_T = 108 \mu f$	-37.9	-37.0	"
Inverter $C_c = 4.6 \mu f$ $C_T = 108 \mu f$	-38.5	-37.1	"
Inverter $C_c = 9.2 \mu f$ $C_T = 108 \mu f$	-37.2	-40.8	"
Inverter with clipped output $C_c = 4.6 \mu f$ $C_T = 108 \mu f$	-40.2	-36.1	"
Linear Amplifier	-36.7	-44.7	"

CONCLUSIONS

Tests of the transmitter verified that it could supply a high-power drive at efficiencies up to 90 percent. The maximum output power used in the test was slight over two kilowatts, which was one kilowatt less than the full rating of the transmitter. It should be noted that semiconductor components are presently available which could be used to build similar transmitters with ten times the output power as the one described in this report. The goal of testing was to investigate overall performance of the transmitter rather than to obtain maximum power. The maximum measured efficiency of the transmitter of 85 to 90 percent probably could not be significantly improved without greatly overspecifying the inverter components.

The output voltage from the transmitter contained a large amount of harmonic distortion, as may be seen in the waveform photographs. This did not appreciably degrade the acoustic performance of the projector, either in beam pattern or efficiency. The acoustic pressure radiated by the array did have a third-harmonic component of distortion, but this was 36 decibels below the fundamental at resonance. From the tests it appears the distorted output voltage from the transmitter does not limit its usefulness for driving variable-reluctance transducers.

During the testing there was no failure of operation of the transmitter. The starting and stopping circuit of the transmitter worked properly and should be adequate to operate the transmitter on a pulsed basis. It was noted during the testing that after starting about seven cycles were necessary for the transmitter to reach a steady state, due to the Q of the load. No information was obtained about the commutation time during this interval before a steady-state condition was reached. Although the transmitter did turn on, further investigation is desirable to determine how close to the minimum commutation time the circuit operates during the build up to steady state. An input current-sensing circuit in the transmitter protects the SCR's against excessive current by stopping the inversion process. It would be desirable to add a voltage-sensing circuit to provide similar protection against excessive output voltages.

The effect of the load impedance on the performance of the inverter circuit in the transmitter was investigated by using two values of series tuning (Tests I and II) and operating at discrete frequencies about resonance. The measured values of R_i , T_c/T , and V_{pf}/V_i are useful as purely experimental data because they show how the input current, commutation time, and output voltage vary with load impedance. A more important reason for taking this data was to compare the measured value of these quantities with calculated values using the ac model for the inverter and load. The plots of the measured and calculated values of these quantities as a function of frequency are similar in form. However, there is a difference in their absolute magnitudes. In Test I this difference between measured and calculated values was 10 to 20 percent, and in Test II 20 to 40 percent. For R_i the measured value was greater than the calculated value, and for V_{pf}/V_i the calculated value was greater than the measured value. For T_c/T the calculated value was larger than the measured value, except for frequencies above resonance. It appears that the model will give a good first approximation to the performance of the inverter. For a design based on it, it can be expected that the actual input current and output voltage will be less than the calculated value.

There are two ways in which the calculated values may be brought into closer agreement with the measured values. First, in calculating the input power (Eq. 6), instead of using the actual input voltage to the inverter V_i , a corrected value of V_i less the approximately constant voltage drop of the SCR's could be used. This is a small correction, except at low input voltage. It does tend to bring the calculated value of R_i and V_{pf}/V_i into closer agreement with the measured value. Second, in calculating V_{pf}/V_i and T_c/T , the third-harmonic term could be included in addition to the fundamental term.

This is particularly important for frequencies above resonance, where the impedance of the fundamental $|Z_1|$ is about the same magnitude as the third-harmonic impedance $|Z_3|$. This is probably the main source of error in the calculated value of T_c/T at these frequencies.

In Test III the transmitter was operated with a clipped output voltage. This type of operation provides the transmitter with voltage regulation with respect to load variation. It is achieved at the expense of transmitter efficiency. Whether this mode of operation is desirable depends on the relative value of voltage regulation compared to efficiency.

APPENDIX A

CALIBRATION OF PROJECTOR ARRAY

An array consisting of 36 variable-reluctance push-pull transducers was supplied by the Transducer Branch, Sound Division, U. S. Naval Research Laboratory. The frame, junction box, and polarizing supply were designed by John Chervenak of that branch. For the purpose of establishing its electrical and acoustic characteristics, the array was calibrated with a sinusoidal driving voltage from a linear amplifier. These measurements were made Oct. 25 and 26, 1962, at the U. S. Navy Electronics Laboratory Pend Oreille Calibration Station.

Figure A1 shows the 36 transducer elements installed in a frame with a junction box mounted on top of the frame. For the test described in this report, all the elements were arranged in a single plane in the center of the array and driven electrically in phase.

The electrical connection of the transducer elements is shown in Fig. A2. All 36 elements are in parallel for the ac driving voltage and the dc polarizing voltage. Total polarizing current for the array was 340 amperes. The capacitors designated $C_T/2$ are used for both blocking dc voltage and improving the power factor of the ac circuit. Meters v , A , and w measure volts, amperes, and watts delivered by the source.

After taking into account the reactive drop due to the capacitors $C_T/2$, the impedance of the array can be calculated from the meter readings. For an ac driving current of 25 amperes, the calculated values of magnitude of array impedance $|Z|_A$ and phase ϕ_A are plotted in Fig. A3, and the real and imaginary parts, R_A and X_A , in Fig. A4. Both plots indicate that there are one or possibly two spurious resonances at frequencies slightly above the resonance of the array of about 960 cps. From data taken at higher frequencies, the clamped inductance of the array was calculated to be about 400 microhenries.

Figure A5 is a beam pattern taken at 960 cps and a driving current of 25 amperes. Directivity factor is 0.1.

Figure A6 shows the measured acoustic pressure at zero degrees and calculated acoustic efficiency for frequencies near resonance with 25 amperes of driving current. Both pressure and efficiency peak at 960 cps.

Figure A7 is a continuous record of the acoustic pressure at zero degrees as a function of frequency from 500 to 5000 cps at constant driving currents of 1.0, 5.0 and 15.8 amperes. There exists a sharp dip in these curves at 3100 cps.

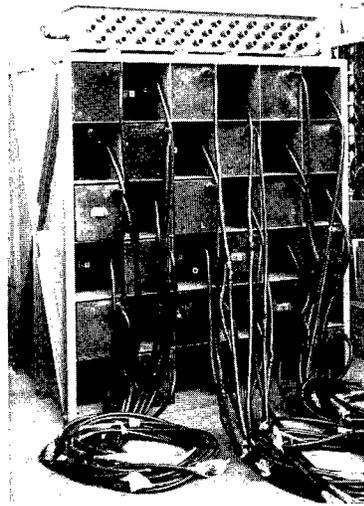


Fig. A1 - Projector array

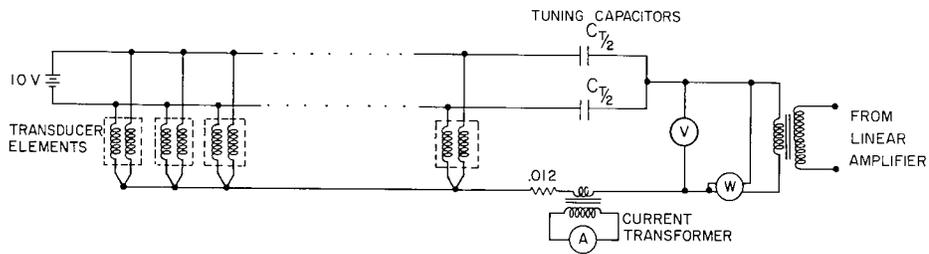


Fig. A2 - Electrical connection of projector array

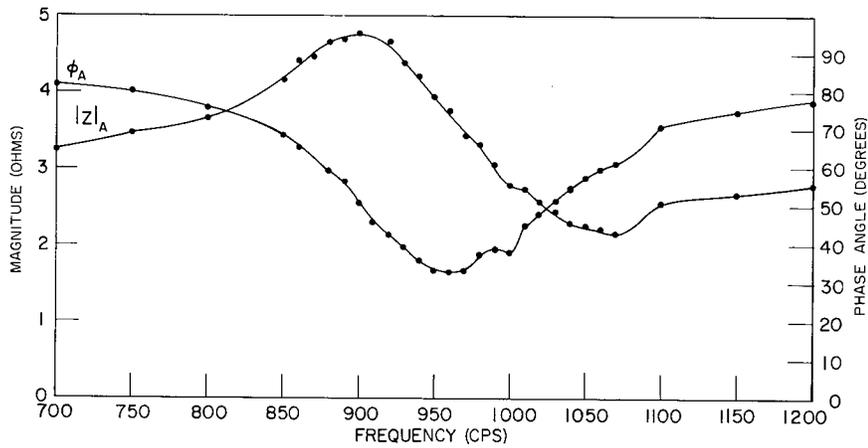


Fig. A3 - Electrical impedance of array, magnitude and phase (measured at 25 amperes)

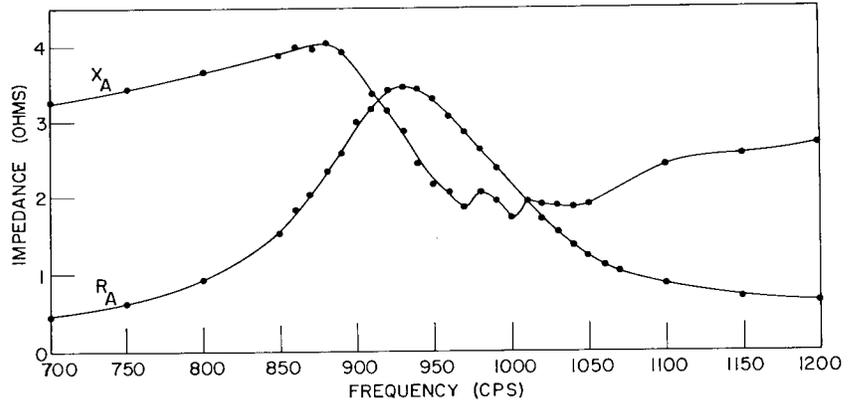


Fig. A4 - Electrical impedance of array, real and imaginary parts (measured at 25 amperes)

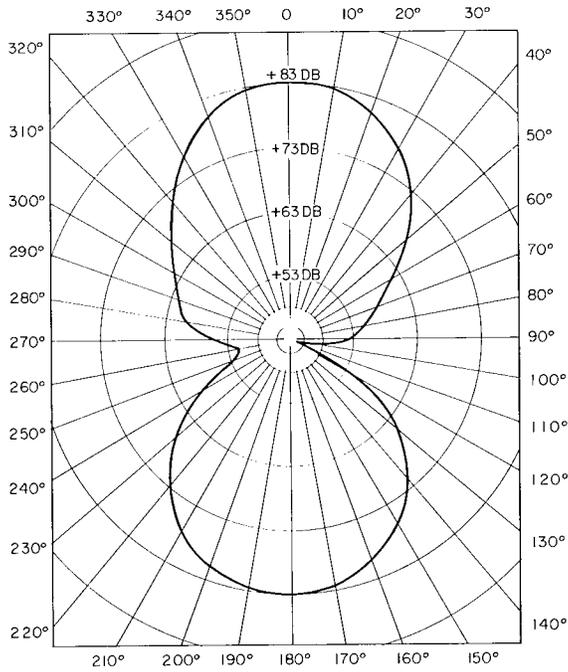


Fig. A5 - Array beam pattern at 960 cps with 25 amperes driving current. Acoustic pressure is in decibels above one microbar per ampere at one meter.

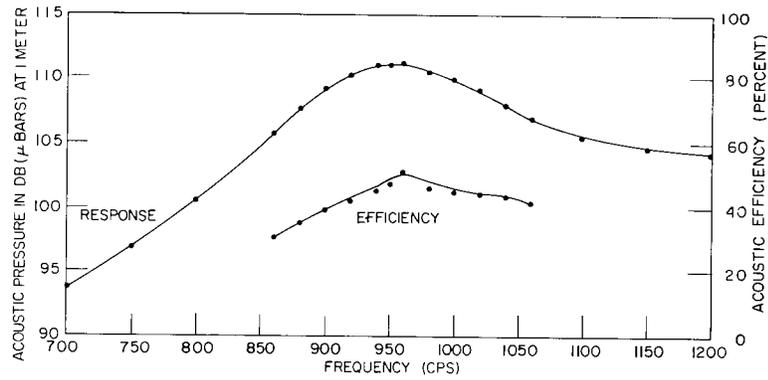


Fig. A6 - Array response and acoustic efficiency at discrete frequencies and 25 amperes driving current. Acoustic pressure is in decibels above one microbar at one meter.

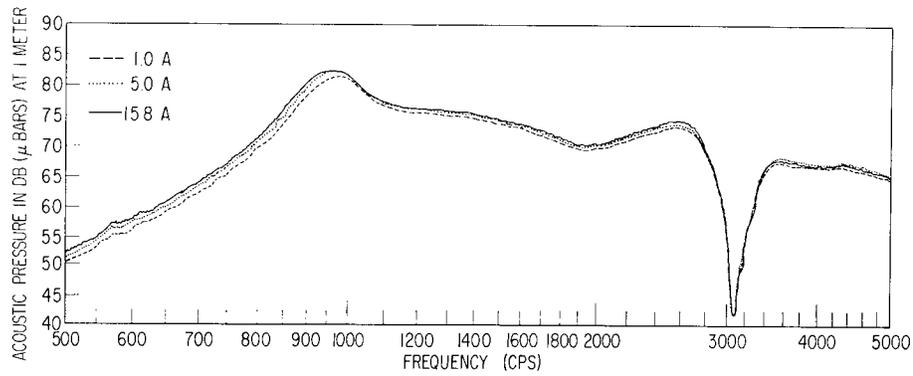


Fig. A7 - Array response at frequencies from 500 to 5000 cps with driving current of 1.0, 5.0, and 15.8 amperes. Acoustic pressure in decibels above one microbar per ampere at one meter.