NRL Report 7572

Standard Digital Data Clock-Rate Generator With Programmable Digital Phase Shift

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June 29, 1973

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ABSTRACT

To perform research and development of satellite-communications circuits, subsystems, and system concepts, a device was designed to generate standard digital data clock rates and to provide continuous, programmable digital phase-shift control to permit synchronization of the output signal to other system signals. This equipment provides data clock rates of 38,400, 19,200, 9600, 4800, 2400, 1200, 600, 300, 150, 75, and 37.5 Hz based on a 1-MHz input signal from a frequency standard.

PROBLEM STATUS

Final report on one phase of a continuing NRL problem.

AUTHORIZATION

NRL Problem R01-34
Project RF21-222-401-4353

Manuscript submitted March 7, 1973.

STANDARD DIGITAL DATA CLOCK-RATE GENERATOR WITH PROGRAMMABLE DIGITAL PHASE SHIFT

INTRODUCTION

To develop and prove satellite communication concepts and designs, a digital data clock-rate signal generator was designed and constructed. The basic requirements were that the generator provide standard data rates, have the stability of a controlling frequency standard, and have a phase shift controllable over the full 360° range. This data clock-rate generator should be useful to any communication group designing or testing digital baseband equipments and modems (modulation-demodulation equipments).

In addition the use of a control device which generates digital data clock rates of 38,400, 19,200, 9600, 4800, 2400, 1200, 600, 300, 150, and 75 bits per second (bps) from a 1-MHz frequency standard would enhance digital communication systems. With this inherent stability, the circuit could be interrupted for short periods of time, as determined by the stability of the frequency standard and changes in propagation path (i.e., satellite range), without loss of synchronization. For example, a satellite circuit using a 1,200 bps data stream would allow a range change of about 62.5 km for a phase shift of about 1/4 of a data bit. The range to a near-synchronous spacecraft from a stationary platform would stay within this range limitation for many minutes, and the range from a fast-moving platform would stay within this range limitation for a minute or more. To make such a concept practical requires that frequency standards be used as the basic timing clock for the data. Use of this digital generator controlled by a precise clock allows synchronization and multiplexing techniques previously not practical. Phase shifting of the clock signal supplied by the frequency standard is necessary for initial bit synchronization, for elimination of the phase differences of the reference frequency standard, and for circuit-delay changes. The correction due to frequency differences between the frequency standards at the transmitter and receiver will be very small. Frequency-standard accuracies of better than 10^{-9} parts/day should become quite available to operational communications in the near future. A 2,400-bps data stream would drift about 0.21 part of a bit in one day of operation with a frequency difference between the receiver and transmitter frequency standards of 10^{-9} parts/day. The variations of data rate introduced by doppler shift are insignificant. Thus the phase shifting of the clock signal would be principally used for tracking and reducing toward zero the effects of range change from the terminal to the satellite. This report describes an experimental data-rate clock generator developed for the application just described.

GENERATION OF DIGITAL DATA CLOCK RATES

There are several methods of generating digital data clock rates. One method, if a crystal-oscillator frequency standard is used, is to multiply or divide the oscillator frequency to provide harmonics or subharmonics and then to combine the frequencies to obtain a frequency which could be successively divided by two to provide the required data clock rates. The principal disadvantage of this method is the filter implementation. Relatively bulky components are required and lower reliability is obtained than from an all-digital

system. A second method of obtaining the data clock rates is to directly provide a frequency which could be simply divided digitally. This requires the use of a nonstandard-frequency crystal, with its attendant increased cost, to obtain the frequency stability associated with frequency standards. The clock generator described in this report uses digital techniques and is related to the ratio counter or variable binary scaler (1, 2). However, the logic design presented here is more straightforward and thereby leads to a simple implementation.

Phase shifting of waveforms can be accomplished in several ways; however, some have serious shortcomings for this application. For example, a selsyn, RC network, and amplifier combination (3) provides continuous 360° phase shift, but is unsatisfactory because a reversing motor must be used for simple searching control, the selsyn is bulky, and the input to the phase shifter must be a sine wave. Other analog methods of phase shifting use bulky components (transformers) and lack sufficient range, although they are quite adequate for special-purpose use. Two digital methods of programmable phase shifting, described in recent publications (4, 5), lack continuous control. These phase shifters can shift the data clock waveform; however, the one described in Ref. 4 has a break in control at 180° and other is not reversible. The phase-shift method used in the NRL digital data clock-rate generator provides continuous, bidirectional phase shift of the clock waveforms (in discrete steps) from 0° to 360°. The phase shifting is done digitally using the same types of integrated circuits as those used for generating the data clock rates.

DIGITAL DATA CLOCK-RATE GENERATOR

The basis for the method of generating the required clock rates is to remove one of every 25 pulses from a square-wave pulse train obtained from the square-wave output of a 1-MHz frequency standard. The resulting pulse train, averaging 960 kHz, is divided by 25 to provide a pulse train averaging 38,400 kHz. Since this quotient is not a multiple of two, the resulting pulse train is asymetric, but the positive-going (or negative-going) transitions occur at regular intervals and are defined as the clock pulses. A symmetric 38,400-pps output can be derived from the output of the N/25 divider by passing the asymmetrical output of the divider through a one-shot multivibrator to restore symmetry. A minor residual jitter remains, due to this basic technique of generating the 960,000-pps pulse train. The 38,400-pps train is divided by two to obtain a symmetric square-wave 19,200-pps pulse train; further divide-by-two stages generate square waves at the lower bit rates. All pulse streams of 19,200 pps or less can be used as alternate 1,0 generators. For this reason, a pulse stream of 37.5 pps was included to provide a digital alternate 1,0 stream of 75 bps. In addition, a 38,400-pps alternate 1,0 generator is provided by creating approximately-13-μs pulses triggered by the negative-going transitions of the asymetric 38,400-pps pulse train. Figure 1 is a block diagram of the divider. This generator develops the required clock bit rates but does not contain the phase shifter; the generator normally would be used on the transmitting end of the circuit. Figure 2 shows the resulting waveforms which depict the removal of one of every 25 input pulses from the 1-MHz input.

As can be seen in Fig. 2, division of 1 MHz by 25 yields a 40-kHz pulse rate, which has a 25-μs period (labeled $\overline{N/5 \cdot N/25}$). The 40-kHz pulses, when NANDed with the 1-MHz input signal, removes pulses from the 1-MHz input signal and results in the average-960-kHz waveform shown in which one out of every 24 pulses is 1 μs wider than the other pulses. The average period then is 1.04166 ... μs, which is obtained by averaging

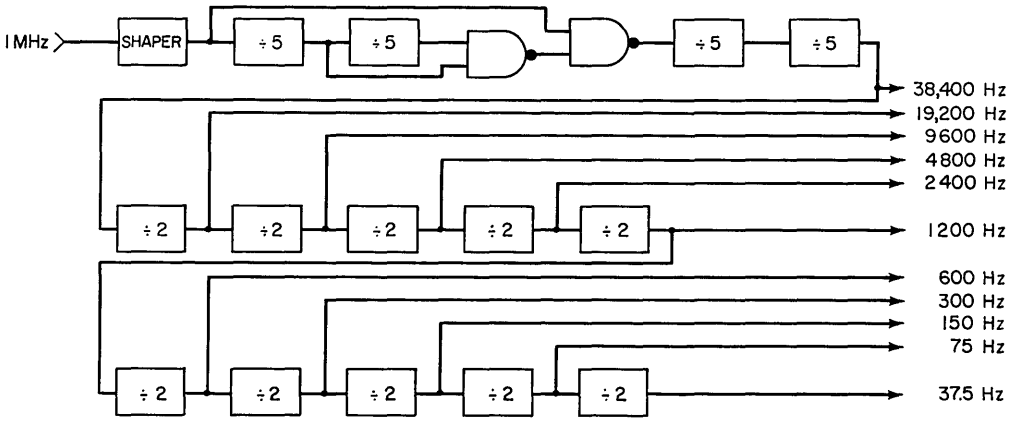


Fig. 1 — Digital data clock generator

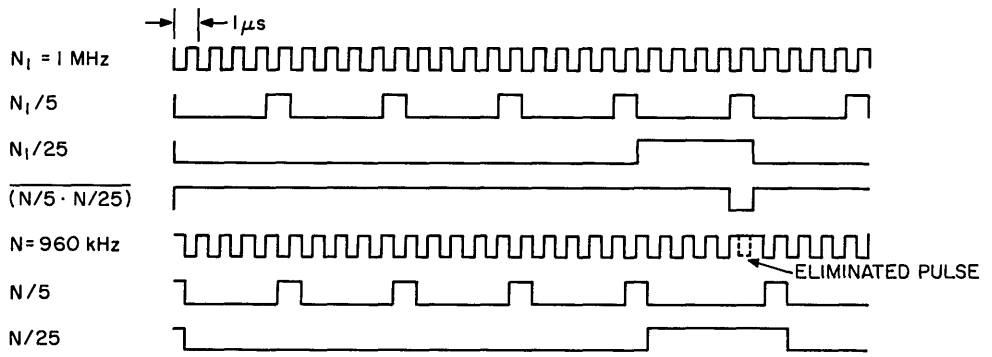


Fig. 2 — Generation of 960 kHz

23 1-μs periods and one 2-μs period. In other words, for every 25 1-μs input periods, we get 24 output periods, the first 23 of which are 1 μs in length and the 24th is 2 μs in length. Thus

$$nt_i = (n - 1)\, t_0,$$

where n is the number of input periods, t_i is the input-period length, and t_0 is the average output-period length. Rewriting, we have

$$t_0 = \left(\frac{n}{n-1}\right) t_i.$$

The average frequency, 960 kHz, is the reciprocal of the average period.

The generation of the required bit rates from the 960-kHz signal depends on successive division and an averaging of the output pulse. The 960-kHz input signal to the $N/25$ divider contains cyclic repetitions 25 μs long comprising 23 1-μs increments and one 2-μs increment. Each of these cycles therefore contains one pulse which is 1 μs wider than the others. Normally the $N/25$ divider puts out a pulse every 26 μs, except when the wide input pulse occurs. Figure 3a shows the 1-μs slippage for two output cycles. On the 24th input cycle, two wide pulses occur, as shown in Fig. 3b, and the output sequence period is lengthened by 1 μs. The result therefore is an averaging process in which there are 23

Table 1
Average Bit Length and Peak-to-Peak Jitter for Each Data Clock Rate

Clock Rate (Hz)	Short Period		Long Period		Average Period Length (μs)	Jitter from the Average Period Length (ns)
	No.	Length (μs)	No.	Length (μs)		
38,400	23	26	1	27	26.0416...	+41.67, −958.33
19,200	23	26	1	27	52.0833...	+20.83, −479.16
9600	11	52	1	53	104.1666...	+10.41, −239.58
4800	5	104	1	105	208.3333...	+5.20, −119.79
2400	2	208	1	209	416.6666...	+2.10, −59.89
1200	1	416	2	417	833.3333...	+1.05, −29.95
600	2	833	1	834	1666.6666...	+0.52, −14.97
300	1	1666	2	1667	3333.3333...	+0.26, −7.49
150	2	3333	1	3334	6666.6666...	+0.13, −3.74
75	1	6666	2	6667	13,333.3333...	+0.06, −1.87
37.5	2	13,333	1	13,334	26,666.6666...	+0.03, −0.94

26-μs periods and one 27-μs period. Equation (1) does not apply in this case because the input periods are no longer equal increments of time; i.e., we now have a number of equal-increment input periods coupled with one period exactly 1 μs longer than the other periods to form one input frame. In this case it is easy to average if the concept of a frame is introduced. Here a frame contains 23 periods of 26 μs duration and one period of 27 μs duration. In this case we can write

$$nt_{avg} = nt_0 + 1\ \mu s$$

or

$$t_{avg} = t_0 + \frac{1}{n}, \tag{2}$$

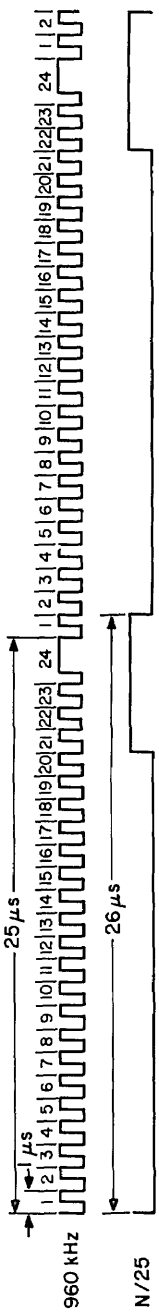
where t_{avg} is the average clock period,in microseconds, t_0 is the smallest output-period increment (26 μs), and n is the number of increments (24). From Eq. (2) the average period length is 26.04166. . . μs, where t_0 is 26 μs and n is 24. This average period provides the required 38,400 Hz.

The clock rates following the N/25 divider are generated by successive divide-by-two stages. These output clock rates are also averages, and each average follows Eq. (2), except for those cases in which the longer period outweighs the shorter period. This occurs at the output clock rate of 1200 Hz. At this time, the 2400-Hz input signal contains two short periods and one period that is 1 μs longer. Since we are dividing by two, six input periods are required to generate three output periods. This has the effect on the output period of forcing one short period and two periods each 1 μs longer than the short period instead of the reverse situation on the input. When we write the formula for this average, we obtain

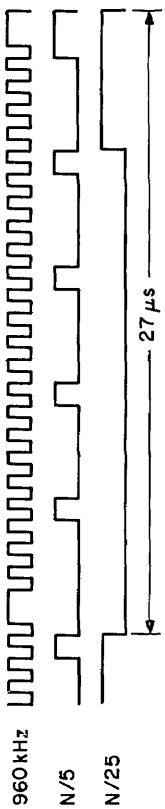
$$nt_{avg} = nt_0 + 2\ \mu s$$

or

$$t_{avg} = t_0 + \frac{2}{n}, \tag{3}$$



(a) Slippage of the wide pulse in the 360-kHz input signal with respect to the $N/25$ output



(b) Generation of the extra-length output cycle of the 38.4-kHz waveform

Fig. 3 — Waveforms of 960 kHz divided by 25

where t_{avg} is the average clock period in microseconds, t_0 is the smallest output period increment, and n is the number of increments in the period. The situation alternates on each successive division by two, as can be seen in Fig. 4. Therefore, Eq. (2) applies at every other clock rate starting with 2400 Hz, and Eq. (3) applies at every other clock rate starting with 1200 Hz. Equation (2) also applies at all clock rates from 38,400 down to 2400 Hz.

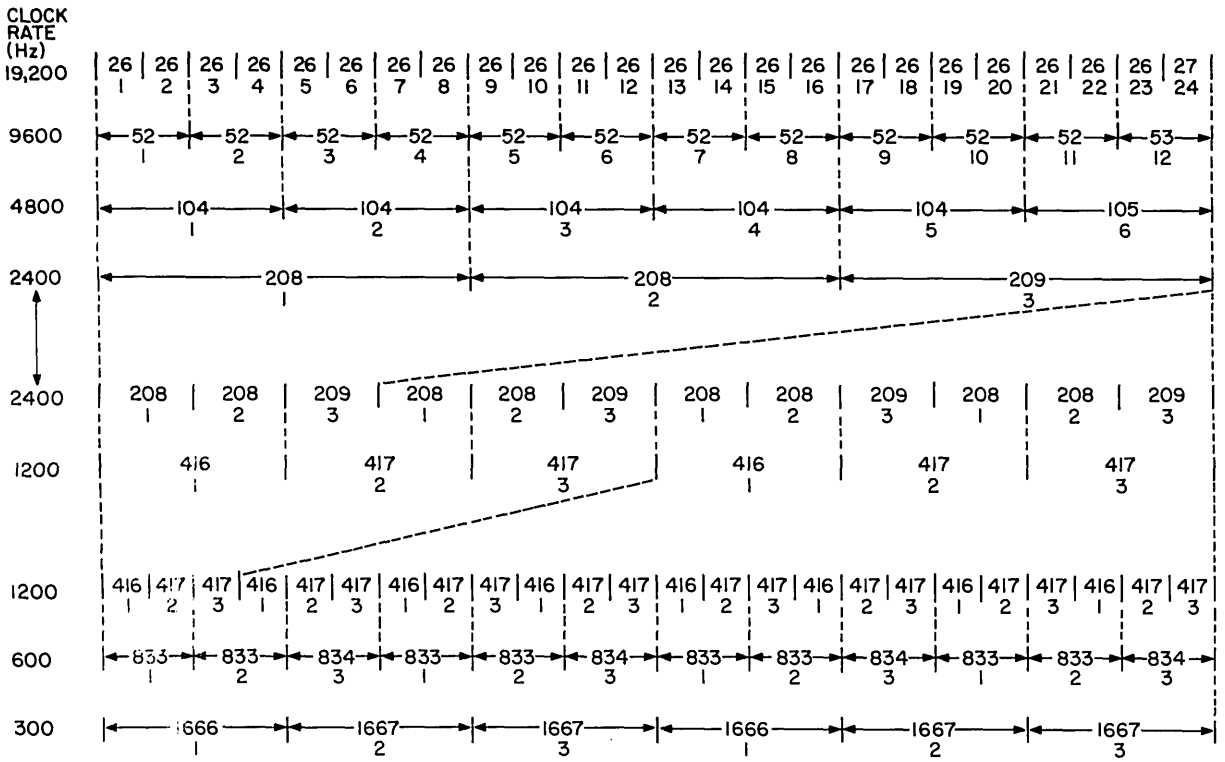


Fig. 4 — Period lengths for successive divisions

The peak-to-peak jitter of 1 μs occurs because of the 1-μs difference between pulses in the output bit stream. The 1-μs difference occurs periodically, as shown in Table 1. The jitter presented in Table 1 is the jitter plus and minus from the average period length. A method of envisioning this effect is shown in Fig. 5 for the 19,200-Hz case. The phase reference is arbitrarily chosen to be zero at the end of the 24th interval. This shows that the output lags the reference by 23 X 0.04166. . . μs at the 23rd interval and then is corrected on the 24th interval. The reason for this is that the true period desired is 26.0416. . . μs but the first 23 output increments are each 26 μs long. This leads to an error of 0.95833. . . μs on the 23rd increment; however, the 24th increment corrects by 1 μs, which includes the 0.95833. . . μs plus the correction of 0.04166. . . μs for the 24th interval. Thus there is a peak-to-peak jitter of 1 μs. Table 1 shows the jitter from the average in nanoseconds for each bit rate.

PHASE SHIFTER

In general the receiver must generate a digital clock signal that can be matched to the crossovers or midpoint of the bits in the received digital stream. This requires that a means exist to phase shift the clock generator used with the receiver. The technique used

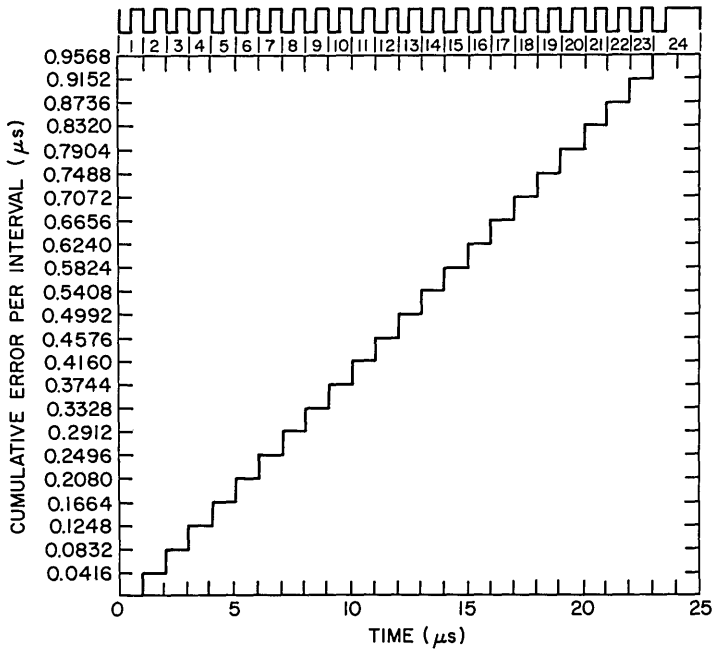


Fig. 5 — Cumulative error for 19,200 Hz

to phase shift is to change the fixed N/25 divider which divides the 960-kHz signal to a programmable divider, with N/25 being the steady or reference state. If the division ratio at the end of an output pulse is changed for one output-pulse period to N/24 and then restored to the N/25 ratio, the result is a bit stream which leads in phase with respect to the reference waveform. A similar phenomena occurs if the division ratio is set to N/26 for one period and is then restored to N/25. The result in this latter case is a bit stream lagging in phase with respect to the reference waveform. Figure 6 shows the reference, leading phase shift, and lagging phase shift. The means of controlling the phase shift as depicted in Fig. 6 is shown in the logic diagram of the digital phase shifter (Fig. 7). The waveforms associated with the digital phase shifter are shown in Fig. 8. This phase shifter includes a digital phase-shift-direction control and step control, as well as the programmable *N*/25 divider. Phase-shift direction (selection of the 24 or 26 divisor) is determined by a logic 0 or 1 to gate B1. The shift of divisor to 24 or 26 is activated with a pulse input to gate B2. Each pulse causes a single step in the phase of the data clock waveforms. Slewing is accomplished by providing a continuous series of pulses to gate B2. Control of the division of the 960 kHz by 24, 25, or 26 is done by three two-input AND gates, A1, A2, and A3. The binary numbers to be detected by these AND gates are given in Table 2. The first two bits (11) are common to all three division ratios, so the single two-input AND gate which detects 24 (labeled A1) can be used in the detection of 25 and 26. The output of the AND gate which detects 24 therefore serves as one input to each of the two other AND gates that detect 25 and 26. The middle bit in all three binary numbers is zero; hence, it need not be detected.

Once detection of the binary numbers has been accomplished, some means of control must be exerted to select which of the numbers is to be used for feedback to reset the counter. A triple two-input AND-OR-INVERT (AOI) gate, controlled by flip flops (FF's) C1 and C2 and gate A4, is used. Each of the detected binary numbers serves as one input to each of the three AND gates in the AOI gate, and the second input to each

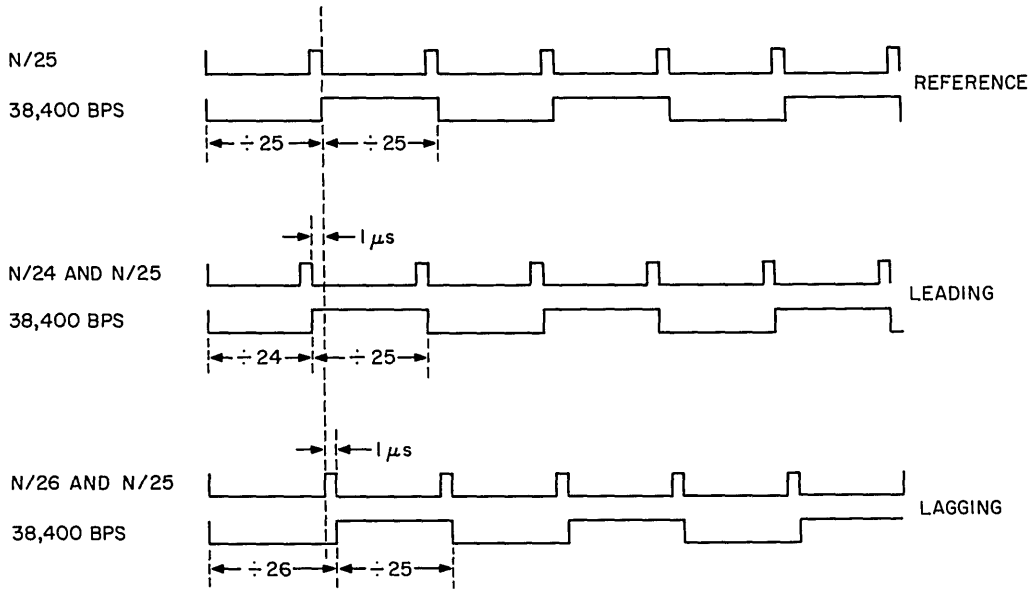


Fig. 6 — Examples of leading and lagging phase shift with respect to the reference

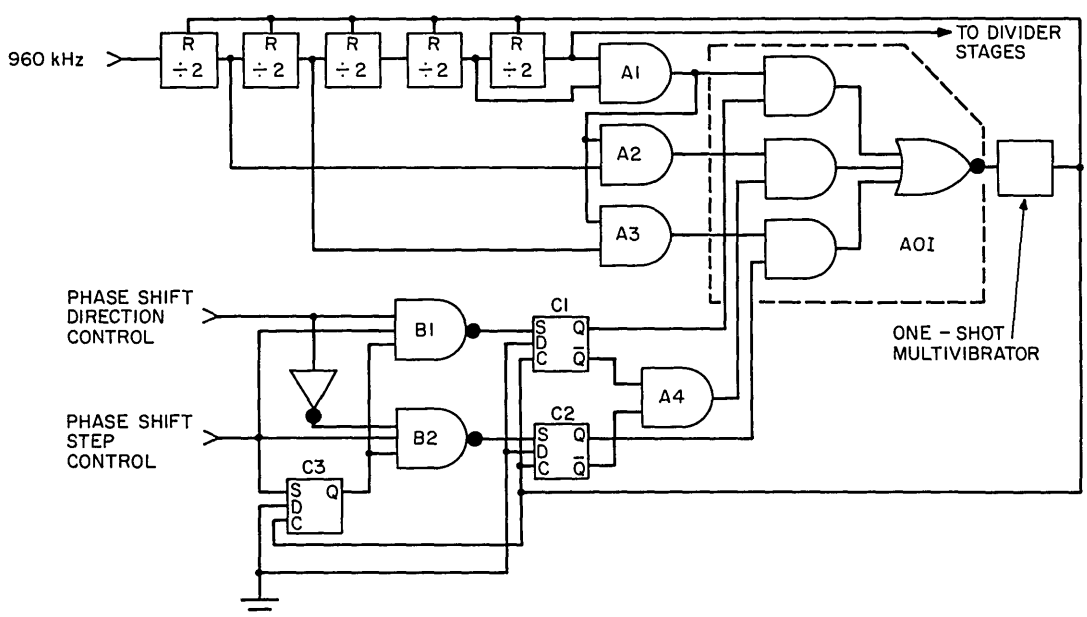


Fig. 7 — Phase shifter logic diagram

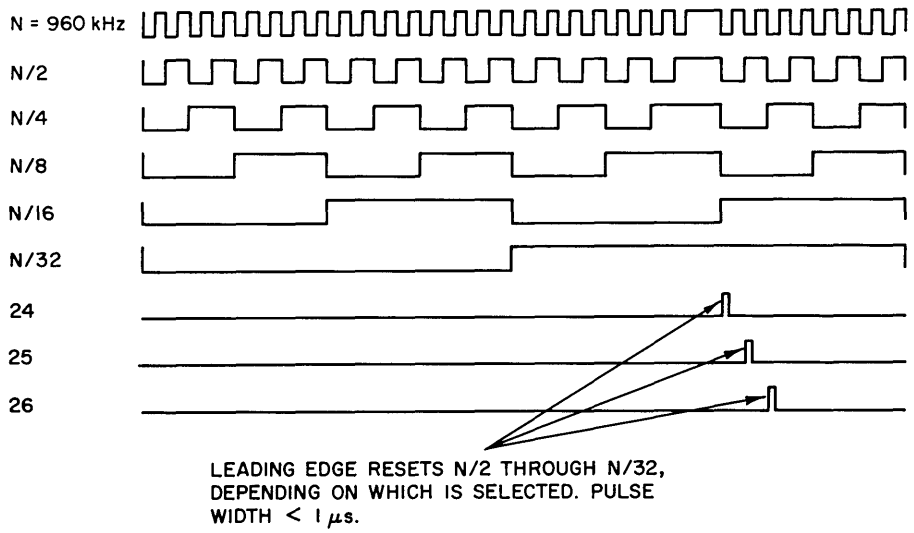


Fig. 8 — Programmable divider inputs and outputs

Table 2
Counter Control

Gate	Number	Binary Equivalent
A1	24	11000
A2	25	11001
A3	26	11010

gate determines which pulse is to be used to reset the counter. Whichever pulse happens to be selected, the one-shot multivibrator acts on the leading edge of the input pulse and puts out a 40-ns reset pulse to the counter; the counter is reset on the leading edge of this pulse.

To control the feedback selection, two FF's (C1 and C2) must be used which maintain the normal state of $N/25$ unless otherwise activated. The type of FF chosen was the data ("D" type) FF, which responds according to the truth table shown in Table 3, where Q_n is the present state and Q_{n+1} represents the new output state after a clock pulse. The preset terminal (marked S in Fig. 7) overrides the action of the truth table and sets the "D" FF to a logic 1 when a logic 0 is applied. The normal state of the "D" FF's in

Table 3
Truth Table for a "D" Flip Flop

D	Q_n	Q_{n+1}
0	1	0
1	0	1

this case is the reset state, so the ANDing of the two $\overline{Q}$ states by A4 is used to control the N/25 feedback mode. Now if N/24 is selected by setting C1, $\overline{Q}$ goes to a logic 0, which shuts off A4. Similarly, if N/26 is selected by setting C2, $\overline{Q}$ goes to a logic 0, which also shuts off A4. After the selected division is accomplished, the pulse from the one-shot multivibrator resets both of the "D" FF's, and the N/25 mode is restored when A4 goes to a logic 1.

Control of the phase-shift direction and rate is accomplished by two three-input NAND gates, B1 and B2, one inverter, and a single "D" FF, C3. The NAND gate responds according to the truth table shown in Table 4.

Table 4
Truth Table for a
Three-Input NAND Gate

INPUT	A	0101	0101
	B	0011	0011
	C	0000	1111
OUTPUT	F	1111	1110

The phase-shift direction is controlled by a logic 0 or 1. A 0 commands lagging phase shift (N/26) and a 1 commands leading phase shift (N/24). The inverter simply insures that if one direction is selected, the other is deactivated.

The phase-shift rate is controlled by a pulse input. A single pulse steps the data clock by 1 μs in relation to the reference. The input pulse is one input to B1 and B2 and also sets a "D" FF, C3, whose Q output is a second input to B1 and B2. (The third input to B1 and B2 is the phase-shift-direction control level.) This pulse sets either C1 or C2; it is only allowed through the NAND gates because of C3. After the shortened (or lengthened) counting sequence has been completed, the pulse from the one-shot multivibrator which resets the counter also resets C1, C2, and C3, the phase-shift-control FF. No further phase shift can occur unless another pulse appears at the rate-control input. The reason for C3 on the rate-control input is to make certain that no noise or extraneous pulses get through the NAND gates and enable the phase shifter when such action is not desired.

A normal phase-shift step would occur only in 1-μs increments; however, it is possible under the right conditions to have a 2-μs step. There is only one possibility for the case of leading or lagging phase shift. This occurs because the 960-kHz input signal contains a pulse which is 1 μs wider than normal. It was shown in the discussion of the data clock generator that this double-width pulse had a 1-μs slippage in relation to the output waveform of the N/25 divider. This slippage places two double-width pulses in the N/25 output period and causes the output period to increase from 26 μs to 27 μs. If we start the leading phase shift (N/24 division ratio) count at the right time, the double-width pulse will cause the binary number 24 to be detected 2 μs earlier than 25. This case is shown in Fig. 9. A similar phenomena can occur for the case of lagging phase shift when two double pulses occur during the N/26 period but only one double pulse occurs during the N/25 period. This is shown in Fig. 10. This jump of 2 μs instead of 1 μs should not be of any large consequence, since each step is a small part of a bit.

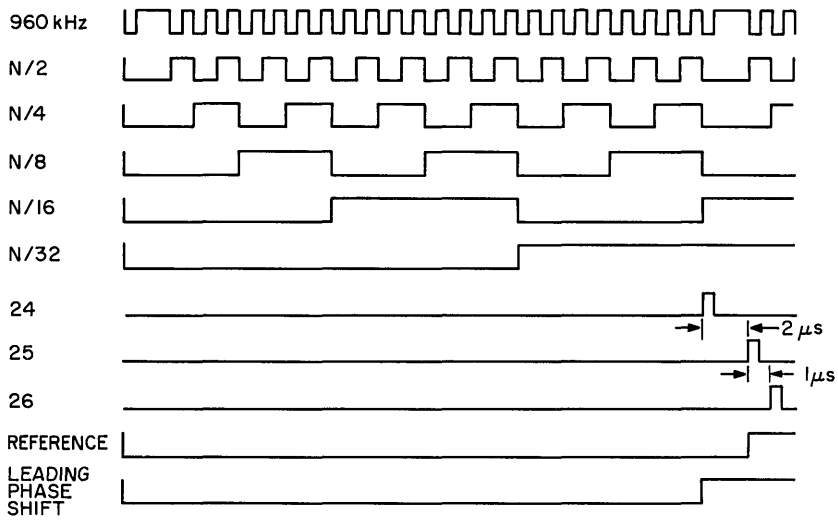


Fig. 9 — Conditions leading to double phase-shift step for the case of leading phase shift

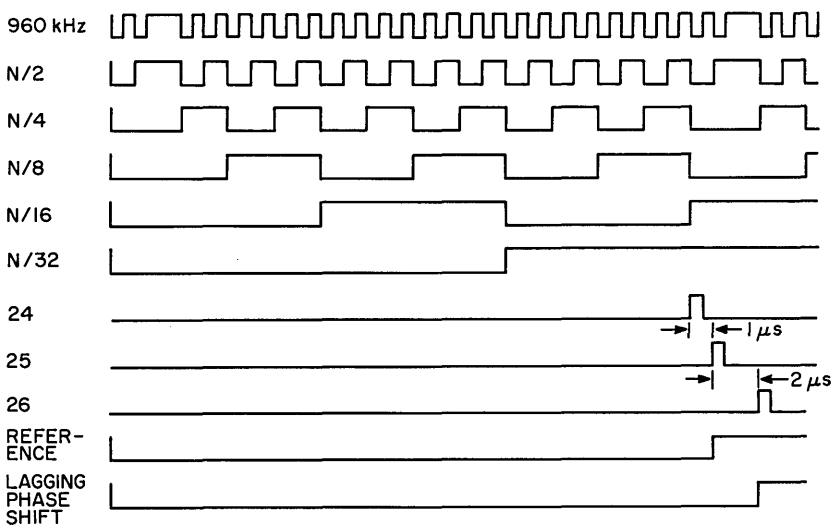


Fig. 10 — Conditions leading to double phase-shift step for the case of lagging phase shift

PERFORMANCE

A data clock generator and a data clock generator with phase shifter were built and tested. Both gave good performance and operated as previously described. Figures 11—13 are photographs of the data clock generator with phase shifter. The data clock generator without the phase shifter is virtually identical except for the reduced count of integrated-circuit packages.

As shown in Figs. 11—13, the implementation of this circuit was accomplished using dual-in-line-plastic (DIP) integrated-circuit (IC) packages. The types chosen were the Texas Instruments SN 7400 series DIP's, which were readily available. Figure 14 is the circuit

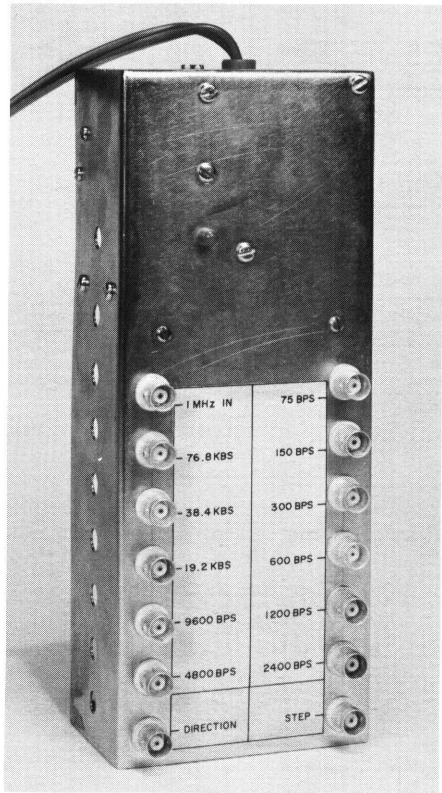


Fig. 11 — Front view of the data clock generator with phase shifter

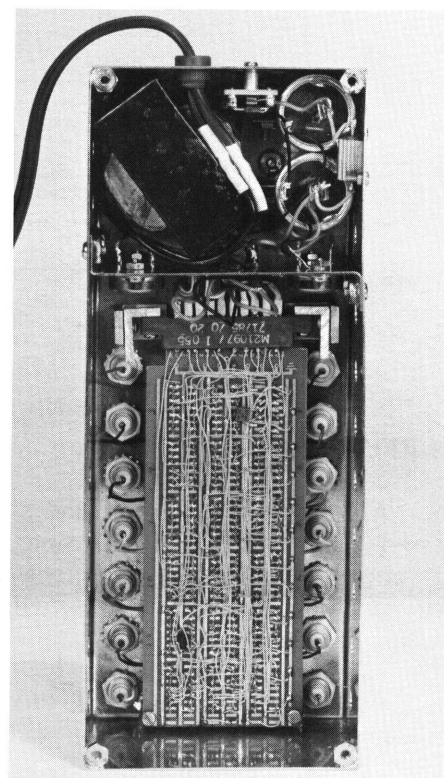


Fig. 12 — Interior view of the data clock generator with phase shifter and power supply

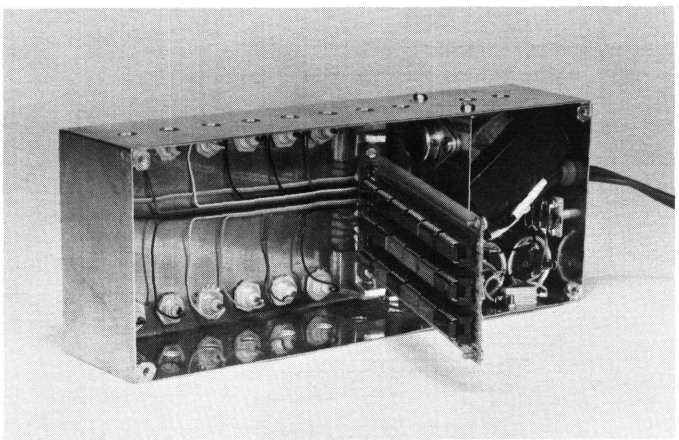


Fig. 13 — Interior view of the data clock generator with phase shifter, with the printed-circuit board exposed

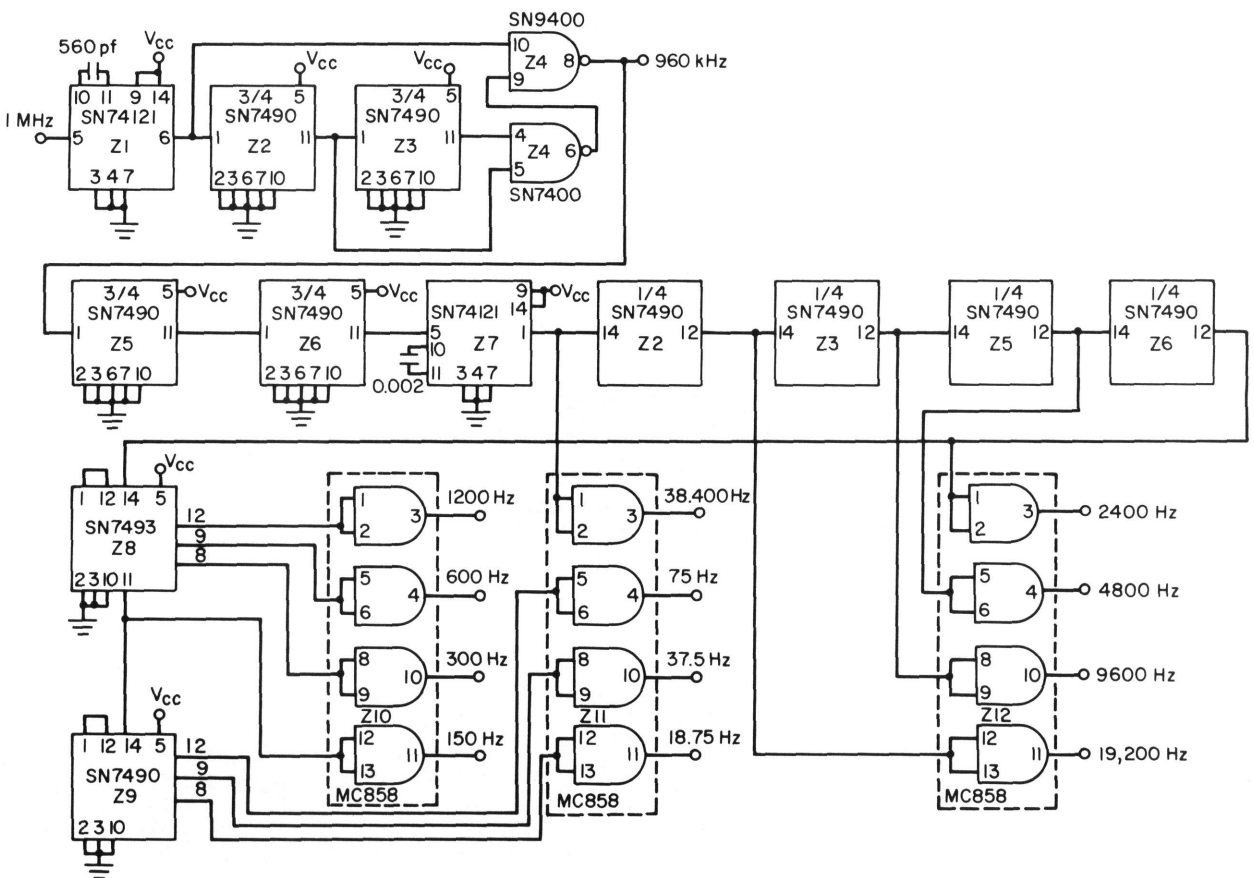


Fig. 14 — Data clock generator

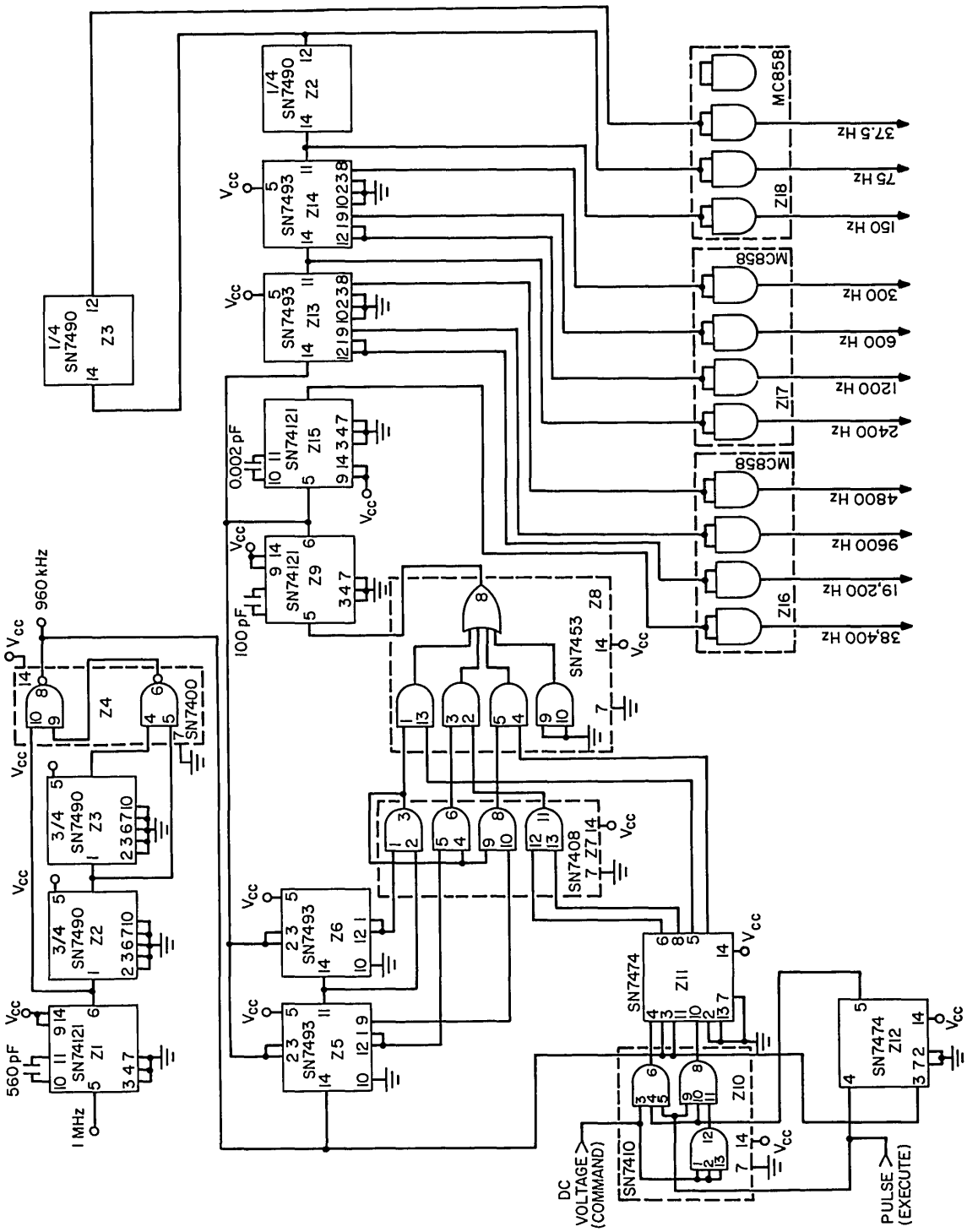


Fig. 15 — Data clock generator with phase shifter

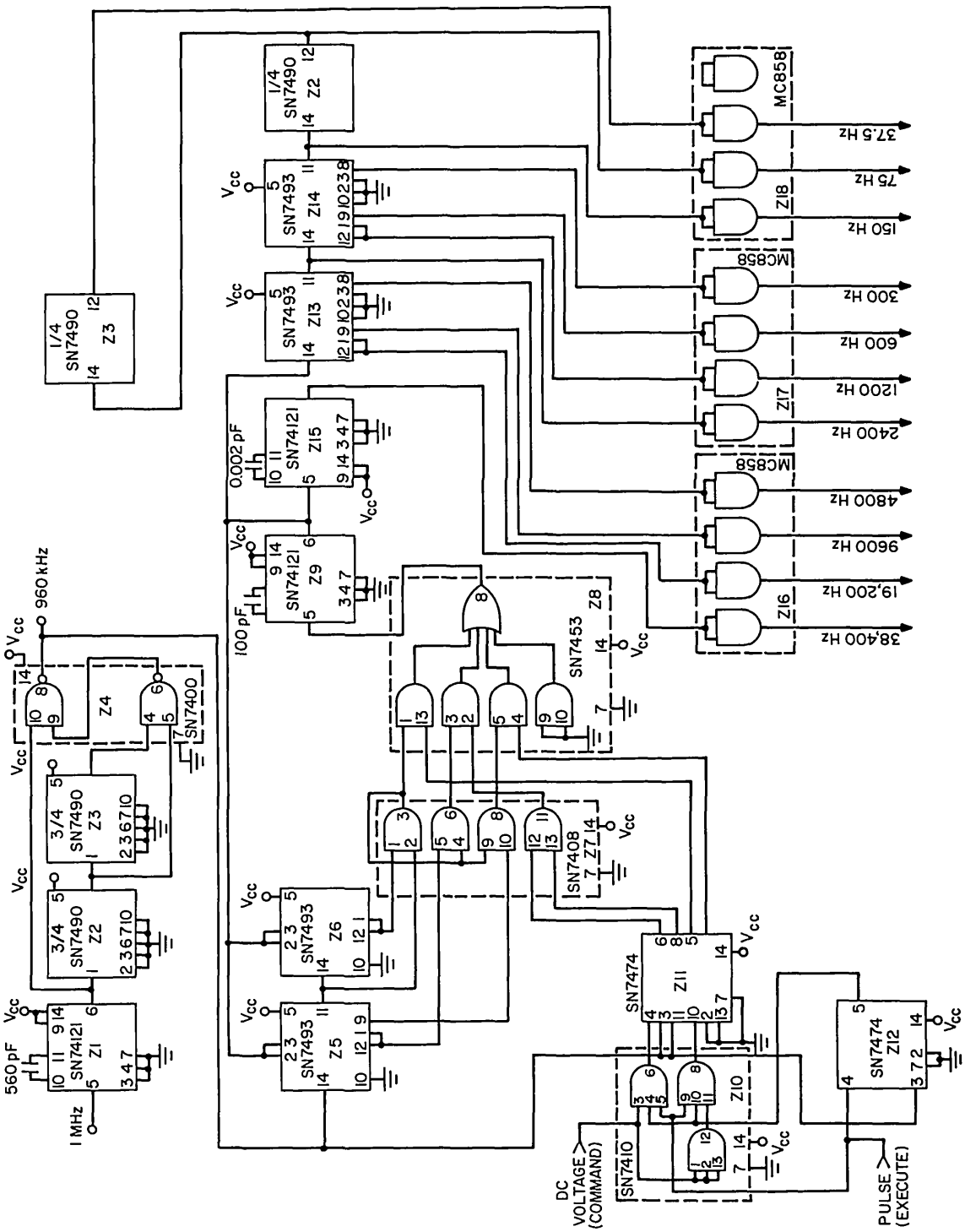


Fig. 15 — Data clock generator with phase shifter

Table 6
Approximate Time for 360° Phase Shift

Data Clock Rate (Hz)	Approximate Time to Complete a One-Cycle Phase Shift (ms)		Number of Steps (Based on 1-μs steps)
	Leading	Lagging	
37.5	666.67	720.00	26,666.67
75	333.33	359.99	13,333.33
150	166.67	180.00	6666.67
300	83.33	89.99	3333.33
600	41.67	45.00	1666.67
1200	20.83	22.50	833.33
2400	10.42	11.25	416.67
4800	5.21	5.62	208.33
9600	2.60	2.81	104.16
19,200	1.30	1.41	52.08
38,400	0.65	0.70	26.04

lag step is always 27 μs and the lead step is always 25 μs. This is approximate but provides a good indication of the length of time required.

Although there is a 1-μs jitter, this would be negligible for essentially all communication purposes. If a smaller jitter is required, the 5-MHz output of a frequency standard could be used. A frequency of 4.8 MHz could be derived by dropping one pulse of the 5×10^6 bps clock at the rate of 2×10^5 bps. A fixed $N/5$ divider would follow to provide the 960-kHz to the present circuit. This would provide data clocks with a jitter of 0.2 μs. If smaller steps are desired, the programmable divider and $N/5$ divider could be reversed. In this case the steps would be 0.2 μs instead of 1 μs.

CONCLUSIONS

A device for experimental laboratory use has been designed and proved suitable for generation of the standard digital data clock rates of 38,400, 19,200, 9600, 4800, 2400, 1200, 600, 300, 150, 75, and 37.5 Hz from an externally supplied 1-MHz frequency standard. The incorporation of a digital phase shifter permits synchronization of the output with signals in the system under study. This device provides phase-controlled standard-data-rate signals with frequency-standard accuracy.

ACKNOWLEDGMENT

The authors acknowledge the invaluable contributions of Mr. W.E. Leavitt of the Satellite Communication Branch.

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Security Classification

DOCUMENT CONTROL DATA - R & D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY *(Corporate author)* Naval Research Laboratory Washington, D.C. 20375	2a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED 2b. GROUP

3. REPORT TITLE

STANDARD DIGITAL DATA CLOCK-RATE GENERATOR WITH PROGRAMMABLE DIGITAL PHASE SHIFT

4. DESCRIPTIVE NOTES *(Type of report and inclusive dates)*

Final report on one phase of a continuing NRL problem.

5. AUTHOR(S) *(First name, middle initial, last name)*

James P. Spraitz and Gerald J. Hilwig

6. REPORT DATE June 29, 1973	7a. TOTAL NO. OF PAGES 22	7b. NO. OF REFS 5

8a. CONTRACT OR GRANT NO. NRL Problem R01-34 b. PROJECT NO. Project RF21-222-401-4353 c. d.	9a. ORIGINATOR'S REPORT NUMBER(S) NRL Report 7572 9b. OTHER REPORT NO(S) *(Any other numbers that may be assigned this report)*

10. DISTRIBUTION STATEMENT

Approved for public release; distribution unlimited.

11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY Department of the Navy Office of Naval Research Arlington, VA 22217

13. ABSTRACT

To perform research and development of satellite-communications circuits, subsystems, and system concepts, a device was designed to generate standard digital data clock rates and to provide continuous, programmable digital phase-shift control to permit synchronization of the output signal to other system signals. This equipment provides data clock rates of 38,400, 19,200, 9600, 4800, 2400, 1200, 600, 300, 150, 75, and 37.5 Hz based on a 1-MHz input signal from a frequency standard.

DD FORM 1 NOV 65 1473 (PAGE 1)

S/N 0101-807-6801

Security Classification

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Digital clocks						
Modem						
Data timing						
Programmable phase shifter						
Digital data						
Synchronization						
Frequency standards						

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(PAGE 2)