

Interactive Effects of Bond Wires Used for Microwave Semiconductor Device Combining and Matching Circuitry

R. E. NEIDERT, H. A. WILLING, AND B. E. SPIELMAN

*Microwave Technology Branch
Electronics Technology Division*

March 5, 1980



NAVAL RESEARCH LABORATORY
Washington, D.C.

Approved for public release; distribution unlimited.

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM	
1. REPORT NUMBER NRL Report 8388	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle) INTERACTIVE EFFECTS OF BOND WIRES USED FOR MICROWAVE SEMICONDUCTOR DEVICE COMBINING AND MATCHING CIRCUITRY		5. TYPE OF REPORT & PERIOD COVERED Interim report on a continuing NRL problem	
		6. PERFORMING ORG. REPORT NUMBER	
7. AUTHOR(s) R. E. Neidert, H. A. Willing, and B. E. Spielman		8. CONTRACT OR GRANT NUMBER(s)	
9. PERFORMING ORGANIZATION NAME AND ADDRESS Naval Research Laboratory Washington, DC 20375		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS NRL Problem 68-0789-0-0 Project RR021-03-46	
11. CONTROLLING OFFICE NAME AND ADDRESS Office of Naval Research Arlington, VA 22217		12. REPORT DATE March 5, 1980	
		13. NUMBER OF PAGES 10	
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		15. SECURITY CLASS. (of this report) UNCLASSIFIED	
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE	
16. DISTRIBUTION STATEMENT (of this Report) Approved for public release; distribution unlimited.			
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)			
18. SUPPLEMENTARY NOTES			
19. KEY WORDS (Continue on reverse side if necessary and identify by block number)			
Microwave Solid state devices Transistors Diodes		Combining Matching Bonding Bond wires	
20. ABSTRACT (Continue on reverse side if necessary and identify by block number)			
<p>For arrays of bond wires, inter-wire coupling can significantly affect the parameters of the individual wires. Design information is given for two port problems consisting of multiple bond wire arrays over a ground plane.</p> <p>Secondly, bond wire coupling can degrade the combining efficiency of several wire-combined solid state devices (such as transistor unit cells). This problem is modeled and analyzed, and remedies are suggested.</p>			

CONTENTS

INTRODUCTION	1
BOND WIRES AS TWO-PORT MATCHING CIRCUIT ELEMENTS	1
BOND WIRES AS SEMICONDUCTOR DEVICE PARALLELING ELEMENTS	4
CONCLUSIONS	6
ACKNOWLEDGMENTS	7
REFERENCES	7
APPENDIX -- Method to Evaluate Multiwire Individual Impedances	8

INTERACTIVE EFFECTS OF BOND WIRES USED FOR MICROWAVE SEMI- CONDUCTOR DEVICE COMBINING AND MATCHING CIRCUITRY

INTRODUCTION

The work described in this paper is primarily related to linear power amplification using single and multicell gallium arsenide power MESFETs (metal semiconductor field effect transistors) [1]. The use of bond wires as two-port microwave circuit elements for impedance matching and as multiport semiconductor device combining networks is applicable to FETs and a wide range of other devices.

In general, the unit cell transistor (bipolar or FET) or the unit cell diode (Gunn, IMPATT, etc.) is physically small and its unit power dissipation capability is small. In many cases useful microwave power levels are achieved only by combining several unit cells. Great benefit in bandwidth can often result from the judicious use of bond wires as microwave circuit elements between the semiconductor unit cells and the external distributed microwave circuitry such as microstrip.

The next section of this report treats bond wires as two-port matching circuit elements, taking inter-wire coupling into account, and the following section describes the problem associated with the use of bond wires as multiport semiconductor device-combining elements, again taking inter-wire coupling into consideration.

BOND WIRES AS TWO-PORT MATCHING CIRCUIT ELEMENTS

Figure 1 shows an example circuit discussed in this report. To the left side of the air gap is a microstrip transmission line whose conductor width, w , is much less than a wavelength in the dielectric with permittivity, ϵ_r . It is assumed that the wires connect to common voltage points at each end. The equivalent circuit of the set of coupled wires across the gap is that of a single transmission line having some characteristic impedance and an electrical length, θ . The electrical length in the air gap is

$$\theta = \frac{2\pi f}{3 \times 10^{10}} \ell \text{ radians,}$$

where f is frequency in Hertz and ℓ is the physical length in centimeters. The total characteristic impedance of a set of wires above ground can be developed from a method outlined in Ryder [2], with the inclusion of the line images below ground. It should be noted in that method that at very high frequencies, the geometric mean radius (GMR) of a single wire approaches its physical radius, as described in Terman [3]; therefore all $(r_n e^{-1/4})$ terms in Ryder may be replaced with $(r_n e^0 = r_n)$. Figure 2 shows the general case of a set of wires above ground, with the image indicated. The total characteristic impedance in air, Z_{OT} , of the real set of wires to ground is

$$Z_{oT} = \frac{60}{n^2} \log_e \left[\frac{\prod_{i=1}^n \prod_{k=1}^n (D_{ik})}{\prod_{i=1}^n \left[r_i \cdot \prod_{j=1}^n (D'_{ij}) \right]} \right] \text{ ohms,}$$

where n is the number of real wires, D_{ik} is a physical distance term from the i th real wire to the k th image wire, D'_{ij} is a physical distance term from i th real wire to the j th real wire, and r_i is the physical radius of the i th real wire. Figure 3 shows some selected impedance calculation results.

Experimental measurements were made using the circuit shown in Fig. 1. The diameter of the bond wires was 0.00254 cm, the centerline wire height was 0.0762 cm, the microstrip transmission line width was 0.0559 cm over a 0.0635-cm-thick alumina substrate with permittivity, ϵ_r , of 9.985, and the wire spacing was $[0.0559 \text{ cm}/(n + 1)]$. Measurements were made for 1, 2, 3, 4, and 5 wires, with gap lengths of 0.0635, 0.127, and 0.254 cm. One example of the measurement results (for 4 wires over a gap length of 0.127 cm) is shown in Fig. 4. The calculated value of Z_0 for this case is 171 Ω . The equivalent circuit with which this data should agree is also shown on Fig. 4. The capacitor, C_f , was found by an earlier measurement without wires to be 0.012 pF. A computer optimization of the wire length was made with Z_0 and C_f held fixed at the above values. The resultant "best fit" wire length was 0.144 cm, for a gap length of 0.127 cm. The difference of 0.017 cm may be attributed to the short vertical portions of the bond wires at each end, and is approximately equal to the sum of the lengths. Indeed, throughout all the above measurements with different numbers of wires and different gap lengths, the "best fit" wire length was approximately the total wire length. Therefore, rather than use a separate analysis of the vertical portion of the wires, so long as they are much less than the gap length, it appears suitable to include them in the wire length over the gap. Figure 4 shows agreement between measured and calculated reflection coefficient angle when the wires are treated as a transmission line.

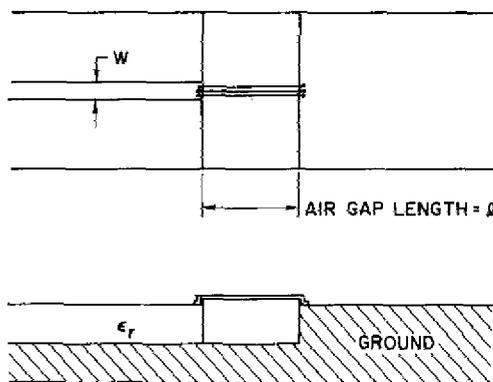


Fig. 1 - Example circuit for analysis of bond wires as matching circuit elements

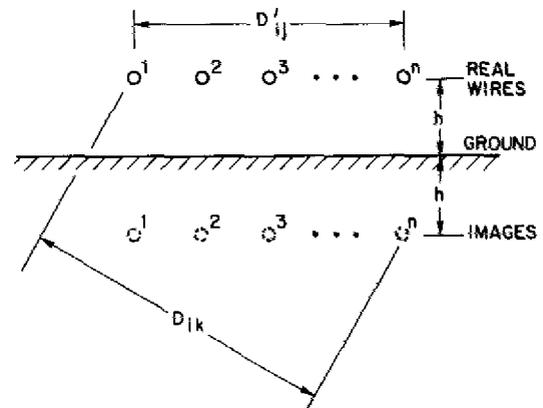


Fig. 2 - Method of images for characteristic impedance calculation

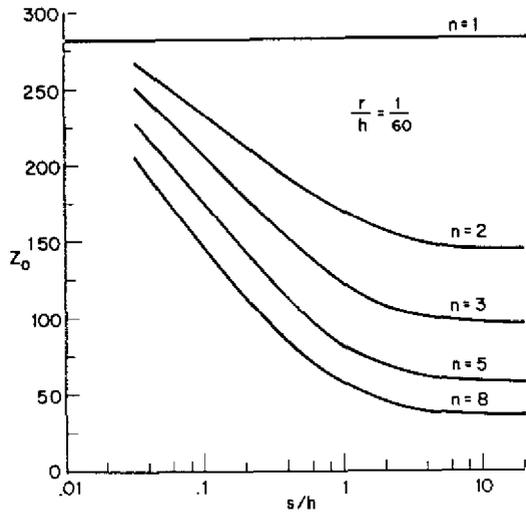


Fig. 3 — Multiwire characteristic impedance vs wire center line spacing to center line height ratio

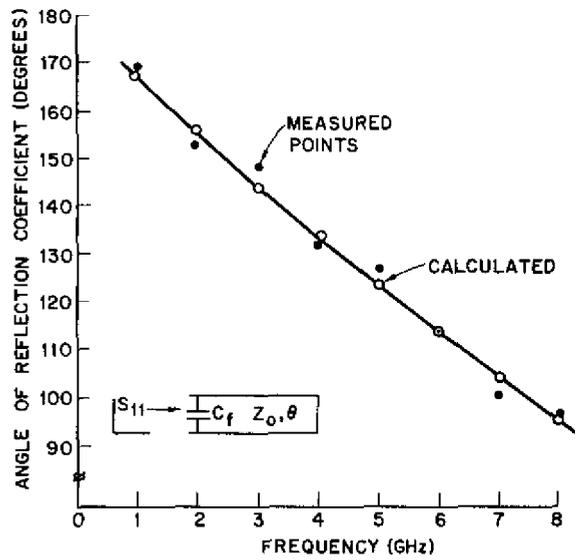


Fig. 4 — Angle of reflection coefficient vs frequency

BOND WIRES AS SEMICONDUCTOR DEVICE PARALLELING ELEMENTS

Figure 5 illustrates a typical case of microwave semiconductor element combining with bond wires. The Z_L terms might represent the input impedance to each cell of a multicell microwave transistor. The three-wire coupled transmission line system shown is assumed to be over air dielectric, and to be attached on the left side to a point of common voltage (for example, the end of a narrow microstrip transmission line). Due to interwire coupling, the characteristics of each wire from the center wire outward, thought of as an isolated transmission line to each load Z_L , is unlike all the others. A general solution requires the formulation of an n -by- n matrix of parameters relating the n input ports to the n output ports. A more restrictive solution will be used in the following discussion.

If the bond wires, as paralleling elements, are electrically short, a first order treatment of their individual characteristic impedances may be found using the Appendix or by using a modified version of computer program MS in [4], by solving the static capacitance problem for each wire to ground in the presence of the other wires, with all wires excited at the same voltage. For the three-wire case pictured in Fig. 5, sample calculations were performed. The wire centerline spacing used in the calculations was 0.0203 cm to conform with the gate pad spacings at the input of a particular three-cell FET; the other dimensions were the same as those mentioned in the second section of this report. The calculated line impedances, referring to Fig. 5, were: $Z_{01} = 461 \Omega$ and $Z_{02} = 605 \Omega$. Since the loads, Z_L , are all equal, it is apparent that, except for a wire length approaching zero, different voltages would appear at the respective loads. It appears that power combining might not be complete in multidevice amplifiers. Also, the impedances terminating multielement sources would not be identical for each element.

A simplified, first-order approach to the solution of this problem for the special case of paralleling microwave semiconductor devices, can be given. In typical applications, the characteristic impedance level of bond wires, whether single or in sets, is much higher than their terminating impedances and they are electrically short. Each wire may then be represented approximately [5] by a pi equivalent circuit, consisting of shunt C , series L , and shunt C . The predominant element in this representation, for the stated environment, is the series inductor, whose value is directly proportional to the product of its length and its

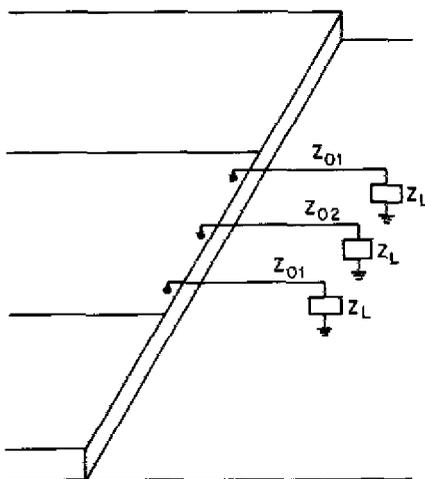


Fig. 5 — Example circuit for analysis of bond wires as semiconductor device paralleling elements

characteristic impedance: $L \propto Z_o \theta$. Therefore if this product is maintained for all the wires of a set, the electrical unbalance can be approximately offset by a designed physical unbalance. Methods of doing this may include lengthening the wires, by increasing amounts, as the distance from the center wire (or point of symmetry) increases, tapering the ground plane beneath the wires, or varying the wire diameters.

The multiwire individual impedances needed to determine the $Z_o \theta$ product described above might be satisfactorily evaluated using the following simple approximation method. In Ryder, in the place already cited, there is information for such a calculation. It yields the individual wire impedances assuming equal currents in all the wires:

$$Z_{oi} = 60 \log_e \left[\frac{\prod_{k=1}^n (D_{ik})}{r_i \cdot \prod_{\substack{j=1 \\ (j \neq i)}}^n (D'_{ij})} \right] \text{ ohms,} \quad (i = 1, 2, \dots, n)$$

where the terms are as defined in the second section of this report. The wire-to-wire impedance spread by this calculation is somewhat less than for equal voltages on the wires.

An interesting example of the effect of unequal bond-wire impedances is shown on the calculated results of Fig. 6, while Fig. 7 shows the related circuitry. In Fig. 7, the S-parameter matrix, $[S_1]$, was a measured set of parameters for a single cell gallium arsenide power field effect transistor, modified to move the range of unconditional stability down to about 2 GHz. Bond wires are assumed to be attached, then, to three adjacent cells and taken off to a common point on the input (gate) side, and to a common point on the output (drain) side. The physical dimensions were the same as earlier described, for which Z_{01} is taken to be 461Ω and Z_{02} is 605Ω . The cascade connections of the input and output lines with $[S_1]$ produces the S-parameter matrices $[S'_n]$. Finally, the paralleling of the three $[S'_n]$ matrices produces the S-parameter matrix, $[S_{TOTAL}]$.

From the $[S_{TOTAL}]$ matrix, the performance of the three cells in parallel was computed and the results appear in Fig. 6. These are curves of maximum available gain (MAG). In Fig. 6, curve 1 applies to either a single cell device, or the three-cell device with the bond wires of zero length, or the three-cell device with bond wires of equal impedance and arbitrary but equal lengths. Curves 2, 3, and 4 are computed curves for $Z_{01} = 461 \Omega$ and $Z_{02} = 605 \Omega$ for wires which are 0.0635 cm, 0.127 cm, and 0.254 cm long, respectively. Large dips in the value of achievable gain have resulted, with the frequency at which the dip occurs decreasing as the bond wire length increases.

The correction method outlined in this section was tested. The length of the two outer wires was increased by the ratio of Z_{02} to Z_{01} , with their impedance held at the Z_{01} value. This is not easy to reproduce physically because the impedance of the extended wires has a different value when not in the presence of the center wire; however, it is analytically valid if the suitability of a constant ($Z_o \theta$) product is valid. The MAG dips disappeared and the calculated curve was again curve 1, showing the merit of the approximate correction method.

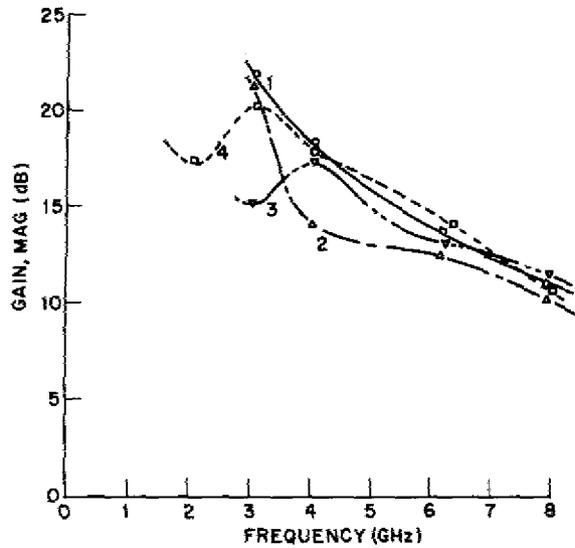


Fig. 6 — Calculation results of the effect of combining with unequal impedance wires

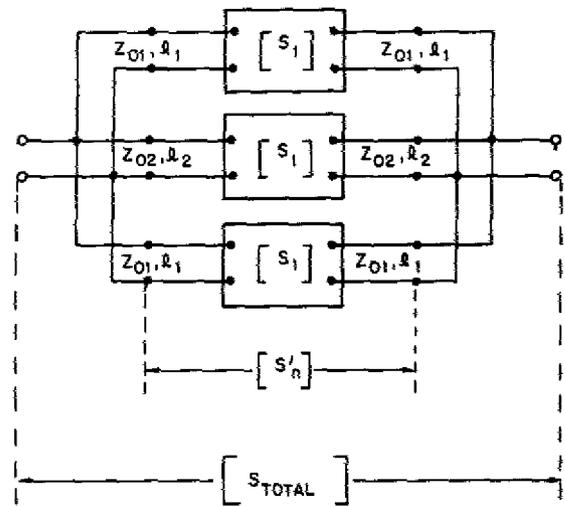


Fig. 7 — Combining procedure

The transistor gain dips appear to have their origin in high Q loop paths among the cells when balance is anything other than perfect. The phase offset of the voltages being applied to the input gates, for instance, may be magnified many times by the loop circuit Q . The phase difference of the several voltages at the output recombination point, then, may be much greater than might be expected.

More gain ripple has been observed experimentally in multicell transistors than in single cell transistors, but it has been difficult to attribute it to bond-wire coupling only. Bond-wire coupling is not the only source of unbalance in multicell transistors. Other sources include inherent differences in the cells themselves and possible intercell coupling.

CONCLUSIONS

It has been shown that interwire coupling can significantly affect the circuit performance of arrays of bond wires used as two-port elements in microwave circuits (e.g., matching circuits) and as multiport networks for combining microwave solid state devices. Simple, approximate models were posed and appear to treat these effects adequately. Based upon these models, it appears that straightforward remedies (e.g., the adjustment of individual wire lengths) can adequately mitigate deleterious effects on performance when bond wires are used to combine microwave solid-state devices (e.g., unit cell bipolar transistors, FETs, Gunn or IMPATT diodes).

ACKNOWLEDGMENTS

The authors thank Leo Young for his helpful suggestions and comments and H. E. Heddings for his experimental fabrication and test support.

REFERENCES

1. R.E. Neidert and H.A. Willing, "Wide-Band Gallium Arsenide Power MESFET Amplifiers," IEEE Transactions on Microwave Theory and Techniques MTT-24 (No. 6), 342-350 (June 1976).
2. J.D. Ryder, *Networks, Lines, and Fields*, 2nd ed. Englewood Cliffs, New Jersey: Prentice-Hall, 208-229 (1955).
3. F.E. Terman, *Radio Engineers' Handbook*, New York and London: McGraw-Hill, 49-50 (1943).
4. B.E. Spielman, "Computer-Aided Analysis of Dissipation Losses in Isolated and Coupled Transmission Lines for Microwave and Millimeter-Wave Integrated-Circuit Applications," NRL Report 8009, July 1976.
5. G.L. Matthaei, L. Young, and E.M.T. Jones, *Microwave Filters, Impedance-Matching Networks, and Coupling Structures*, New York, San Francisco, Toronto, London: McGraw-Hill, 361 (1964).

Appendix

METHOD TO EVALUATE MULTIWIRE INDIVIDUAL IMPEDANCES

The multiwire individual impedances might be evaluated satisfactorily using the following method. The assumption of uniform charge distribution is required in addition to that of equal voltages on the wires. Then the voltages between the various conductors and ground can be obtained, such that $[V] = [P][Q]$, where $[P]$ is the matrix of Maxwell's Potential Coefficients. Referring to Fig. 2, the terms of the $[P]$ matrix are

$$P_{ik} = \frac{1}{2\pi\epsilon} \log_e \left(\frac{D_{ik}}{D'_{ij}} \right) \text{ with } j = k, \text{ noting also}$$

that $D'_{ij} = r_i$ when $i = k$. For air dielectric,

$$\epsilon = \epsilon_{\text{air}} = 8.85 \times 10^{-12} \text{ farad/meter.}$$

Then, from $[Q] = [C][V]$, the capacitance matrix is the inverse of the potential matrix, or:

$$[C] = [P]^{-1}$$

Since all the voltages are assumed equal,

$$Q_i = \left(C_{i1} + C_{i2} + C_{i3} + \dots + C_{in} \right) V,$$

or

$$Q_i = C_{T_i} V.$$

Thus the total capacitance from wire i to ground is obtained in terms of the physical dimensions of the multiwire system. Then each individual wire's characteristic impedance to ground is given by $Z_{0i} = 1/(v_{\text{air}} C_{T_i})$, where $v_{\text{air}} = 3 \times 10^8$ meters/sec. Differences between this solution and that obtained in [4] are small for typical bond wire configurations. For the three wire case above, this method yields $Z_{01} = 460 \Omega$ and $Z_{02} = 607 \Omega$, while the more exact solution allowing for nonuniform charge distribution yields 461Ω and 605Ω .