



**Interference Rejection and Detection Performance
of the *Smallest of Circuit***

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13. ABSTRACT (Maximum 200 words) Radar systems encounter severe interference when other nearby systems operate on the same frequency. Usually, this type of interference is eliminated with a binary integrator or <i>M</i> -out-of- <i>N</i> detector. The loss of amplitude information is a disadvantage incurred with this type of detector, also the detection performance is worse than that of a detector that integrates the signal prior to thresholding. This report describes the means of eliminating asynchronous interference by amplitude comparison of consecutive radar sweeps; the smaller of the two is retained. Interference is eliminated, amplitude information is retained, and the detection performance is shown to be only 0.7 dB worse than that of a moving window integrator.				
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INTERFERENCE REJECTION AND DETECTION PERFORMANCE OF THE "SMALLEST OF" CIRCUIT

BACKGROUND

A method of rejecting asynchronous pulsed interference was proposed [1]. In this method the smaller of two amplitudes in two consecutive radar sweeps is selected for every pair of range samples. Figure 1 shows a diagram of the circuit. If a large signal occurs only in one of the two sweeps, the circuit chooses the smaller signal and rejects the larger. Signals from targets are usually present (at the same range) in a number of consecutive sweeps, and the circuit passes these signals with only a small amplitude reduction. This circuit has been built and tested on two SPS-10 radars [2].

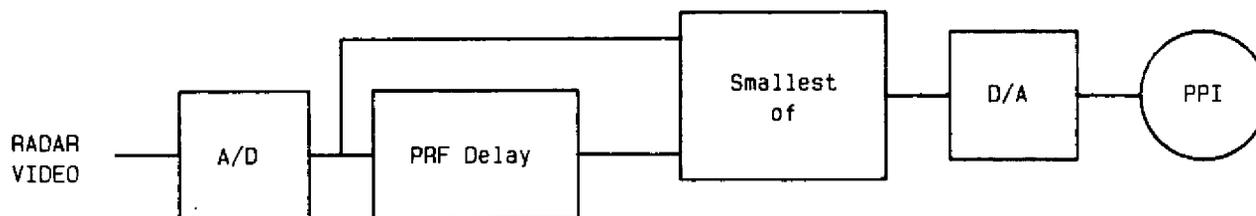


Fig. 1 — *Smallest of* interference rejection circuit

The use of an M -out-of- N detector is a more conventional way for eliminating asynchronous interference. Radar video is thresholded, and one or more sweeps are saved in a memory. When threshold crossings occur at the same range in more than one sweep, a valid return is declared. If the analog to digital (A/D) converter is reduced to one bit, then the *smallest of* circuits is nearly identical to a 2 out of 2 detector. The disadvantages of using the single bit interference eliminators are that the video amplitude information is lost, the detection performance is poor [3], and usually a constant false alarm rate (CFAR) is needed to adjust the threshold. The *smallest of* circuits retains amplitude information and requires no CFAR for proper operation.

Figure 2 shows two examples of the circuit's operation with video interference injected into the radar; for Fig. 2(b) the *smallest of* circuit was active to a range of 80 nmi, and the range rings are at 40 and 80 nmi. Since no CFAR was used, extended land targets retain their proper shape. Some loss in detectability is expected because the smallest of two consecutive radar sweeps is chosen; however, the same logic operates on noise and also reduces the noise level. To obtain a quantitative value for the effect on detection performance, a computer simulation was performed.

SIMULATION OF *SMALLEST OF*

The *smallest of* processor was compared to a *moving window* reference processor that integrates detected signal returns during an antenna dwell. The signals were weighted uniformly; so while the

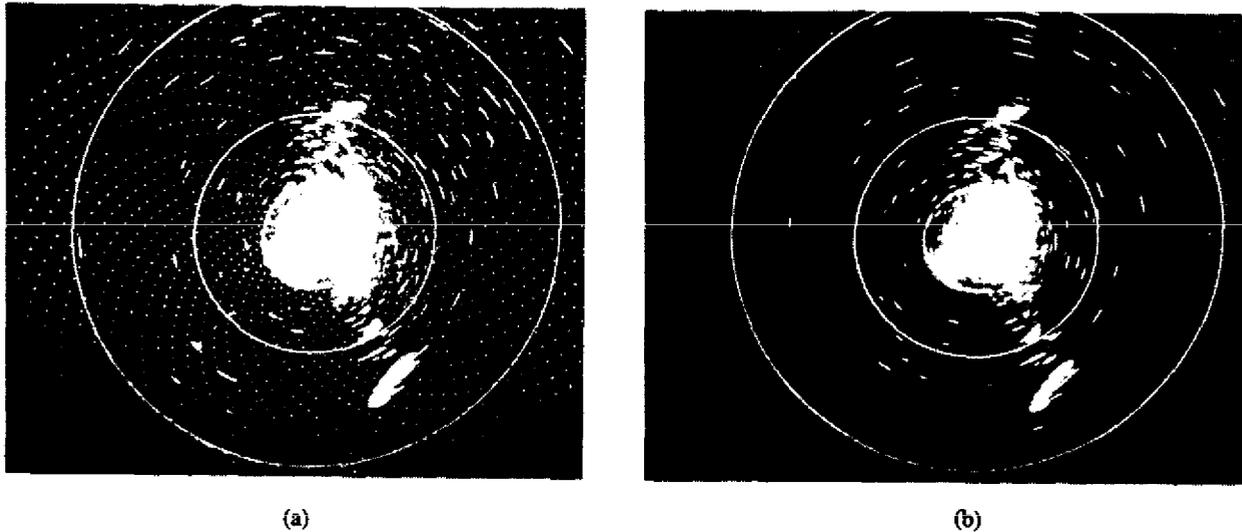


Fig. 2 — PPI photographs showing interference without use of the circuit (a) and rejection of interference with use of the circuit (b)

reference processor is not optimum, it should be within ~ 0.5 dB of an optimum processor [3]. Figure 3 is a diagram of the simulation showing the processors and the signal and noise generators. The antenna pattern and the number of pulses in a dwell were chosen to approximate those of the SPS-10 radar. A $\sin(x)/x$ function was used for the one-way antenna pattern scaled to a 3 dB beamwidth of 1.45° . At the normal rotation rate and pulse repetition frequency (PRF) 10 pulses are within a beamwidth. Only one computation was done per dwell; the peak of the beam was approximately centered in the integration window. From dwell-to-dwell the location of individual pulses was randomized by ± 0.6 of the pulse-to-pulse spacing. Figure 4 shows envelopes of the normal signal and the *smallest of* as they enter the integrator in a noise-free case. The *smallest of* processor needs an initial value so that 10 outputs can be integrated by both processors. As in a real system, the initial value comes from a pulse prior to the group of pulses used in the integration window. To generate the curves shown in Fig. 4 the processing was started at negative angular displacements and moved to the right; the output of the *smallest of* is less than the normal output until the peak of the beam is passed, then both processors have nearly the same outputs. In the example used, the peak output from the *smallest of* processor lags the normal peak by 5% of the beamwidth.

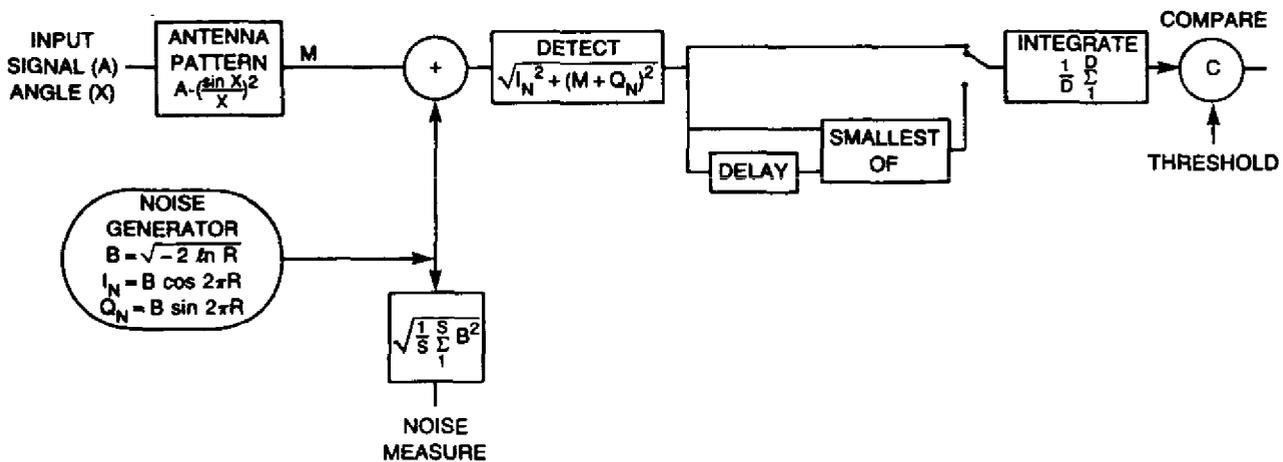


Fig. 3 — Simulation process used to calculate detection performance

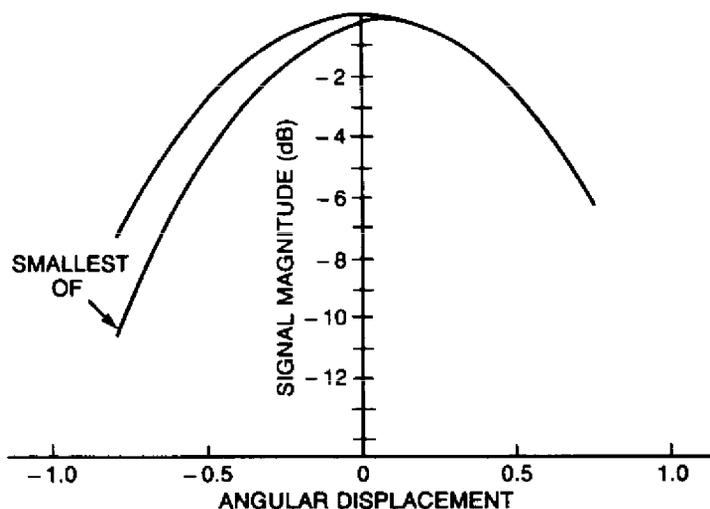


Fig. 4 — Signal input to integrator as a function of angle

The additive noise has a uniform phase distribution and a Gaussian amplitude distribution given by

$$I_N = B \cos 2\pi R,$$

$$Q_N = B \sin 2\pi R, \text{ and}$$

$$B = \sigma(-2 \ln R)^{1/2},$$

where I_N and Q_N are the inphase and quadrature components of noise, and R is a uniformly distributed random number between 0.0 and 1.0.

Figures 5 and 6 show histograms of noise distributions and signal, plus noise distributions, prior to the integrator. Figure 5 shows only noise as the *smallest of* circuit reduces the number of occurrences of larger amplitudes. A signal ~ 3.6 times the root-mean-square noise amplitude was added to the noise for the histograms shown in Fig. 6; while the normal histogram is symmetrical, the *smallest of* is skewed toward smaller amplitudes.

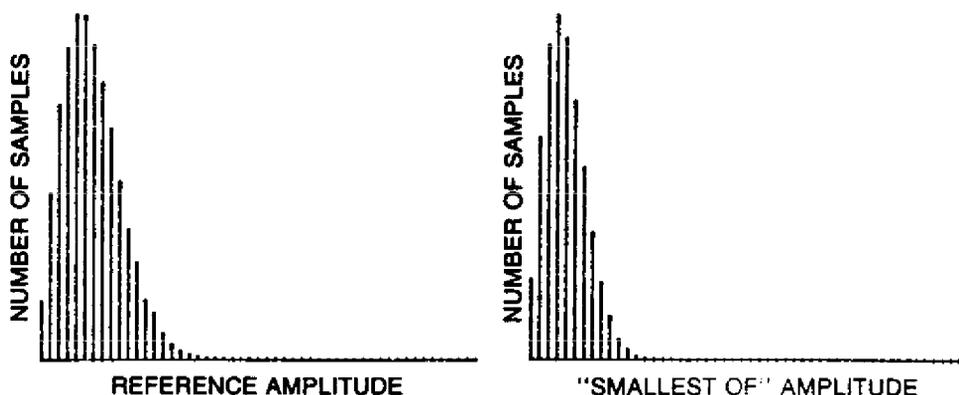


Fig. 5 — Distribution of noise used in simulation showing the effect of the *smallest of* process

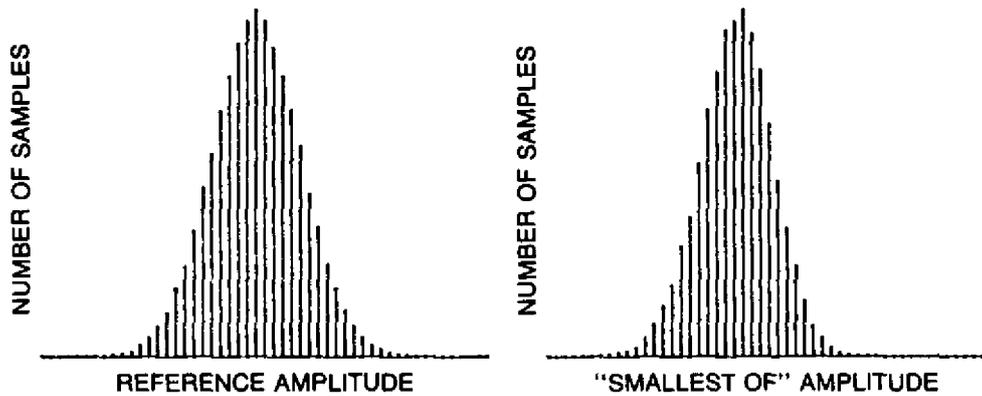


Fig. 6 — Distributions of noise + signal prior to integration

SIMULATION RESULTS

The first step in the simulation is to determine the threshold setting T for various false alarm rates. Figure 7 shows the results that were obtained by setting the input signal to zero and measuring the probability of false alarm (P_{fa}) as a function of the threshold setting. Approximately 10^7 trials were used. Now, one can use threshold settings at a desired P_{fa} and measure the probability of detection (P_d) by running the simulation with various values of signal amplitude.

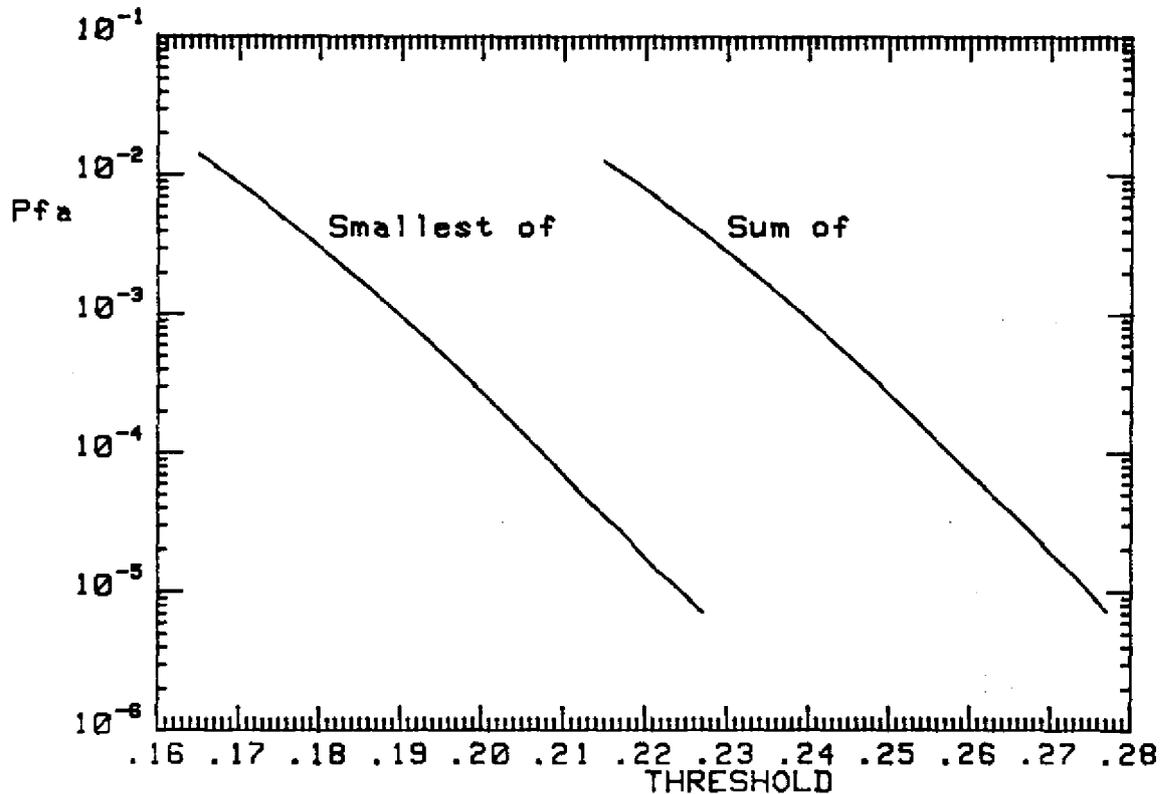


Fig. 7 — Probability of false alarm as a function of threshold level using pulses from an antenna dwell

Figure 8 shows the detection results for false alarm rates of 10^{-3} and 10^{-5} . The input signal-to-noise ratio (SNR) is plotted as a function of P_d for both processors. For values of P_d near 0.9 the *smallest of* processor requires ~ 0.7 dB more signals than the moving window integrator does. The difference between the two processors is fairly constant with increasing advantage for the moving window at higher values of P_d and higher P_{fa} . As a check of the simulation, a simplified case was run where an optimum processor was compared to a version of the *smallest of*.

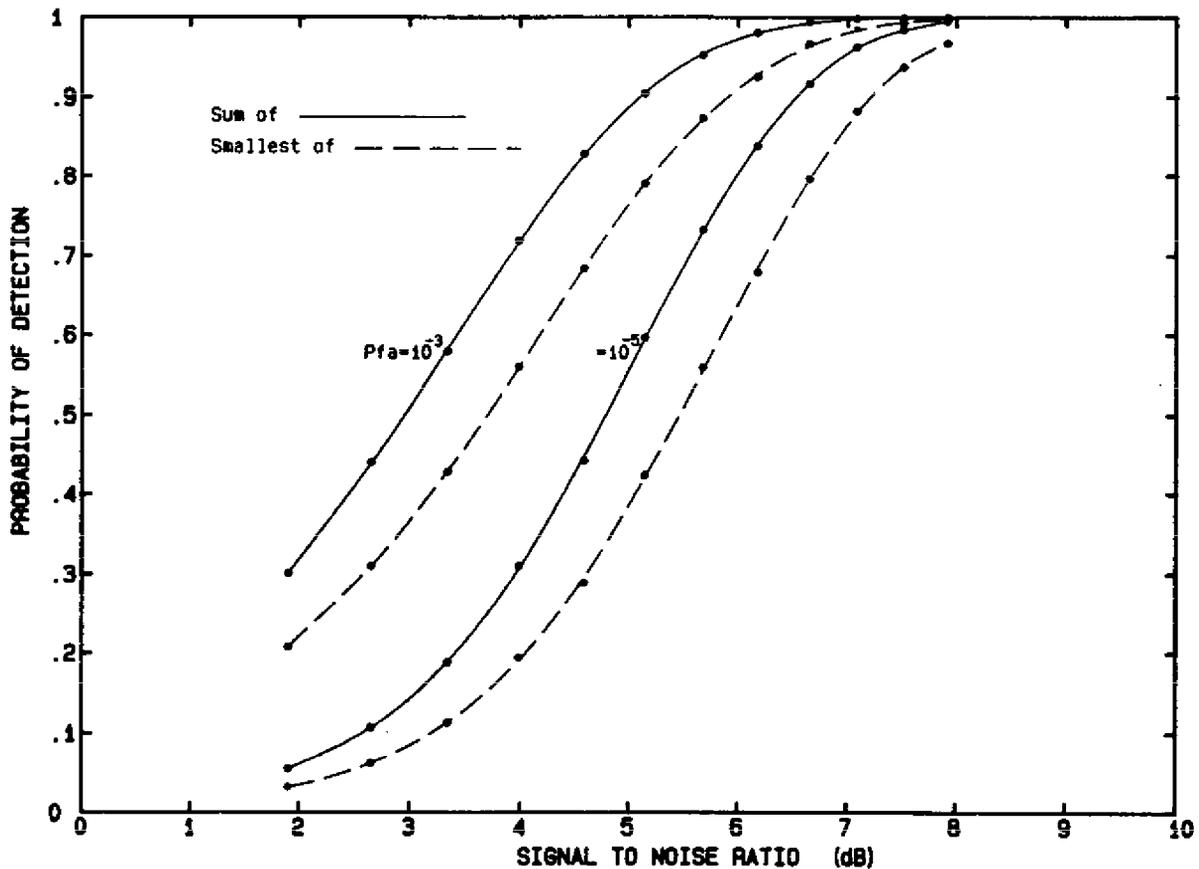


Fig. 8 — Probability of detection as a function of the input signal-to-noise ratio for a processor that uses pulses from an antenna dwell

TWO-PULSE SIMULATIONS

A second case was tried by processing groups of two equal-amplitude pulses. The reference processor adds two pulses while the *smallest of* chooses the one with the smaller amplitude. This case can be compared to the standard detection curves such as in Blake [4]. Again a noise-only case was run to calculate threshold settings for various values of P_{fa} . Figure 9 shows these results.

Figure 10 shows the detection performance of these two-pulse processors for P_{fa} of 10^{-3} and 10^{-5} . The *smallest of* processor always requires more SNR for equal values of P_d . For a P_d of 0.9, ~ 0.8 dB more is needed. The largest disadvantage shown in Fig. 10 for the *smallest of* processor is only 1.1 dB at a P_d of 0.99.

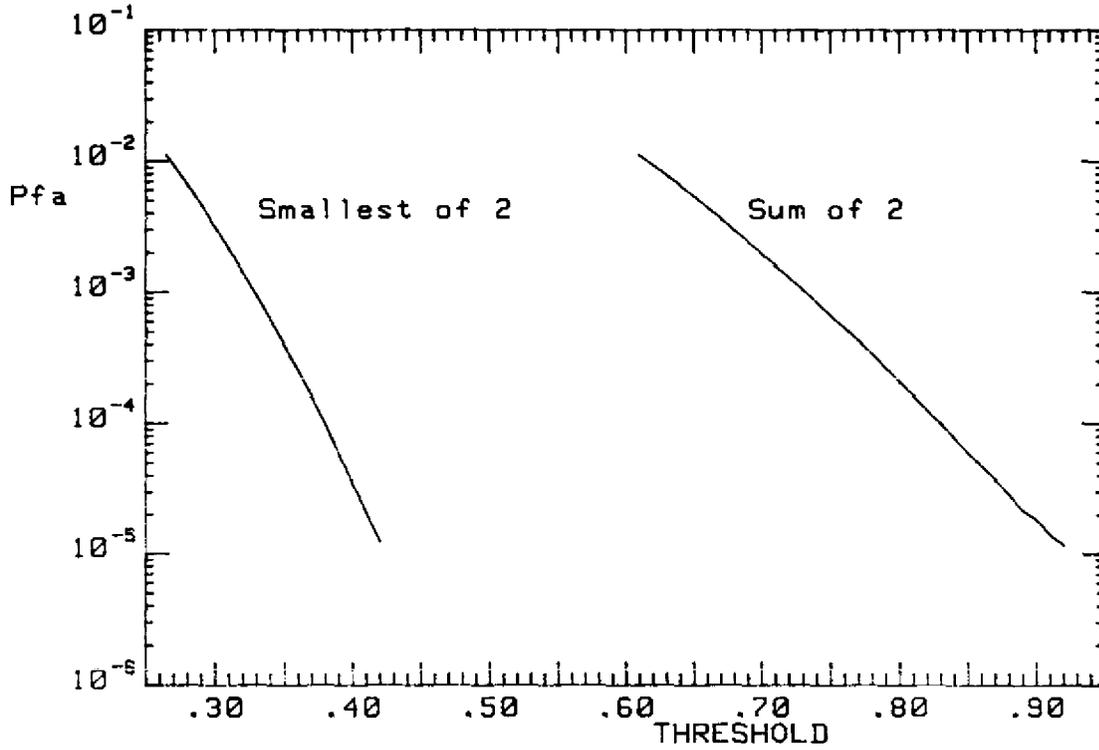


Fig. 9 — Two-pulse probability of false alarm as a function of threshold level

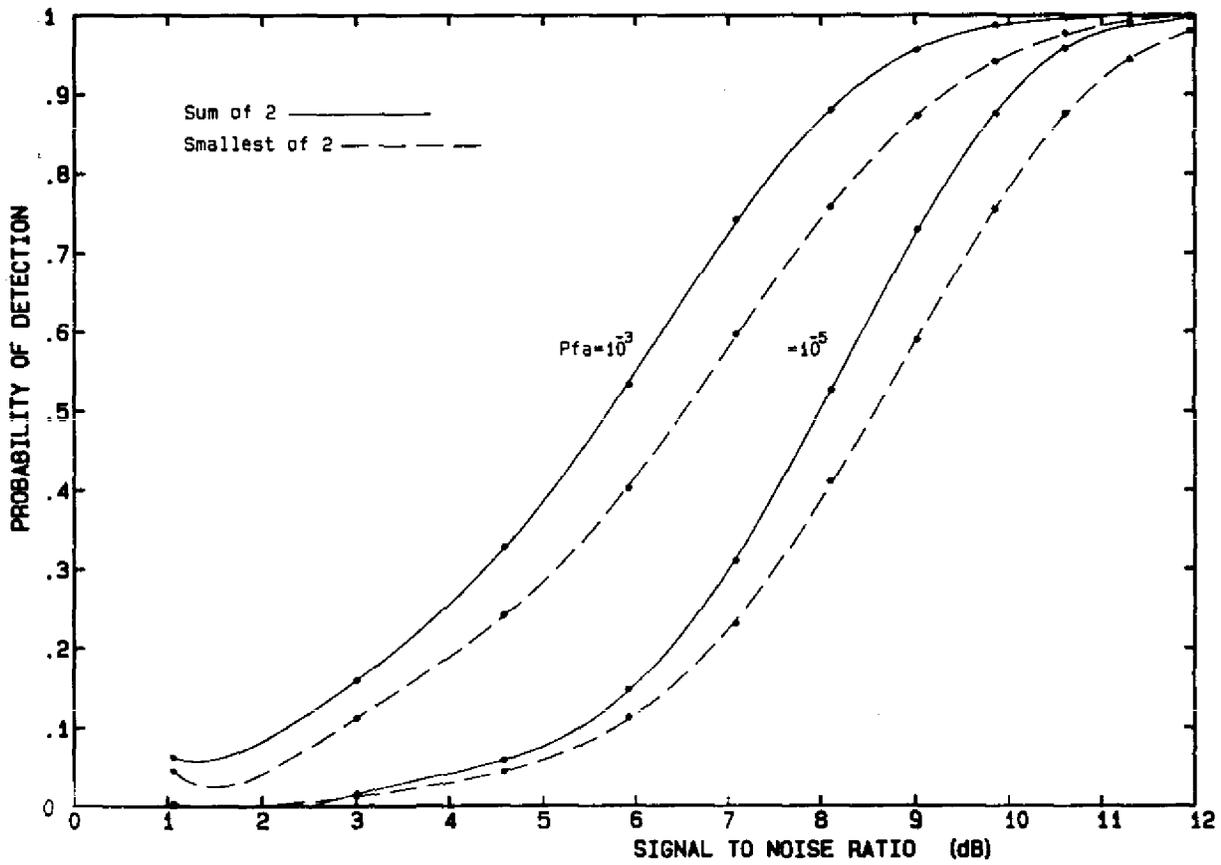


Fig. 10 — Two-pulse detection probability as a function of the input signal-to-noise ratio

CONCLUSIONS

The *smallest of* circuit that is effective in eliminating asynchronous pulsed interference, suffered very little reduction in signal detection performance (~ 0.7 dB) when compared to a normal moving window integrator. Even in the two-pulse simulation, which is less realistic and should clearly favor the addition of two pulses, the *smallest of* processor was ~ 0.8 dB worse.

REFERENCES

1. "Interference Rejection for the SPS-10," NRL Memorandum 5330-584L/GJL:pjw, dtd 10 Dec. 81.
2. B.R. Jarrett, "Time-Domains Radar Interference Rejections," 1984 Naval Research Laboratory Annual Review.
3. G.V. Trunk, "Survey of Radar ADT," NRL Report 8698, Jun. 1983.
4. L.V. Blake, "A Guide to Basic Pulse-Radar Maximum-Range Calculations, Part 1-Equations, Definitions, and Aids to Calculation," NRL Report 6930, Dec. 1969.