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Adaptive Feedforward Linear Wideband HF Power Bank

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To fulfill modern naval command, control, and communication requirements, a new, wideband, high-frequency (HF) communications system is being developed that is characterized by the complete removal of high-power switching and tuning and that uses adaptive-cancellation techniques in the transmitting subsystem to suppress unwanted radiation of noise and distortion. The report focuses on the development of an unusually linear 500-W power amplifier and describes techniques that have been applied to further reduce noise and distortion-product generation by means of iterated

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feedforward cancellation stages. Although three stages have been planned, only two have been implemented. To minimize power handling and distortion requirements of the auxiliary feedforward amplifiers, adaptively controlled weights are used to augment nonadaptive equalizers in the cancellation of fundamental energy for each stage. Performance measurements verifying the concept are presented, and various practical limitations are described. Intermodulation distortion-to-signal ratios of greater than −86 dBc have been achieved with the amplifier delivering two 100-W fundamental signals.

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ADAPTIVE FEEDFORWARD LINEAR WIDEBAND HF POWER BANK

CONSPECTUS

A new, wideband, high-frequency (HF) architecture is being developed to meet the operational requirements of full-duplex, antijam (AJ), and rapid-frequency-change capability. This architecture eliminates mechanically tuned, narrowband radio-frequency (RF) filters (multicouplers) in the transmitting and receiving subsystems of conventional shipboard HF communication systems in order to provide compatibility with wideband and frequency agile signal structures.

The transmitting subsystem of this new architecture consists of a number of agile exciters which drive a linear power bank. The linear-power-bank output is distributed to existing broadband transmitting antennas. The key portions of the linear power bank are the power bank and the power-bank linearizer.

This report focuses on the development of an adaptive, feedforward, linear HF power bank (linear power bank) for the new wideband HF architecture that is composed of an unusually linear HF power amplifier (the power bank) and describes adaptive techniques (the power-bank linearizer) used to reduce noise and distortion-product levels at the transmitting-subsystem output.

The power bank described in this report is composed of a single HF linear amplifier (power banks in the future will be composed of many HF linear amplifiers) and represents a significant step forward compared to typical contemporary amplifier performance. The amplifier operates broadband from 2 to 30 MHz. The amplifier is fully stable and will operate connected to any type of load with a VSWR (voltage standing-wave ratio) range from one to infinity over this frequency range. Operation is Class A and the overall efficiency, excluding losses in the power supply, for 500-W RF (two equal-amplitude tones output), is 9.4%. The level of third-order in-band intermodulation products generated under these conditions is −74 dBc at the low end of the frequency range and −54 dBc at the high end.

The power-bank linearizer (composed of several linearization stages) further improves the performance achieved by the power bank. Each linearization stage of the power-bank linearizer contains two feedforward cancellers—a feedforward fundamental-signal adaptive canceller (FSAIC) and a broadband, feedforward, nonadaptive intermodulation-distortion (IMD) canceller.

Although the ultimate objective for the linear power bank is a distortion level of −116 dBc (with a power-bank linearizer composed of three linearization stages) for signal output levels of 1 kW per fundamental, the hardware described in this report has a distortion level design goal of −100 dBc (with a power-bank linearizer composed of two linearization stages) when it delivers two 100-W signals.

Three sets of performance data are discussed and presented. Each set corresponds to one of three pairs of fundamental frequencies: 11.3 and 16.0 MHz, 4.8 and 5.5 MHz, and 2.0 and 2.3 MHz. A probe signal is also injected into the system such that it appears in the power-bank output but is not present in the reference-signal path to the linearizer. The probe signal appears to be generated in the

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power bank, but its frequency is selected so that it does not correspond to an actual IMD-product frequency. The relative amplitude of the probe signal with respect to the amplitude of the fundamentals is used to illustrate the potential cancellation available by use of the power bank linearizer. Output spectra discussed are for the power bank and linearizer delivering two 100-W tones (20 dBW) to a 50-Ω load.

The level of third-order in-band intermodulation products at the output of the linear power bank (for two 100-W tones to a 50-Ω load) are −87 dBc at the low end of the frequency range and −90 dBc at the high end. The probe signal is reduced to a level that varies from −102 dBc (cancelled by 44 dB) to −91 dBc (cancelled by 36 dB).

It is observed that the power bank linearizer has significantly reduced the amplitude of distortion products; however, the amount of reduction for many distortion products is not nearly as great as the reduction obtained for the probe signal.

Ideally, the power-bank linearizer should not generate distortion. It is observed however, that significant second-, third-, and fifth-order distortion products are generated within the linearizer. Since this IMD is not generated by the power bank, its interaction in the feedforward cancellation process is not predictable, and it will usually appear undiminished at the output of the linearizing stages. Thus, the internally generated distortion limits the amount of IMD cancellation that the linearizer can provide.

Although the power-bank linearizer is effective in reducing intermodulation distortion, the harmonic performance can be degraded as a result of harmonic distortion originating in the adaptive weights. Observed IMD cancellation is on the order of 20 dB per stage (as expected), except where it is limited by IMD generated within the linearizer. Research effort is currently under way for the development of active weights, ferrite-core transformers, and couplers having improved distortion performance, so that the power-bank linearizer may be optimized.

The report makes recommendations for further test measurements to be performed and suggests making the linear power bank hardware developed thus far a permanent part of a test bed for further research.

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INTRODUCTION

As a backup and an alternative to satellite communications systems, the Navy, through its High Frequency Improvement Program (HFIP), is placing increased emphasis on high-frequency (HF) radio as a means of supporting command, control, and communications requirements. This report describes the effort and results to date in the development of a critical component of the HFIP wideband system, the linear wideband HF power bank.

First, the report briefly reviews the Navy's present HF system architecture in order to compare its capabilities with objectives that have been established for a wideband system architecture for HFIP. Next, the report presents an overview of portions of the wideband transmitting subsystem. Finally, the report focuses on the development of an adaptive, feedforward, linear, wideband HF power bank (linear power bank) that has an unusually linear power amplifier (the power bank), and it describes adaptive techniques (the power-bank linearizer) that have been applied to further reduce noise and distortion-product levels at the transmitting-subsystem output.

Present U.S. Navy HF System Architecture

Conventional shipboard HF communication systems, shown in Fig. 1, accommodate collocated transmitting and receiving functions by means of filtering techniques. Careful frequency management and the use of narrowband filtering provided by transmitting multicouplers, base tuners (under development), receiver multicouplers, and intermediate frequency (IF) filters help limit electromagnetic interference (EMI) to tolerable levels. This conventional approach deals with the collocation problem but limits HF communication circuits to frequency separations of about 5% and narrow bandwidths of about 1% of each operating frequency. It is not readily compatible with new operational requirements for communication systems having antijam (AJ) capability. Furthermore, the ability of the conventional communication system to change operating frequency quickly is poor because of the time required to tune the mechanically sluggish and complex high-power switch matrices, multicouplers, and base tuners.

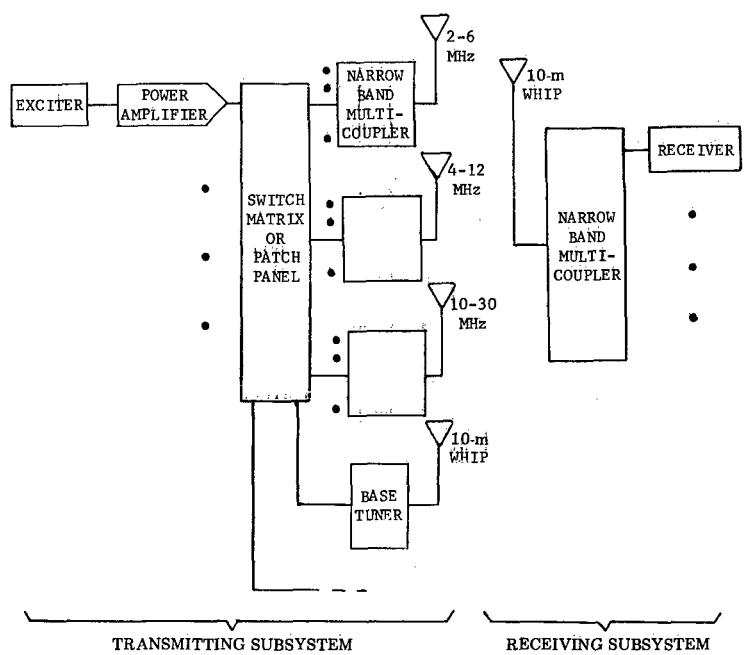

Fig. 1 — Conventional narrowband shipboard HF architecture

New Wideband HF Architecture

To meet the operational requirements of full-duplex, AJ, and rapid-frequency-change capability, a new wideband HF architecture is being developed. A description of the architecture has been given [1], a risk analysis for the major elements constituting the system has been performed [2], and a test facility has been established [3]. Alternative potential architecture implementations have been described [4].

The new architecture has three prominent features:

- The full HF spectrum is available to all users at all times;
- The rapidity of frequency change is limited only by synthesizer settling time and the settling time of adaptive circuitry; and
- The minimum separation between transmitting frequencies or between transmitting and receiving frequencies is limited only by synthesizer phase noise. (It is estimated to be about 2.5% or 100 kHz, whichever is larger.)

These features are achieved through the elimination of narrowband, mechanically tuned RF filters in the transmitting and receiving subsystems in order to provide compatibility with wideband signal structures and frequency agility. Figure 2 shows the essential features of the new architecture.

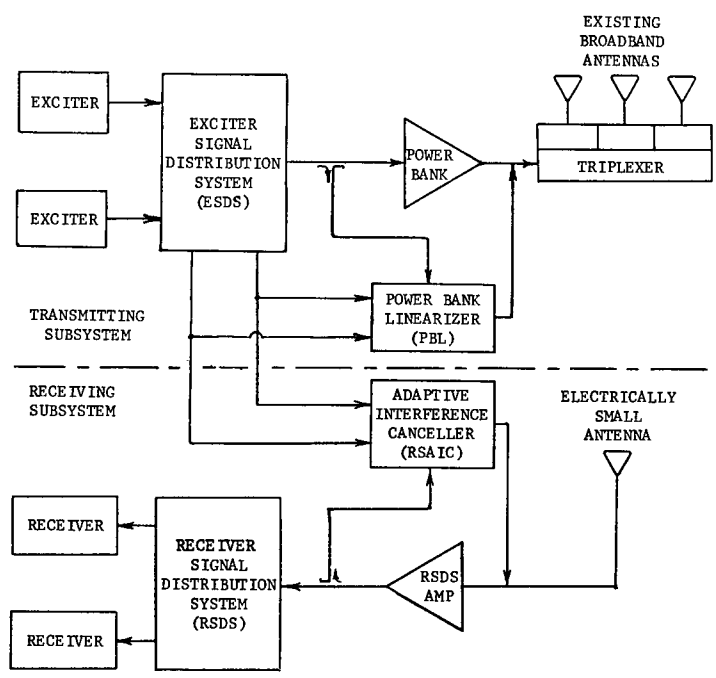

Fig. 2 — Wideband HF architecture

The receiving subsystem [5] includes an appropriately sited, electrically small antenna driving a broadband amplifier followed by a passive power-divider network that distributes signals to multiple receivers. The amplitudes of fundamental signals that originate in the transmitting subsystem and couple to the collocated receiving antenna are controlled by antenna design and arrangement [6], and these

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signals are cancelled at the input to the amplifier by the receiving-subsystem adaptive interference canceller (RSAIC) [7-10]. Reference signals for operation of the RSAIC are obtained from the exciter signal-distribution subsystem (ESDS).

The transmitting subsystem consists of a number of agile exciters, having exceptionally low noise and distortion, which drive a linear power bank via the ESDS. The function of the ESDS is to combine the exciter signals and to distribute appropriate reference signals that are used in the RSAIC and the power-bank linearizer (PBL) to reduce distortion. The linear-power-bank output is distributed to existing broadband transmitting antennas by a passive triplexer network, and in the future it may be directly connected to new wideband transmitting antennas under development [11].

The key portions of the linear-power-bank structure are the power bank and the power-bank linearizer. The objectives for the power bank and the linearizer operating as a system are for second- and third-order distortion levels of −116 dBc and a noise power density of −164 dBW/Hz [2] for signal output levels of 1 kW per fundamental. The hardware described in this report is for a system having an initial design goal of −116 dBc for distortion and −164 dBW/Hz noise power for signal output levels of 100 W per fundamental. The linearizer is designed to achieve this goal using three cascaded feedforward stages. Two of the three stages have been implemented into an operating system which accommodates two fundamental signals. The distortion design goal for two stages is −100 dBc.

The power bank for this report consists of a single HF linear amplifier developed for NRL under contract by Westinghouse Electric Corporation (Contract N00173-79-C-0483) and the power-bank linearizer consists of hardware developed under contract by Zeger-Abrams Incorporated (Contract N00173-78-C-0238).

POWER BANK

The power bank (HF linear amplifier—shown in Fig. 3) developed by this effort represents a significant step forward compared to typical contemporary amplifier performance. Radio-frequency (RF) power is generated by a main amplifier which in itself is very linear, and the distortion performance of this main amplifier is then further improved by the operation of a feedforward canceller. Figure 4 shows a block diagram of the linear amplifier. The output power is generated by eight power-amplifier (PA) modules within the main amplifier. The phase of the signals amplified by each of the four pairs of PA modules is maintained in a quadrature relationship. All blocks other than the main amplifier in Fig. 4 are associated with the feedforward canceller.

Another notable feature of the linear amplifier is that it generates a 500-W output without any tuning adjustments. The linear-amplifier design can be expanded from 500 W to 4000 W. For reasons of economy the 500-W version was constructed.

The linear amplifier operates broadband from 2 to 30 MHz. The amplifier is fully stable and will operate connected to any type of load with a voltage standing-wave ratio (VSWR) range from one to infinity over this frequency range. Operation is Class A and the overall efficiency, excluding losses in the power supply, for 500-W (one-tone output) peak envelope power (PEP) is 9.4%. The noise power generated by the amplifier is equivalent to a noise figure of better than 18 dB. With some small increase in complexity this could be improved. Table 1 gives a brief summary of the linear-amplifier performance.

Distortion

The most difficult and important aspect of performance, linearity, is specified to be far better for the linear amplifier than anything normally attainable with existing tube or transistor amplifiers. It is specified in terms of third-order intermodulation products (the worst distortion products) generated by

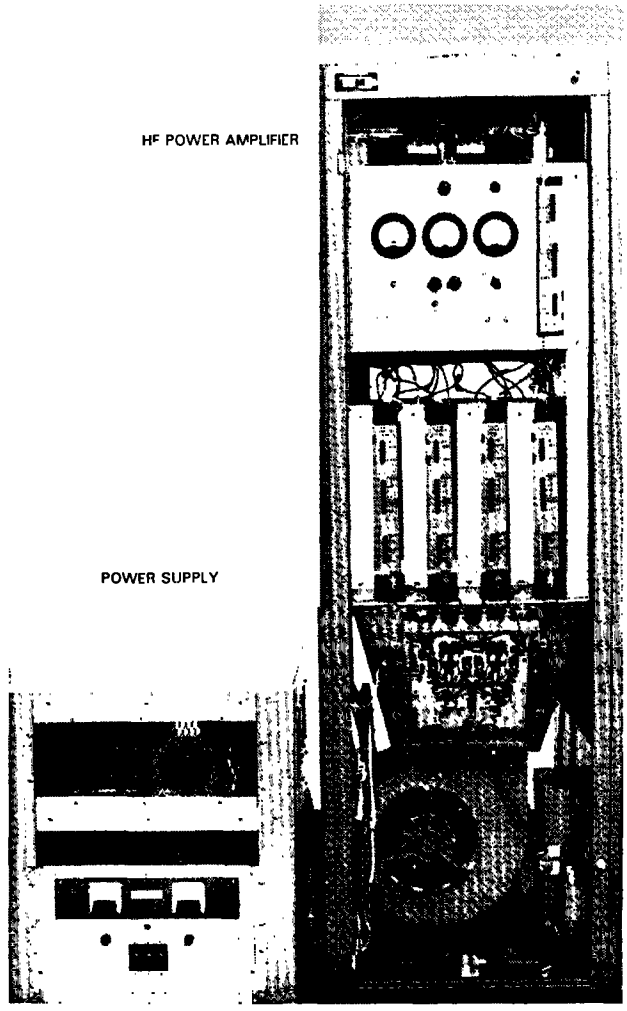

Fig. 3 — HF power amplifier and power supply

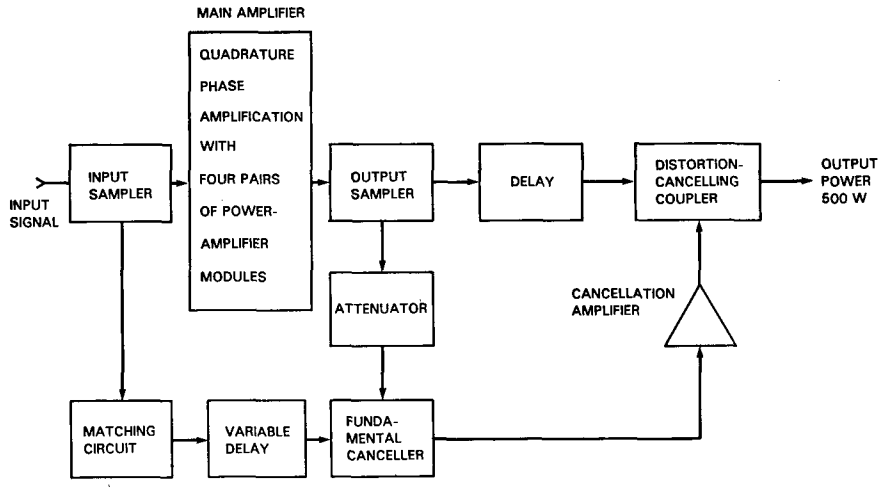

Fig. 4 — Linear amplifier showing power generation and linearization

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Table 1 — Linear Amplifier Performance Summary

Characteristic	Goal	Performance
Frequency Range	2-30 MHz	2-30 MHz
Output Power (peak envelope and average)	500 W	500 W
Intermodulation Products (third order)	−70 dBc	2-10 MHz, −74 dBc 10-25 MHz, −60 dBc 25-30 MHz, −54 dBc
Output Noise Power Spectral Density	−163 dBW/Hz	−160.8 to −156.0 dBW/Hz
Gain		28.75 dB
Gain Flatness		0.75 dB
Input VSWR (relative to 50 Ω)		1.2
Efficiency (for one-tone rated PEP output)	8%	9.4%
Load VSWR (relative to 50 Ω)		4
DC Power		5320 W

the amplifier from two equal fundamental signal tones with a combined output power equal to the maximum PEP of 500 W. With two equal tones generated to yield 500-W PEP (i.e., 125 W per tone), all harmonics and intermodulation products are required to be less than either tone by 70 dB (or −70 dBc). Table 2 shows the maximum levels of third-order in-band intermodulation products generated under these conditions by the linear amplifier. Each of the two tones listed has a power of 125 W (equivalent to 500-W PEP). As shown, a level of −74 dBc is achieved with two tones at the low end of the frequency range, and −54 dBc at the high end. The third-order products listed in Table 2 are difference products, i.e., they are formed at frequencies $2F_1 - F_2$ and $2F_2 - F_1$, where F_1 and F_2 are the frequencies of the two fundamental-signal tones.

Table 2 — Maximum Third-Order Distortion-Product Levels

Frequencies of Fundamental Tones (MHz)	Level of Third-Order Products Relative to 125 W (dBc)
2 and 2.3	−74
10 and 11	−70
28 and 30	−54

An unusual property of the linear amplifier is its ability to suppress the generation of third-order sum products ($2F_1 + F_2$ and $2F_2 + F_1$) and third harmonics. Table 3 compares third-order sum products, third-order difference products, and third harmonics. As can be seen, the third-order difference products are the largest. In effect, the amplifier not only has outstanding linear performance as measured by the levels of third-order difference products, but also, due to its unique balanced amplification technique, it suppresses the generation of many other products and harmonics.

Table 3 — Suppression of Third-Order Sum Products and Third Harmonics

Fundamental Tones (each at 125 W) (MHz)	Third-Order Difference Products (dBc)	Third-Order Sum Products (dBc)	Third Harmonics (dBc)
2 and 2.3	−74	−88	−90
4.8 and 5.5	−75	−88	−85
8 and 11.3	−68	−78	−78
2 and 22.6	−79	−87	−88

To achieve the linearity expressed by Tables 2 and 3, the following techniques are employed:

- Four-phase balanced amplification;
- Feedforward cancellation;
- Quadrature hybrid output-power combination;
- Vertical-metal-oxide semiconductor field-effect transistors; and
- Negative feedback.

Detailed explanations of the operation of each of these techniques follow.

Four-Phase Balanced Amplification

Four phases of the input signal in quadrature with each other are amplified separately and combined in the output. In contrast to a push-pull balanced amplifier (two phases), this technique cancels not only all even-order products, but also a large number of odd-order products. The products cancelled in this manner (for two-tone operation) include second-, third-, fourth-, sixth-, seventh-, eighth-, and tenth-order harmonics and intermodulation-distortion products. Some particular types of difference intermodulation products are not cancelled.

Figure 5 shows the main amplifier in more detail. The phase relationship of the signals to be amplified is shown by the angles 0, $\pi/2$, π, and $3\pi/2$ at the input to each pair of PA modules. As depicted, the input signal is split into two equal-amplitude signals, $\pi/2$ radians (90°) apart in phase, by the input quadrature hybrid and delivered to a pair of input amplifiers. Within the input amplifiers the two signals are separately amplified and then divided equally by hybrids that shift each signal by a further 0 or π radians. The result at the outputs of the input amplifiers is four equal-amplitude signals bearing a quadrature phase relationship of 0, $\pi/2$, π, and $3\pi/2$.

These signals are split once again (in phase) to provide the necessary drive for each of the eight PA modules. After separate amplification by the PA modules, the outputs are combined. The combination process cancels (by balancing) many odd-order and all even-order harmonics and intermodulation products. Figure 6 shows the improvement due to this technique for one class of third-order intermodulation products. In Fig. 6, the level of the product formed from $2F_2 + F_1$ (a cancelled product) is compared with the level of the product $2F_2 - F_1$ (an uncancelled product). The improvement varies from 10 dB to 16 dB over the frequency range. Similar or larger improvements are observable for other products and harmonics, including second, third, fourth, sixth, seventh, eigth, and tenth orders.

Figure 7 shows the output spectrum from 0 to 20 MHz of the four-phase balanced amplifier, when the amplifier is driven by two tones at 2.0 and 2.3 MHz, for an output-power level of 500-W PEP at 125-W (0 dBc) per tone. The two third-order difference products ($2F_1 - F_2$ and $2F_2 - F_1$) at 1.7 and 2.6 MHz are at a level of −42 dBc. Second-order products are not visible, but third-order sum products ($2F_1 + F_2$ and $2F_2 + F_1$) are shown at frequencies of 6.3 and 6.6 MHz at a level of about −53 dBc, 11

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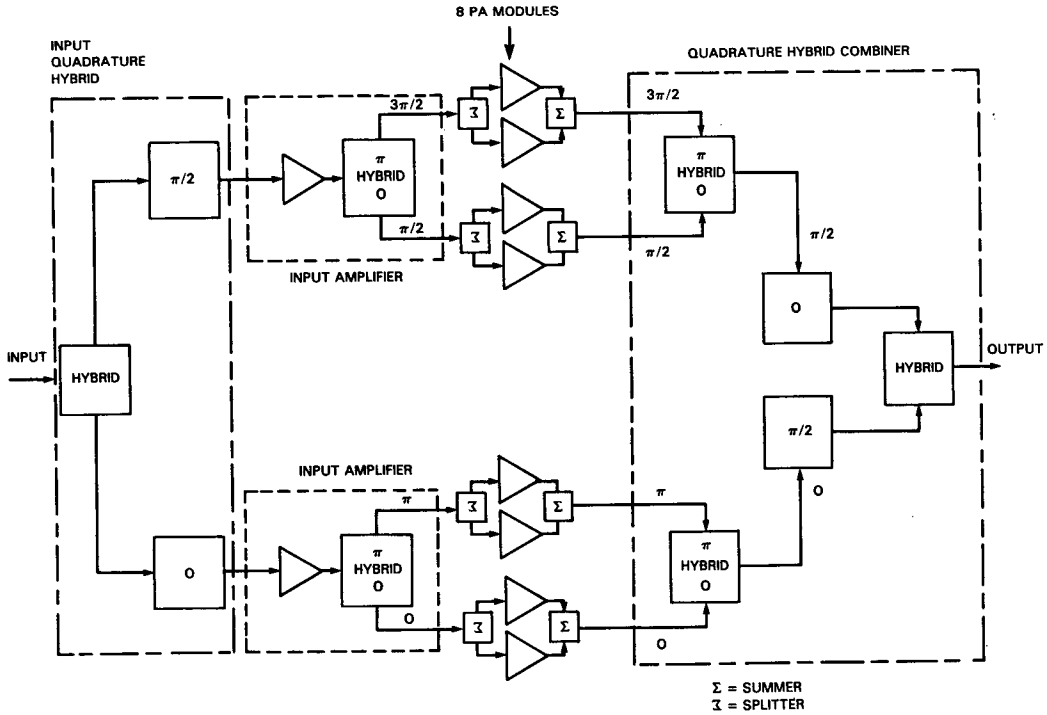

Fig. 5 — Main amplifier

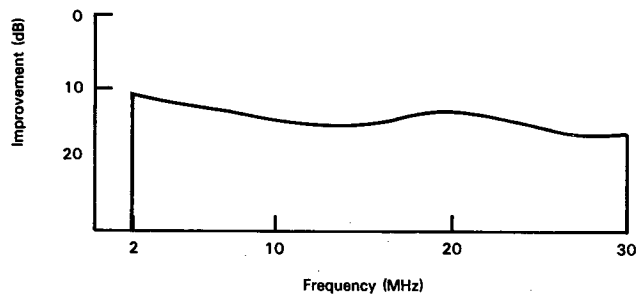

Fig. 6 — Improvement in third-order products ($2F_2 + F_1$ compared with $2F_2 - F_1$) due to four-phase balancing

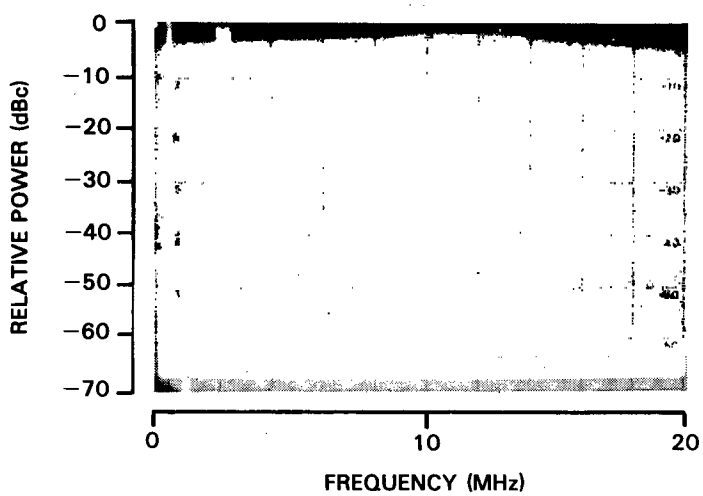

Fig. 7 — Distortion performance with four-phase balancing for two tones at 2.0 and 2.3 MHz (500-W PEP)

dB below the third-order difference products due to the four-phase balancing action. Fourth-order products are balanced beyond measurement range and are not visible. Fifth-order products grouped between 10 and 12 MHz are not balanced and are clearly visible.

A general analysis of multiphase balanced amplifiers and the improvements that result therefrom is given in Ref. 12.

Feedforward Cancellation

Feedforward cancellation applied to the output of the main amplifier is a second method used to reduce distortion products. This method of improving linearity is a technique recently applied to high-power amplifiers. Implementation of the feedforward technique provides about 30-dB distortion reduction at 2 MHz and 15-dB reduction at 30 MHz.

Figure 8 shows a simplified block diagram of the linear amplifier, highlighting the feedforward cancellation circuit. The canceller consists of two separate but overlapping loops, Loop 1 and Loop 2. Loop 1 is used to obtain a sample of the distortion, originating in the main amplifier, that is not dominated by the presence of the fundamental signal components. Loop 2 amplifies the distortion sample and injects it into the output of the main amplifier at the same amplitude but 180° out of phase with the distortion generated in the main amplifier. If the second loop is appropriately equalized, cancellation of distortion is achieved over a very wide bandwidth. Detailed operation of the linear amplifier is described in the following paragraphs.

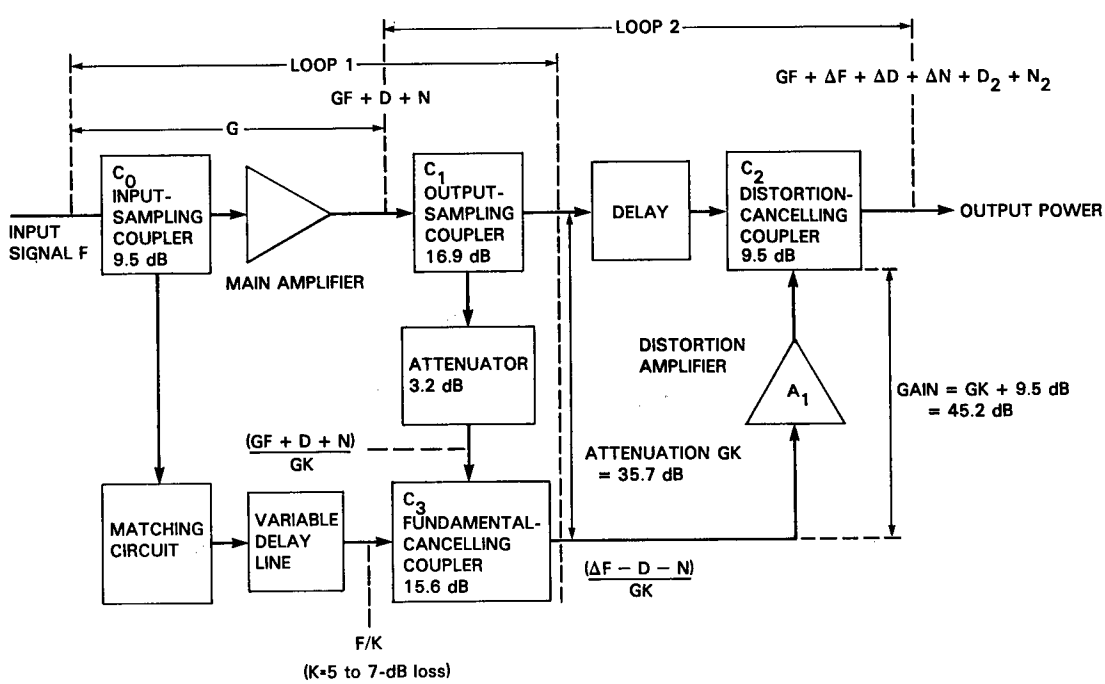

Fig. 8 — Basic feedforward canceller

We obtain a sample of the input signal F by the use of coupler C_0 with a 9.5 dB coupling factor. This sample of the input signal F is sent to the main amplifier and is amplified to a level GF, where G is the overall gain of the main amplifier. Additionally, distortion power D and noise power N are generated by the main amplifier, contaminating the output signal. As a result, the output is $GF + D + N$.

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The remainder (the larger portion) of the input signal from C_0 is sent to the fundamental cancelling coupler C_3 via a set of matching circuits and a variable delay line, and it is injected into C_3 at a level of F/K.

A sample of the output from the main amplifier is taken by the output sampling coupler C_1 and sent to the fundamental-cancelling coupler C_3. To facilitate cancellation of the fundamental signal in C_3, the output sample is suitably attenuated and the input sample is amplitude-matched to the response of the main amplifier and delayed to match the time delay of the output sample. Due to unavoidable imperfections in the matching process caused by various effects, including reflection from the load, the output of C_3 contains a small residue $\Delta F/K$ of fundamental signal. The output of C_3 is also the output from Loop 1 and it is represented by $(\Delta F - D - N)/GK$.

The output of Loop 1 is a sample of the distortion generated by the main amplifier and is fed to Loop 2, where it is amplified by the distortion amplifier A_1 and then injected into the main line by the distortion-cancelling coupler C_2 to cancel the distortion and noise components $(D + N)$ on the main line. This is also an imperfect process, and it leaves residues denoted by $\Delta D + \Delta N$. Further, amplifier A_1 generates distortion products from the fundamental residue ΔF applied to the input and, also, by power reflected from the load into its output circuits. The sum of these distortion products is denoted by D_2. The distortion products D_2 and noise power N_2, generated in A_1, are not cancelled and will appear in the main-line output of the linear amplifier. The output of the distortion-cancelling coupler C_2 can therefore be denoted by

$$GF + \Delta F + \Delta D + \Delta N + D_2 + N_2.$$

The total attenuation of the output sample is the sum of the attenuation of the directional couplers C_1 and C_3 and the 3.2-dB attenuator; this is the attenuation GK, equal to 35.7 dB, as shown in Fig. 8. The maximum power level injected into C_3 is therefore 500 W divided by the power ratio equivalent to 35.7 dB, i.e., −8.7 dBW. The cancellation achieved in Loop 1 varies across the frequency range and is always better than 26 dB. Of the three signal components, ΔF, D, and N, appearing at the output of the fundamental-cancelling coupler C_3, i.e., at the input to the distortion amplifier A_1, ΔF is generally the largest in amplitude. The largest signal likely to be injected into A_1 is, therefore, −8.7 dBW minus 26 dB, or −34.7 dBW. For the distortion products to cancel in the distortion-cancelling coupler C_2, A_1 needs a gain of 35.7 plus 9.5 dB, since C_2 has a coupling factor of 9.5 dB. The maximum output power of A_1 is therefore −34.7 dBW plus 35.7 dB plus 9.5 dB, or 10.5 dBW. This is the peak envelope power delivered by A_1.

The amplitude of the fundamental-signal residue ΔF appearing at the output of Loop 1 is important, as it directly affects the power-handling capability of A_1. The better the balance of the two signals fed into C_3, the smaller the size of the residue ΔF and the smaller the amplitude of the distortion products generated by A_1. Ideally, the amplitude of residue ΔF would be smaller than the amplitude of the largest distortion component in D.

With reference to Figs. 5 and 8, the parts of Loop 1 which have a significant effect on the amplitude and phase matching of the input sample F/K and the output sample $(GF + D + N)/GK$ fed into the fundamental canceller are as follows:

- The main amplifier;
- The quadrature hybrids (one located at the input immediately preceding the main amplifier, the other combining the output of each half of the main amplifier);
- The directional couplers (for coupling a sample of the output and the fundamental canceller);

- The variable attenuator (within matching circuits); and
- The variable delay line.

Any variation in the load VSWR will also have a significant effect on the amplitude and phase matching of the input sample F/K to the output sample $(GF + D + N)/GK$. The effects of load VSWR variation are mitigated by the use of a quadrature output combiner. This is dealt with later.

The relationships between amplitude and phase transfer characteristics and the degree of cancellation achieved are shown in Fig. 9. Figure 9 depicts contours of equal cancellation, $\Delta F/A_1 = 29$ dB, 26 dB, etc., as a function of amplitude and phase mismatches of two signals: $F_0 = A_0 \cos \omega t$ and $F_1 = A_1 \cos (\omega t + \phi)$. The effects of amplitude mismatch between the two signals fed into the fundamental canceller are shown by the intersection of the cancellation contours with the ordinate of the graph. The effects of phase mismatch are similarly shown along the abscissa.

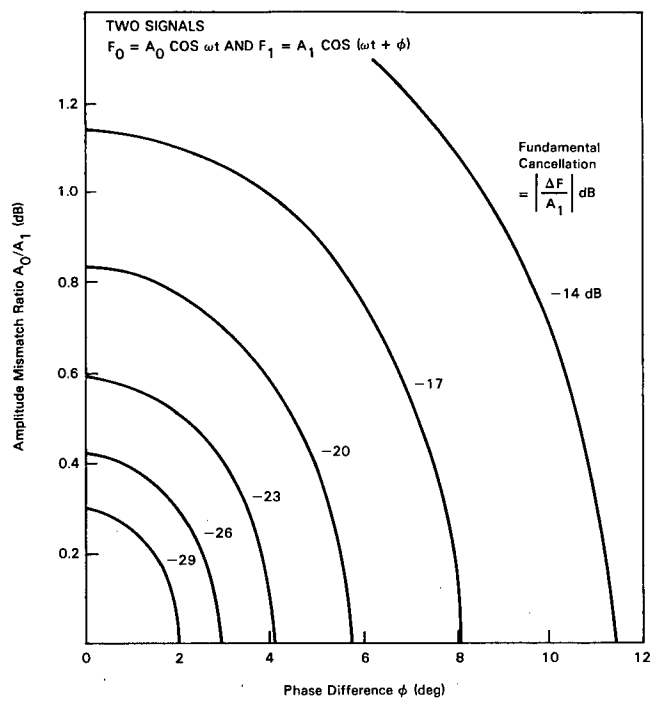

Fig. 9 — Amplitude and phase mismatches affecting cancellation of fundamental signal

Amplitude matching is governed primarily by the frequency response of the main amplifier, but the passive components in Loop 1 have a small effect. Matching phase responses is complicated by the effect of the quadrature hybrids at the input and output of the main amplifier.

The matching circuits shown in Fig. 8 are used to compensate for the amplitude and phase responses and provide matches of better than 0.5 dB and 3° into the fundamental canceller. This amount of matching allows more than 26 dB of fundamental cancellation across the 2- to 30-MHz range.

The distortion products appearing in the output of A_1 following the distortion-cancelling coupler C_2 are shown in Fig. 8 as ΔD and D_2. These are produced by separate mechanisms. The component ΔD is the residue resulting from imperfect cancellation of the distortion products D generated by the

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main amplifier. The component D_2 is composed of distortion generated by three different sources. First, distortion is generated by A_1 from the application of the fundamental signal residue ΔF to its input terminals. This is a forward intermodulation effect. Second, distortion is generated by C_2. And third, distortion is generated by the action of power reflected from the load (i.e., reverse power) being coupled into the output circuits of A_1. This is sometimes termed reverse or "backdoor" intermodulation.

Figure 10 shows the output spectrum from 0 to 20 MHz after feedforward cancellation for two tones at 2.0 and 2.3 MHz with a combined power level of 500-W PEP. The feedforward canceller has reduced third-order difference products at 1.7 and 2.6 MHz to levels of −78 dBc and −74 dBc, respectively, a 30-dB improvement over the levels shown in Fig. 7. All other products have been reduced below −80 dBc. This spectrum shows clearly the excellent performance of the linear amplifier at the low end of the frequency range. The effective dynamic range of the spectrum analyzer used to create Fig. 7 is improved by 30 dB when notch filters are used to decrease the levels of the 2.0- and 2.3-MHz fundamental signals. (The noise floor is −65 dBc in Fig. 7 and −95 dBc in Fig. 10.)

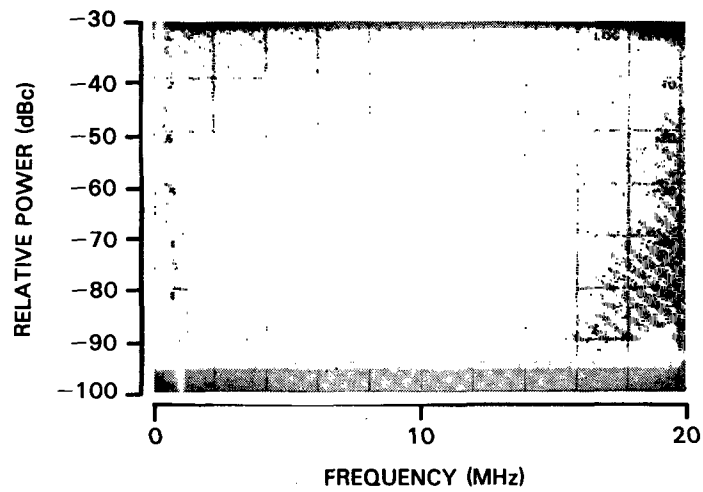

Fig. 10 — Distortion performance after feedforward cancellation for two tones at 2.0 and 2.3 MHz (500-W PEP)

Quadrature Hybrid Output Power Combination

As shown in Fig. 5, final power combination is made with a quadrature output combiner. This type of combination preserves the improvements in linearity obtained by feedforward cancellation when the linear amplifier is operated into a transmission line with a VSWR greater than one.

Quadrature combination, with its attendant advantage of absorption of reflected power, would not be required if the output stage of the main amplifier could be designed to match the characteristic impedance of the output transmission line exactly. All reflected power would be absorbed in the output of the amplifier, and there would not be any further reflections. Since it is difficult even to approach a matched condition with the amplifier output impedance, doubly reflected power will always be present and it can be significant. Its effect is to change the incident power on the line and upset the amplitude- and phase-matching of Loop 1. The quadrature hybrid combiner in the output of the amplifier is used to make this effect negligible by matching output impedance to the line as nearly as possible.

The amplitude of the doubly reflected signal is dependent on the amplitude and phase of the reflections from each end of the line due to VSWR conditions existing at the load and amplifier ends of the transmission line. This amplitude is given by a converging series,

$$A_{dr} = |PA + P^2A + \ldots|,$$

where A_{dr} is the amplitude of the doubly reflected signal after the steady state condition is achieved, A is the initial amplitude of the incident or forward signal, and P is the product of the load and generator impedance reflection coefficients (including phase shift due to line length). Depending on the electrical length of the line and the phases of the reflected signals, A_{dr} can vary up to a maximum value equal to the sum of all the terms in the above series (when all the terms have the same phase).

The term *doubly reflected signal* is used herein to include the effects of all contributions represented by each term in the series. These contributions are generated as a result of two, four, six, eight, etc. reflections, i.e., an even number of reflections, hence the term doubly. To reduce the doubly reflected voltage component, the main amplifier is constructed in two halves which are driven 90° out of phase. Combination of these two halves is by a quadrature hybrid. The quadrature hybrid combiner is shown in simplified form in Fig. 11.

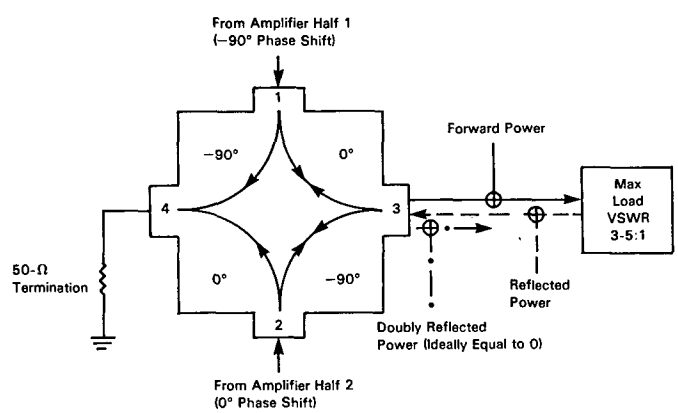

Fig. 11 — Output quadrature hybrid

The output power from the two halves of the main amplifier is fed into Ports 1 and 2 in quadrature phase. The signals fed into Port 2 are delayed 90°, matching the delay of the signals fed into Port 1, and these two signals combine at Port 3 and flow to the load. With a perfect load (VSWR = 1) none of the signal is reflected and there is no power coupled to Port 4. If the load is mismatched and if, further, the source impedances of the amplifier halves do not match the line impedance, but nevertheless have output impedances equal to each other, then the following conditions occur. Power reflected from the load incident at Port 3 is coupled equally to Ports 1 and 2. At Ports 1 and 2, this power is partly absorbed and the remainder is reflected equally toward Ports 3 and 4. Power from Port 2 is subjected to two additional 90° phase shifts and arrives at Port 3 with a phase lag of 180°, as compared with the power from Port 1. Therefore, these two equal-amplitude but opposite-phase signals cancel at Port 3. Power reflected from Port 1 toward Port 4 is subjected to a 90° phase lag; this is the same phase lag that is incurred by the power reflected from Port 2 to Port 4. These two signals of equal power are therefore in phase and add at Port 4, where they are completely absorbed by the 50-Ω termination. None of the doubly reflected power ever reemerges at Port 3. The effect is to have an amplifier created that absorbs all the power reflected from the load; that is, the amplifier's output is matched to the characteristic impedance of the line.

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Vertical-Metal-Oxide Semiconductor Field-Effect Transistors

Vertical-metal-oxide semiconductor (VMOS) field effect transistors (FETs) are selected for the linear amplifier, instead of bipolar transistors, chiefly because of their better linearity. Compared to bipolar transistors they have superior distortion characteristics, especially for high-order distortion products. VMOSFETs also possess other advantages, which are summarized as follows:

- They are not subject to thermal runaway: Output current decreases with temperature, thus preventing thermal runaway. As a result, operation is simple and safe, and device-balancing resistors (to prevent thermally induced destruction) are not required.

- They are free from secondary breakdown: Only power dissipation considerations govern the choice of operating parameters.

- They provide low-noise power generation: They have excellent noise figures. High-power FETs have noise figures comparable to those of low-power, small-signal bipolar transistors.

- They have charge-storage delay times near zero: The electrical length of FETs is short; thus, they are suitable for high-frequency operation and can be used in feedback-amplifier circuits, where phase shift at high frequency is important.

- They have high gain and large bandwidth: The device has relatively low capacity and high transconductance, so that circuit design is simple and large bandwidths beyond 30 MHz are easily obtained.

- They operate into any load: They can operate into any VSWR load without harmful effects.

The particular FET chosen is the DV2880 made by Siliconix. Operated in a circuit with 11 dB of feedback at a level of 16-W PEP and an efficiency of 23%, two-tone performance provides third-order products that are −50 dBc at the low end of the frequency range and −40 dBc at the high end of the frequency range.

Negative Feedback

Two-stage negative feedback is used in the PA modules to improve the linearity of the output stages. Negative feedback is effective for frequencies below 20 MHz, and about 8 dB of improvement in linearity is obtained at 2 MHz. A mixture of voltage and current feedback is used, as shown in Fig. 12. Voltage or shunt feedback has the effect of reducing input and output impedance levels. Current or series feedback raises input and output impedances.

Two-stage feedback, although highly desirable, is difficult to employ if the feedback signal is derived from the load. To achieve an appreciable degree of feedback, the phase of the feedback signal must be controlled well above 30 MHz, where the very high frequency characteristics of the load are now very important. The phase of such a feedback signal is dependent on the characteristics of the load and can adversely affect the stability of the PA module. The problem of load variability can be avoided by the use of a feedback signal developed from the source current of the output FET, as shown in Fig. 12, since the source current is unaffected by load variations. The performance of the DV2880 FET proves to be satisfactory in this circuit. When the amplifier is operated at a level of 16-W PEP per output FET, two-tone performance is such that third-order products are down to −50 dBc at the low end of the frequency range and −40 dBc at the high end.

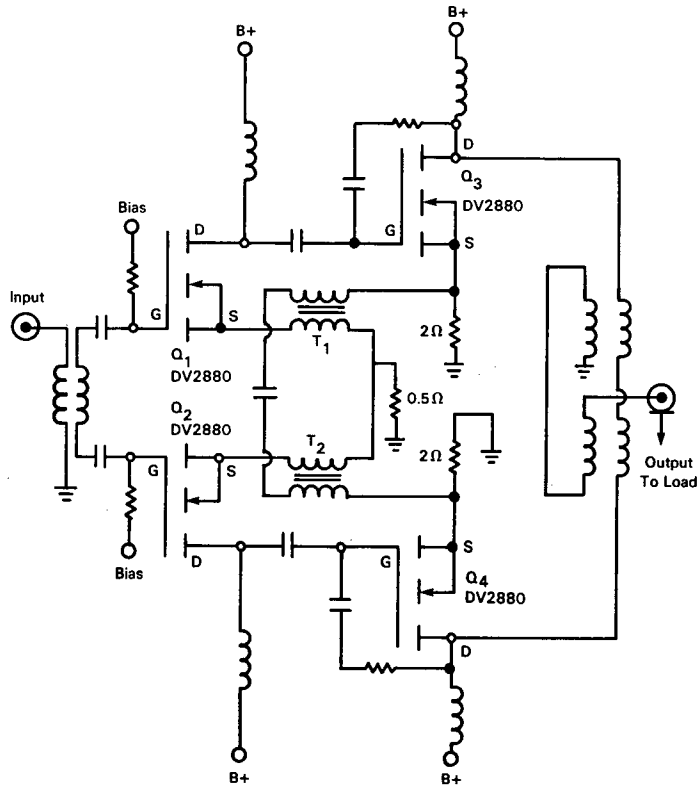

Fig. 12 — Two-stage feedback

The output impedance of the PA module varies from 236 Ω to 88 Ω over the 2- to 30-MHz frequency range. The circuit proves to be very stable and operates into loads of any VSWR with all conditions of phase. However, the overall efficiency of the output stage is low, because each output FET requires its own driver FET.

Noise

Noise power is generated by the linear amplifier from noise sources in the FETs. The noise power available at the output of the main amplifier is dominated by noise originating in its early stages, i.e., from the FET amplifiers in the PA modules. The noise signals generated by the main amplifier from noise sources in the FETs are cancelled in the main line, in a manner similar to the cancellation of the distortion products, leaving only a small noise residue. However, the distortion amplifier generates noise power of its own independently, and this is injected into the main line and is not cancelled. This noise power dominates over the residual noise. In effect, the noise generated by the distortion amplifier is substituted for that generated by the main amplifier. The resulting noise output of the linear amplifier is, thus, due to noise sources in the distortion amplifier plus residues of uncancelled noise from the cancellation process. Noise originating in the distortion amplifier from the FETs in its first stage of gain acounts for most of the noise power at its output. These FETs are type DV2880, the same as used elsewhere in the main amplifier. The noise performance of these FETs is, therefore, of particular interest and was measured early in the program. Based on these measurements, we can calculate the overall noise performance of the linear amplifier. A comparison of the predicted and measured noise performance of the linear amplifier is shown in Table 4. Detailed performance characteristics of the linear amplifier will be presented in Ref. 13.

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Table 4 — Actual and Predicted Noise Performance of Linear Amplifier

Frequency (MHz)	Predicted Noise Output (dBW/Hz)	Measured Noise Output (dBW/Hz)
2	−159.7	−156.2
10	−162.0	−158.9
30	−161.7	−160.8

POWER-BANK LINEARIZER

The major function of the power-bank linearizer is to reduce the intermodulation distortion (IMD) products at the power-bank output from a level as great as −60 dBc down to a level of −116 dBc. The performance objectives are given in Table 5.

Table 5 — Performance Objectives for Power-Bank Linearizer

Parameter	Objective
Frequency Range	2-30 MHz
Number of Fundamental Signals	Two—expandable to eight
Fundamental Signal Power Level	100-W PEP per signal
IMD	−116 dBc at output with up to −60 dBc at input
Settling Time	$<40\ \mu s$
Output Harmonic Level	Unspecified
Output Noise Level	−164 dBW/Hz
Fundamental Signal Insertion Loss	As small as possible
Load VSWR (relative to 50 Ω)	$\leqslant 4$

The linearization system is designed to achieve this goal using three cascaded feedforward stages, configured as shown in Fig. 13. The first stage is designed to reduce IMD to a level of −80 dBc, the second to a level of −100 dBc, and the third to a level of −116 dBc. Two of the three stages have been implemented in an operating system that accommodates two fundamental signals. The two stages are shown in Fig. 14. Note that the unused inputs and outputs on combiners and splitters in Fig. 13 are there to indicate the potential for expansion.

Each stage, as shown in Fig. 13, contains two feedforward cancellers, similar in many ways to the feedforward canceller used in the main amplifier. The major difference is that much-deeper fundamental-signal cancellation is obtained using adaptive, instead of nonadaptive, cancellation techniques.

Each stage consists of a feedforward fundamental-signal adaptive canceller (FSAIC), which optimizes cancellation at those frequencies where exciter signals are present, and a broadband, feedforward nonadaptive IMD canceller. The exciter signal-distribution system (ESDS) provides the FSAIC with individual exciter signals, as well as the combined signals, through a broadband power-bank equalizer

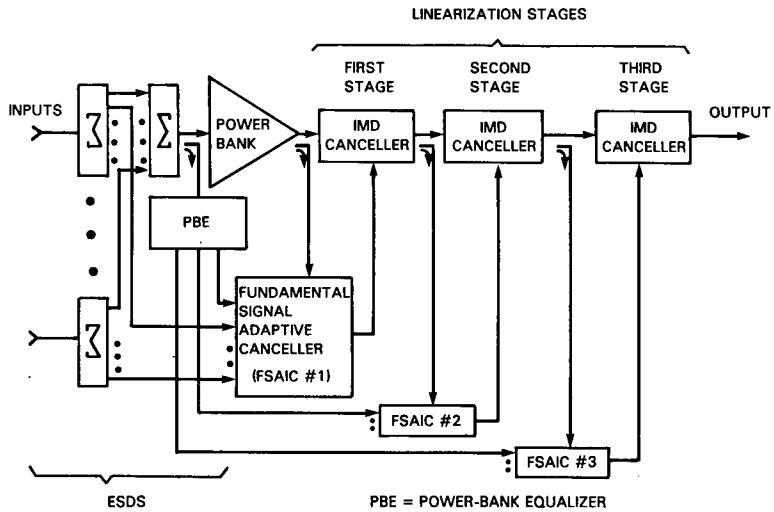

Fig. 13 — Power-bank linearization using cascaded feedforward stages

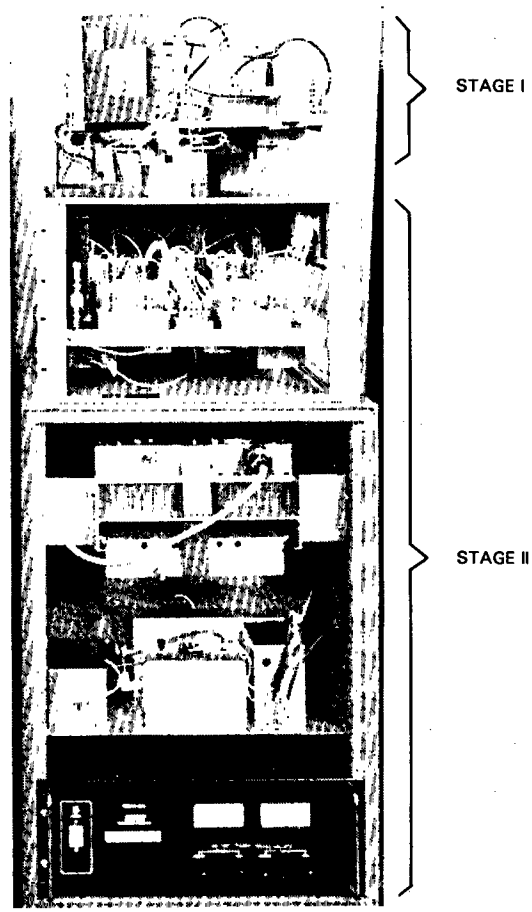

Fig. 14 — Power-bank linearizer consisting of two stages

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(PBE), whose amplitude and phase characteristics vs frequency match those of the power bank. The FSAIC is designed to cancel fundamental signals by at least 50 dB: 20 dB by use of the PBE and 30 dB by adaptive cancellation of the individual exciter signals. The high degree of fundamental-signal cancellation in the FSAIC is important in that it greatly eases the dynamic range requirement imposed on the amplifiers in the IMD cancellers.

Figure 15 shows greater detail in a single linearization stage and its system interfaces. The unused inputs and outputs on combiners and splitters are shown to indicate the potential for expansion. A portion of the power-bank output, extracted through the sampling coupler C_1, is combined in the fundamental-cancelling coupler C_3 with the PBE output, and the fundamental signal components are cancelled by at least 20 dB, but IMD remains uncancelled. Further cancellation of fundamentals occurs in coupler C_4, whose main-line input is the output of the FSAIC. The FSAIC output is a combination of adaptively weighted fundamental signals, where the adaptive weights provide both amplitude and phase adjustment of the signals flowing through them. The adaptive weights are set by feedback control that seeks to minimize the fundamental-signal components in the feedback error signal, thereby optimizing fundamental-signal cancellation in C_4. Note that each adaptive weight in the FSAIC handles only one fundamental signal, thereby allowing deep cancellation, because the signal bandwidth is relatively narrow, as well as preventing IMD generation in the adaptive weights. IMD generation in the adaptive weight is also suppressed by the unidirectional signal flow allowed by the isolator that follows each adaptive weight. However, fundamental-signal harmonics are generated in the adaptive weights. The IMD components remaining at the output of C_4 are amplified by amplifiers A_1 and A_2, and they are equalized by the feedforward equalizer (EQR), so that when injected into C_2 they cancel the IMD components flowing in the main line. In the IMD canceller, the delay cable, EQR, amplifier gains, and coupler values are selected so the IMD components that flow through the two paths from the input of C_1 to the output of C_2 undergo the same gain and phase shift in both paths across the 2- to 30-MHz range. The allowable amplitude and phase differences between the two signal paths are determined by the requirement to cancel IMD components in the main line by at least 20 dB (see Fig. 9) for each PBL stage.

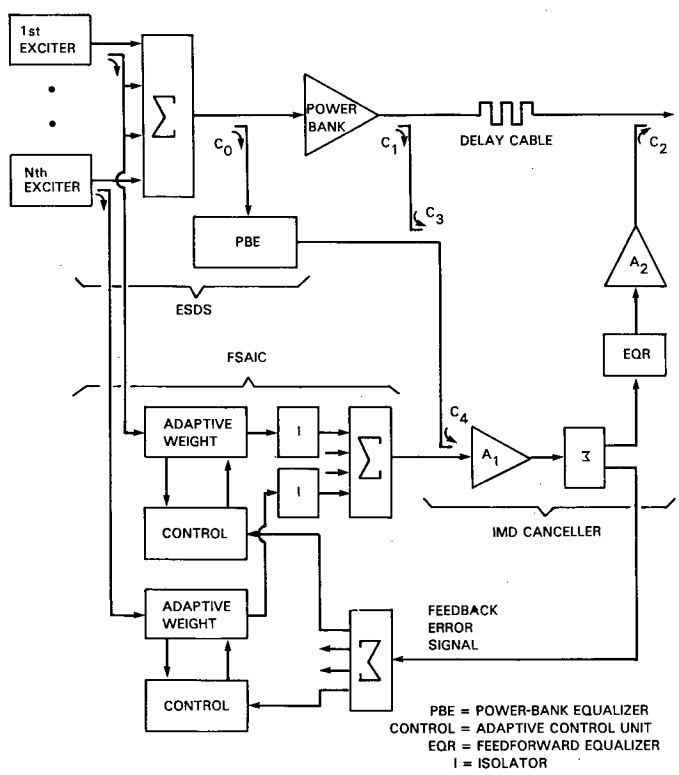

Fig. 15 — Detail of linearization stage and its system interfaces

Noise generated in the power bank is cancelled by the IMD canceller. In its place, noise generated in the IMD-canceller amplifier chain is injected into the output. The main factor that determines the output level of the injected noise is the gain from the input of A_1 to the output of C_2. This gain is equal to the coupler losses from the input of C_1 to the input of A_1. A reduction of these coupler losses would require an increase in the power to the FSAIC, which would cause a corresponding increase in the generation of harmonic distortion.

Table 6 summarizes the objectives, in terms of performance areas, and the system techniques used to achieve the desired performance. Performance results for the power-bank linearizer when used with the power bank are presented in the section entitled Performance Results.

Table 6 — Summary of Techniques Used in the Power-Bank Linearizer

Performance Area	Techniques Used for Performance Achievement
Large IMD Reduction	Cascaded feedforward broadband IMD cancellers
	Deep Adaptive fundamental-signal cancellation combined with nonadaptive feedforward broadband cancellation
	Separate adaptive weights for each fundamental signal
	Careful attention to IMD generation in ferrite devices
Fast Settling Time	Avoidance of tuned circuits
	Development of high-speed adaptive weight and control system
Low Output Noise	IMD cancellers also cancel power-bank noise
	Linearizer noise injection minimized by FSAIC operating at a high level without internal amplifiers

Power-Bank Equalizer

The PBE is shown in Figs. 13 and 15 as part of the ESDS. Its purpose is to allow at least 20 dB of cancellation in each linearization stage of samples of fundamental signals amplified by the power bank. To achieve that objective, the amplitude and phase vs frequency responses of the PBE must closely duplicate those of the power bank over the 2- to 30-MHz range.

Figure 16 shows the fundamental-signal cancellation performance achieved with the PBE, for Linearization Stages I and II, with a tone swept from 0 to 50 MHz. For Stage I, shown in Fig. 16a, approximately 30 dB of cancellation is achieved from 2 to 30 MHz (only 20 dB of cancellation is needed here). Figure 16b shows that the cancellation achieved for Stage II is at least 20 dB from 2 to 30 MHz.

Fundamental-Signal Adaptive Interference Canceller

The cancellation of fundamental signals provided by the PBE is further enhanced by the adaptive weights within the FSAIC. Each linearization stage contains an FSAIC, which contains one adaptive weight for each fundamental signal. The system is implemented for use with two fundamental signals,

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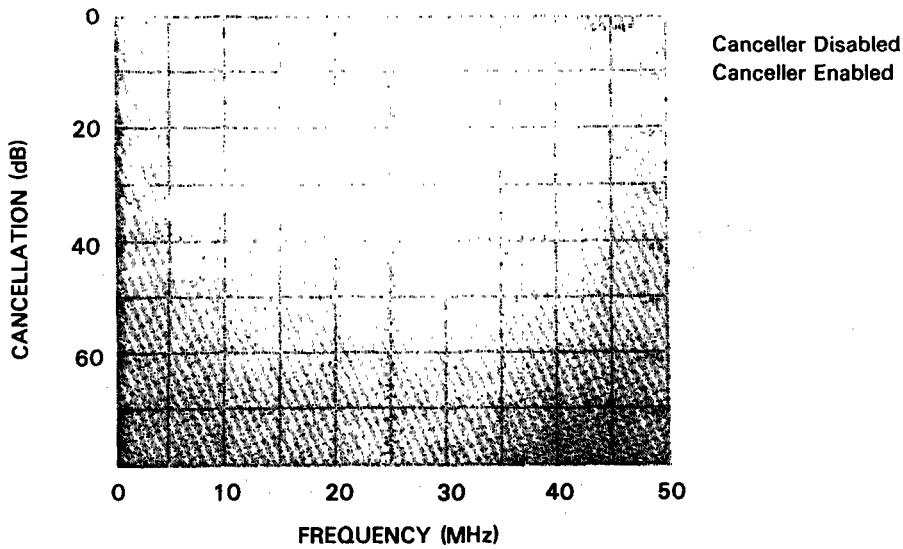
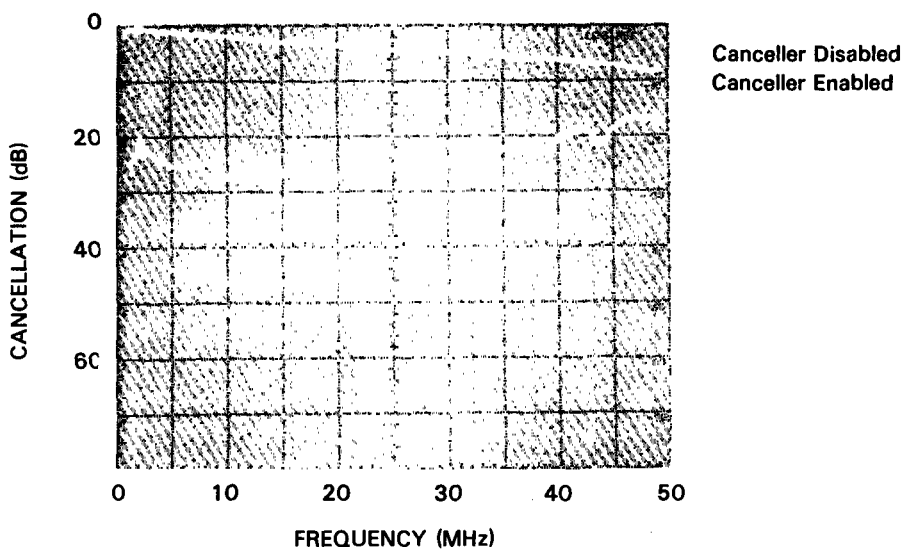


(a) Cancellation results of Linearization Stage I



(b) Cancellation results of Linearization Stage II

Fig. 16 — Fundamental-signal cancellation results with power-bank equalizer

and it can be easily expanded to handle eight fundamental signals. Figure 17 shows the adaptive weight and its least-mean square (LMS) control. The potential for expansion is illustrated by unused inputs and outputs on the combiner and the splitter, respectively. The adaptive weight is implemented by a quadrature hybrid, two balanced modulators, and an in-phase combiner. This implementation permits the adaptive weight to impose any amplitude and phase adjustment on its input signal, within the saturation limits of the balanced modulators. After the weight output is used for cancellation, a sample of the cancelled output is used as a feedback error signal. We obtain the W_I weight control voltage by correlating the in-phase component of the weight input with the error signal; we obtain the W_Q weight control voltage by correlating the quadrature component of the weight input with the error signal. The

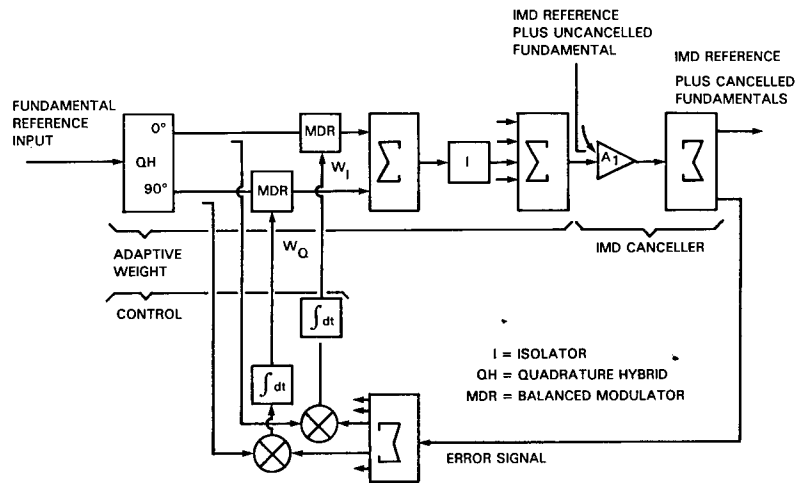


Fig. 17 — Detail of adaptive weight with LMS control

correlators are implemented by a mixer (or phase detector) followed by an integrator. This structure implements the LMS gradient control adaptive algorithm [14]. The modulators and control-loop time constants are designed for fast closed-loop responses in order to achieve an overall settling time of less than 40 μs.

Transient Response

The transient response of an LMS adaptive canceller to a sudden input change (transmitter turn-on or frequency hop) is exponential and converges to the steady-state condition with a time constant that is inversely proportional to the loop gain [14]. In theory, the transient response time (acquisition time) can be made arbitrarily short by the selection of a loop gain that gives a suitably short closed-loop time constant.

However, short time constants (or large loop gains) have certain detrimental effects on canceller performance. One such effect is the increased production of control-loop distortion products (described in the next section). Another is increased noise power at the canceller output [15]. This noise originates in the control-loop amplifiers and takes the form of multiplicative bandpass noise surrounding the cancelled fundamental signal. The noise bandwidth is approximately equal to the closed-loop bandwidth (the reciprocal of the closed-loop time constant) of the LMS loop. A final objection to the use of extremely short time constants is that in practical (nonideal) systems they can introduce instabilities leading to oscillations in the control loops. The requirements for FSAIC performance are sufficiently restrictive that no single time constant value can satisfy them all. Therefore, the control loop is designed to switch between long and short time constants, according to the current status of the canceller. If the canceller is in acquisition mode (the transmitter has just turned on or changed frequencies), the short time constant is selected to speed up the transient response. After the canceller has reached steady state (as defined by some specified depth of cancellation), the long time constant is switched in to provide reduced noise, reduced control-loop distortion-product generation, and enhanced stability. In this manner, the switched time constant combines the best features of both long and short time-constant values.

Distortion-Product Generation

Distortion products generated in the FSAIC constitute a threat to PBL performance, because they are not removed by feedforward cancellation and they appear at the system output. Hence, it is important that the distortion power produced by the adaptive canceller be kept sufficiently low so that it does not limit the achievable linearization of the power bank.

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The adaptive weights contain electronically adjustable attenuators (balanced modulators) that, by their nature, are much more apt to generate distortion than are fixed-value attenuators. Each weight operates on a single fundamental signal and produces distortion at harmonics of the fundamental frequency. Since the weight input consists of only one fundamental signal, IMD products are not expected at the weight output. Intermodulation distortion products can be generated in the weights, however, due to imperfect isolation of the weight outputs when they are combined. The weight outputs are summed by a hybrid combiner and, because of imperfect isolation in the combiner, some of the input from one port leaks around and flows in the reverse direction out of the other port toward the other weight. These reverse-flowing signals enter the weights and interact with the strong forward-flowing signals to produce IMD products. This reverse-signal IMD generation is suppressed in the PBL by an active reverse-signal isolator following each adaptive weight. The isolator, shown in Fig. 18, samples the signal from the main line entering the isolator in the reverse direction. This sample is inverted, amplified to make up for coupler losses, and then coupled back into the main line in the direction of the reverse-flowing signal in order to cancel the reverse-flowing signal. Equalization is included in the main-line path between the sample point and the injection point to compensate for the amplifier's delay response.

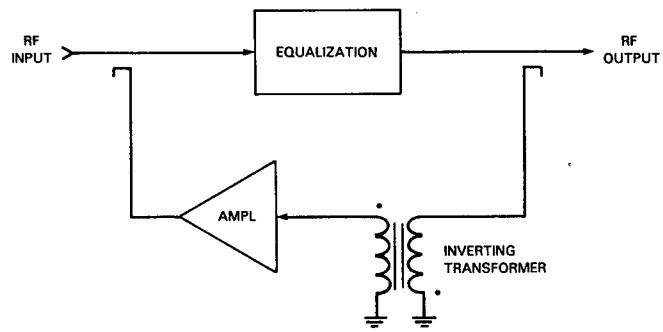

Fig. 18 — Reverse-signal isolator

The FSAIC can also generate IMD products in another way, which does not require any nonlinear component behavior in the canceller. This IMD generation is a consequence of the nonlinear nature of the LMS adaptive control system. Figure 19 illustrates the manner in which the FSAIC produces control-loop distortion products. Two fundamental signals are present at frequencies F_1 and F_2. Their separation $F_1 - F_2$ is defined as ΔF. The canceller error signal, common to both LMS loops, contains residues of both the F_1 and F_2 fundamentals. Thus, the output of the correlator (a multiplier followed by an integrator) for Loop 1 contains components at two frequencies, one at dc, from the correlation of the F_1 reference with the F_1 component of the error signal, and one at ΔF, from the correlation of the F_1 reference with the F_2 component of the error signal. The correlator output provides the weight control voltage for Weight 1; hence, Weight 1 is driven by a dc control voltage having a ripple at frequency ΔF superimposed on it. This ripple modulates the F_1 fundamental signal flowing into Weight 1, producing sidebands at $F_1 - \Delta F$ and F_2. Likewise, ripple in the Weight 2 control voltage modulates the F_2 fundamental, producing sidebands at F_1 and $F_2 + \Delta F$. These spurious sidebands travel through the loops to the FSAIC output. The sidebands at F_1 and F_2 are small compared to the fundamental residues at the output, and they do no harm. The sidebands at $F_1 - \Delta F$ and $F_2 + \Delta F$, however, are third-order difference IMD products that threaten to limit the achievable linearization of the power bank if their levels are too high.

As the fundamental separation ΔF is increased, the amplitude of control-loop IMD decreases, in accordance with the closed-loop low-pass filter function of the LMS loop, as defined for signals injected into the error path. It should be noted that the gain of the closed-loop filter function is proportional to

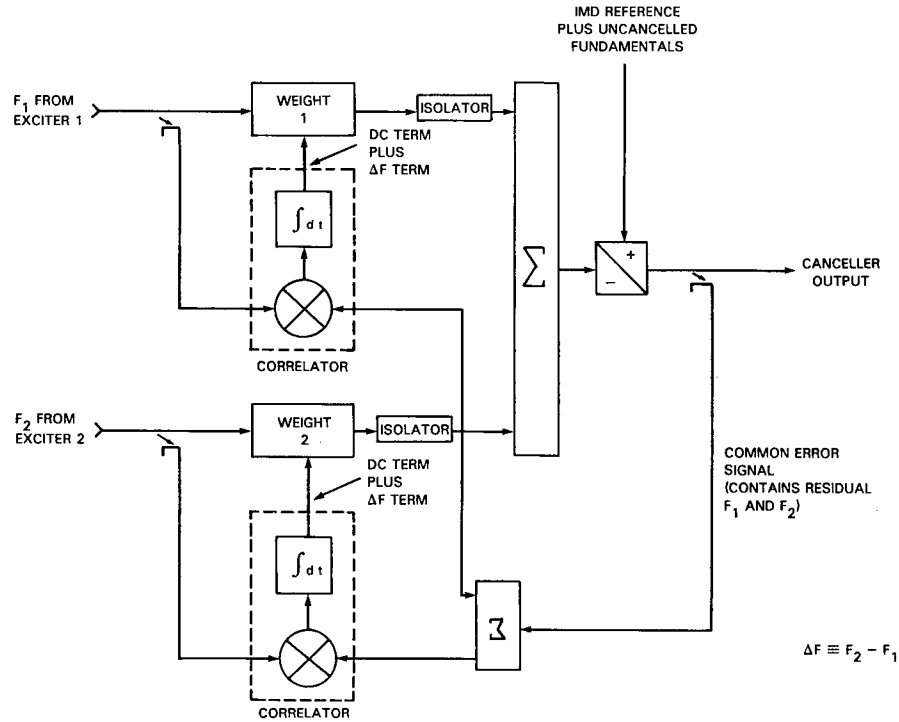

Fig. 19 — Generation of control-loop IMD

the LMS loop gain. Thus, for a given fundamental spacing ΔF, an increase in loop gain causes a commensurate increase in the amplitude of control-loop IMD. In the PBL system design, control-loop IMD is kept to acceptably low levels by the maintenance of low LMS loop gains in the FSAICs during steady-state operation.

IMD Canceller

The cancellation of IMD is provided by the IMD cancellers. Figure 20 shows a generalized block diagram of a feedforward IMD canceller. The RF input goes through the sampling coupler C_1 and the main-line delay cable to the distortion cancelling coupler C_2, where IMD cancellation is effected. The RF sample extracted by C_1 is one of the inputs to the fundamental-signal-cancelling coupler C_3. The other input is from the gain-adjusted output of the PBE. During initial balancing of the linearizer, the delay and amplitude of the signal from the PBE must be adjusted so that, when it is combined with the sample from C_1 in coupler C_3, at least 20-dB cancellation of fundamental signals is achieved (see Fig. 9). The delay can be adjusted by varying the cable length in the PBE signal path and the amplitude can be adjusted by varying the gain adjustment preceding C_3.

The output from coupler C_3 enters coupler C_4, where it is combined with the output of the FSAIC. The FSAIC cancels fundamental signals by at least an additional 30 dB, making the total reduction in relative fundamental levels more than 50 dB.

The feedforward amplifier chain begins with amplifier A_1, composed of two 15-dB amplifiers in series for a combined gain of 30 dB. The splitter divides the output of the amplifier A_1 into two paths. One output from the splitter supplies the feedback error signal to the FSAIC. The other output goes to the EQR, which compensates for nonlinear phase and nonconstant amplitude vs frequency in the feedforward amplifiers and couplers, mainly near 2 MHz.

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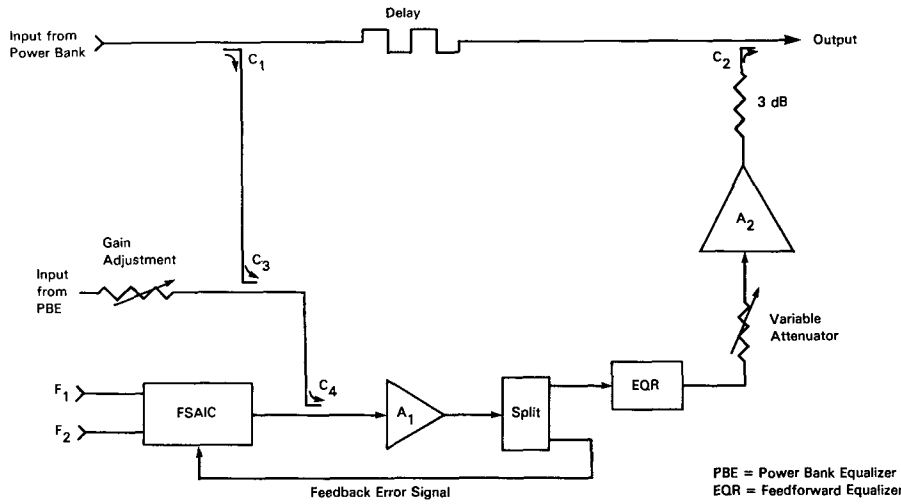

Fig. 20 — Feedforward IMD canceller

The EQR output goes through a variable attenuator to the final amplifier A_2. The variable attenuator allows easy adjustment of amplitude during initital balancing of the IMD feedforward loop. Delay adjustment is accomplished by varying cable lengths.

The output of amplifier A_2 goes through a 3-dB attenuator before entering the distortion-cancelling coupler C_2, where IMD cancellation is effected. The purpose of the attenuator is to make forward- and reverse-flowing signal levels equal at the output of amplifier A_2. The reverse-flowing signal at issue is that which would reflect back from the RF output port of the linearizing stage when that port is terminated in a load having a VSWR of four. It is desirable to make forward- and reverse-signal levels equal, because for this situation the distortion levels generated by intermodulation in amplifier A_2 are minimum [2] provided that the forward- and reverse-distortion characteristics of the amplifier are equal.

Phase compensation in the EQR introduces a 15° phase lag at 2 MHz to correct for a similar phase lead in the entire IMD canceller amplifier chain. The IMD cancellers in Stage I and Stage II are similar in design but differ in significant ways as described in the following sections.

Stage I IMD Canceller

For Stage I C_1 is a 30-dB directional coupler and the amplifier A_2, composed of two 10-dB amplifiers in series, has a combined gain of 20 dB. The EQR in Stage I has approximately 24-dB gain over the 2- to 30-MHz range. Experimental measurements have shown that, using this compensation, Stage I can achieve a feedforward IMD cancellation ratio of at least 22 dB from 2 to 30 MHz. This performance is shown in Fig. 21 for a tone swept from 0 to 50 MHz.

The first linearization stage is intended to reduce IMD products from a maximum level of −60 dBc to a maximum level of −80 dBc. Table 7 presents the required and realized second- and third-order output intercept points (OPI^2P and OPI^3P) [16] for critical components of the first-stage IMD canceller.

OPI^2P and OPI^3P are expedient parameters to use in characterizing the IMD requirements of components that are subjected to two fundamentals, assuming that the nonlinearity of the components is well behaved. OPI^nP is the arithmetic sum of the output power per fundamental (in dBW) plus

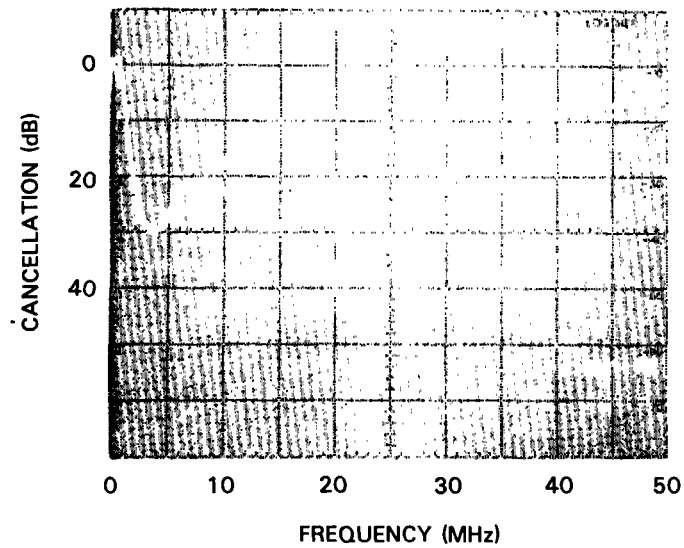

Fig. 21 — Performance of Stage I IMD canceller

Table 7 — Distortion Levels for Stage I Components

Component	Requirement for Output (IMD = −80 dBc)		Realized*	
	OPI^2P (dBW)	OPI^3P (dBW)	OPI^2P (dBW)	OPI^3P (dBW)
Sampling Coupler C_1	100	60	131	78
Fundamental-Cancelling Coupler C_3	63	23	101	34
Distortion-Cancelling Coupler C_2	100	60	111	70
Amplifier Chain $A_1 + A_2$	23	8	28	14

*Per laboratory measurements or manufacturer's data sheet

$1/(n-1)$ times the ratio (in dB) of the output fundamental power to the nth-order product power. Thus, OPI^2P (dBW) = fundamental power (dBW) + IMR, and OPI^3P (dBW) = fundamental power (dBW) + IMR/2, where IMR is the ratio (in dB) between the amplitude of the fundamental and the distortion product.

The amplifier chain within Stage I has a noise figure of approximately 3 dB. The broadband noise from the power bank will be cancelled to a negligibly small level, and in its place the noise from the amplifier chain and noise emanating from the adaptive weight drivers will be injected into the first-stage output.

Stage II IMD Canceller

As in the first stage, amplifier A_1 is composed of two 15-dB amplifiers in series; however, the first 15-dB amplifier in A_1 of Stage II operates at a 9-V dc bias level, where it has a low noise figure of

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approximately 2 dB. This is sufficient to keep the effective noise figure of the entire feedforward amplifier chain under 3.5 dB. The second 15-dB amplifier in A_1 operates at a 15-V dc bias level, so it can deliver higher output power without saturating.

For Stage II C_1 is a 20-dB directional coupler instead of a 30-dB one as in Stage I. This provides a signal 10 dB stronger to couplers C_3 and C_4 and the input to amplifier A_1. Signals 10 dB stronger are therefore required for the Stage II IMD canceller from the PBE and the Stage II FSAIC.

The second-stage EQR does not have gain, as does the first-stage EQR; in fact, there is approximately 16 dB of loss through the second-stage EQR. Stage II can achieve a feedforward IMD cancellation ratio of at least 19 dB from 2 to 30 MHz. This performance is shown in Fig. 22 using a tone swept from 0 to 50 MHz.

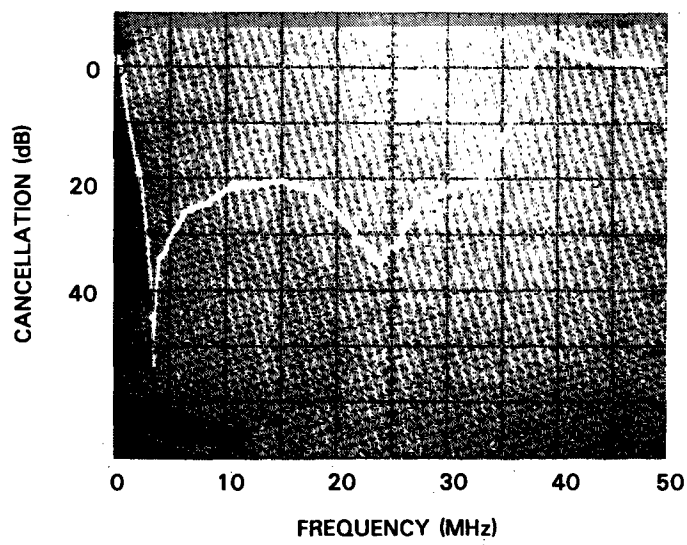

Fig. 22 — Performance of Stage II IMD canceller

The final amplifier A_2 in Stage II is composed of three amplifiers in series, with 10 dB, 13 dB, and 27 dB gain, for a total gain of 50 dB.

The second linearization stage is intended to reduce IMD products from a maximum level of −80 dBc to a maximum level of −100 dBc. Table 8 presents the required and realized second- and third-order output intercept points for critical components of the second-stage IMD canceller.

The amplifier chain in Stage II has a noise figure of approximately 3.5 dB. The broadband noise from the first stage will be cancelled to a negligibly small level, while noise from the second-stage amplifier chain and noise generated by the adaptive-weight drivers will be injected in its place into the second-stage output.

PERFORMANCE RESULTS

Figure 23 shows a block diagram of the performance measurement setup. Fundamental tones from two signal generators are amplified and provided separately through bandpass filters to the first- and second-stage FSAICs. The amplified signals are also combined by a multicoupler to provide the

Table 8 — Distortion Levels for Stage II Components

Component	Requirement for Output (IMD = −100 dBc)		Realized*	
	OPI^2P (dBW)	OPI^3P (dBW)	OPI^2P (dBW)	OPI^3P (dBW)
Sampling Coupler C_1	120	70	137	73
Fundamental-Cancelling Coupler C_3	83	33	123	47
Distortion-Cancelling Coupler C_2	120	70	137	73
Amplifier Chain $A_1 + A_2$	43	18	47	37

*Per laboratory measurements or manufacturer's data sheet

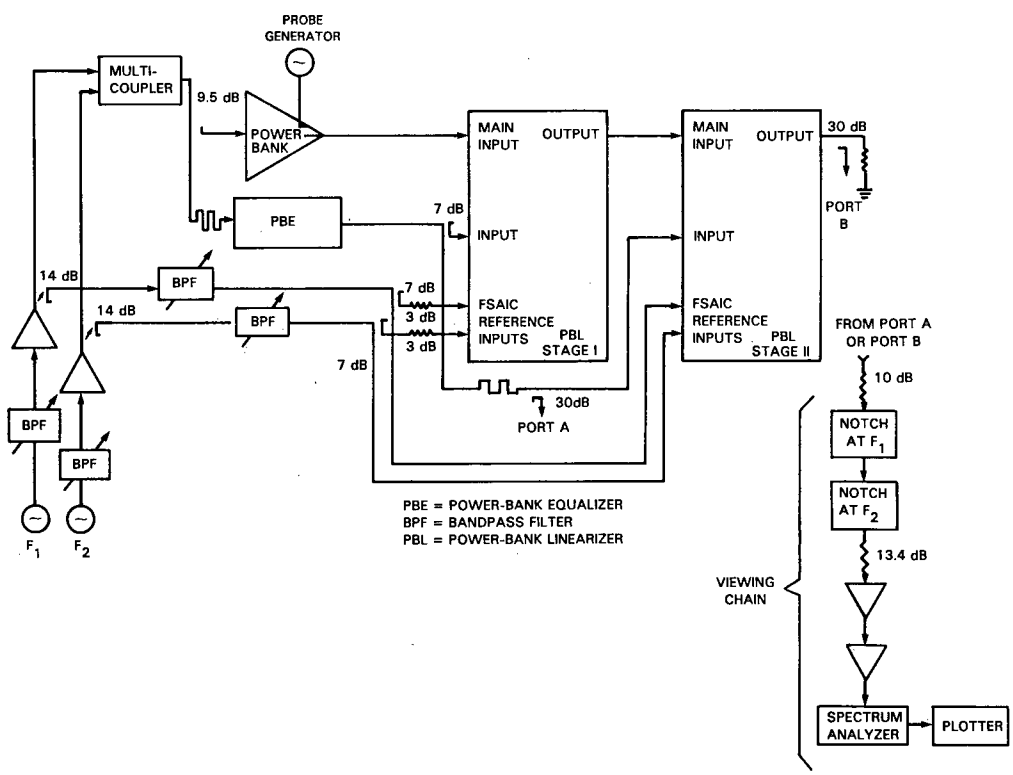

Fig. 23 — Experimental setup for measuring IMD cancellation of two-stage PBL

power bank and PBE with a combined signal. A third signal generator is available to inject a probe tone into the main signal output path through a 30-dB directional coupler built into the power bank. The bandpass filters and multicoupler remove exciter noise from the signals. The multicoupler and filters will not be required in future systems with low-noise exciters.

The probe signal is injected into the system such that it appears in the power-bank output but is not present in the signal path to the PBE and the adaptive weights. The probe signal appears to be generated in the power bank, but its frequency is selected so that it does not correspond to an actual IMD product frequency. Thus, the relative amplitude of the probe signal with respect to the amplitude of

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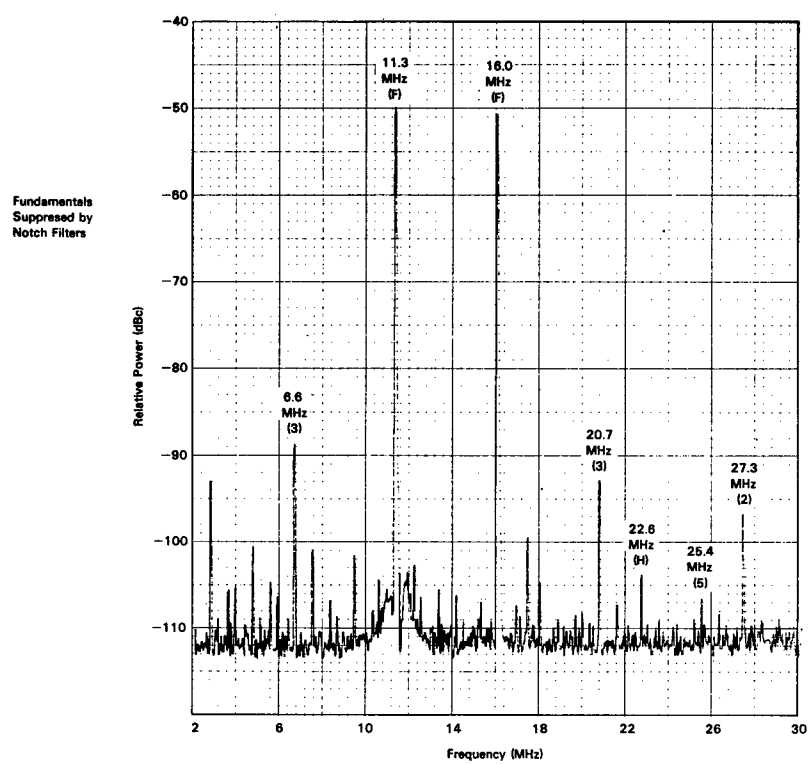
the fundamentals can be used to illustrate the potential cancellation available in each PBL stage, as distinguished from the IMD generated in that stage.

The signal viewing path is designed to have 0-dB loss, except at the fundamental frequencies, where notch filters provide from 50 to 55 dB of signal rejection. The signals of interest are monitored through 30-dB directional couplers placed in the PBE path (Port A) and the system output (Port B).

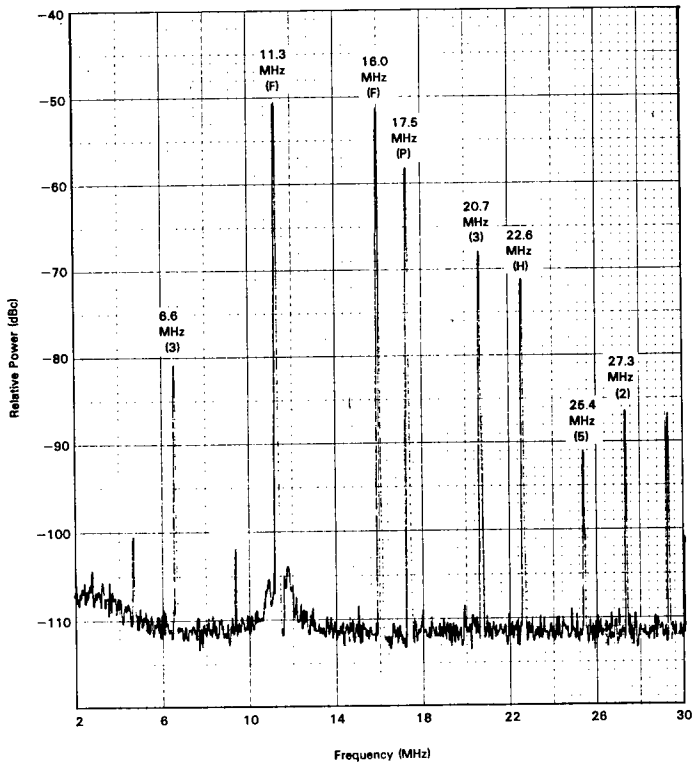
Three sets of performance data are discussed and presented below. Each set corresponds to a pair of fundamental frequencies, 11.3 and 16.0 MHz, 4.8 and 5.5 MHz, or 2.0 and 2.3 MHz. These three sets of performance data are shown in Figs. 24, 25, and 26. Output spectra are for the power bank and linearizer delivering two 100-W tones (20 dBW) to a 50-Ω load. Narrowband notch filters have suppressed the amplitude of the fundamentals by about 50 dB in Figs. 24 and 26 and by 55 dB in Fig. 25, providing an effective measurement range of about 110 dB. The most prominent intermodulation products are identified by a number appropriate to the distortion product order; harmonics of the fundamentals are designated by *H* and the probe signal is designated by a *P*.

Since harmonics are generated by the weights within the FSAICs and for this reason are not cancelled by the IMD cancellers, the output spectra are expected to show high levels of harmonic-tone generation. The discussion of results therefore will not deal with the levels of harmonics but will focus instead on the levels of IMD products generated by the fundamental signals.

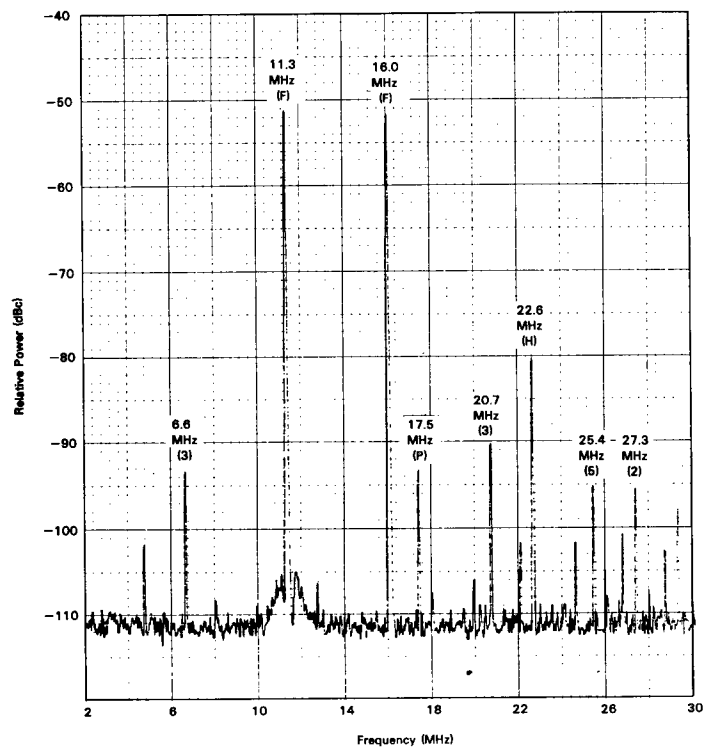


(a) Fixed-weight reference spectrum (Port A)

Fig. 24 — Performance spectra for fundamental frequencies of 11.3 and 16.0 MHz



(b) Uncancelled output spectrum (Port B)



(c) Cancelled output spectrum (Port B)

Fig. 24 (Continued) — Performance spectra for fundamental frequencies of 11.3 and 16.0 MHz

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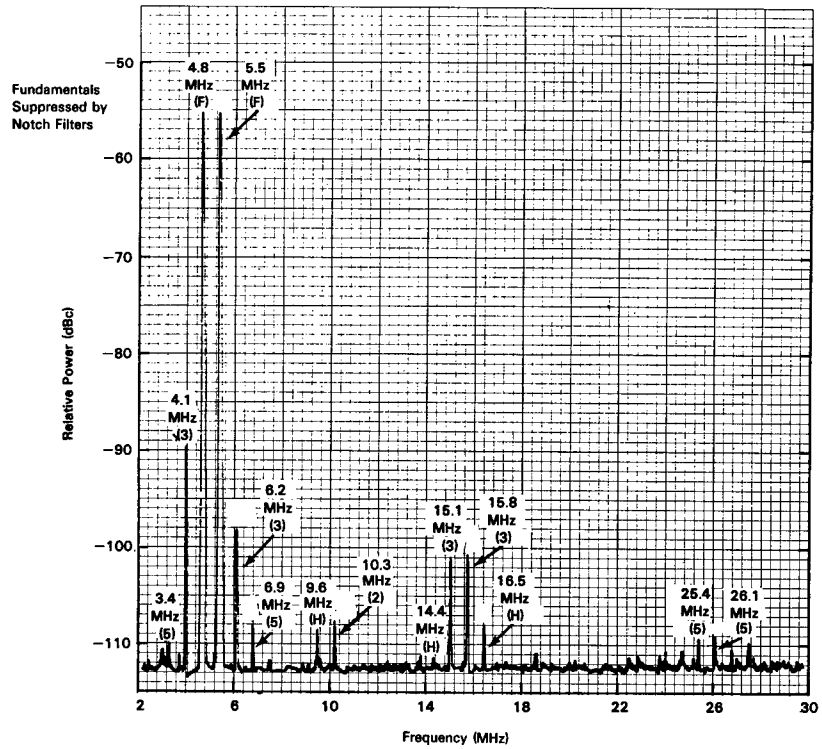
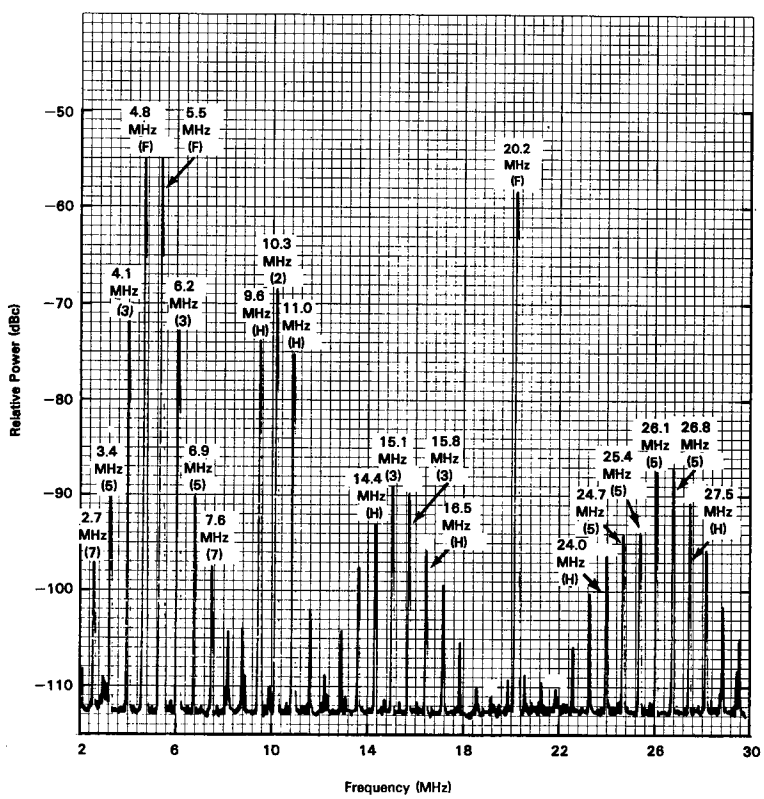
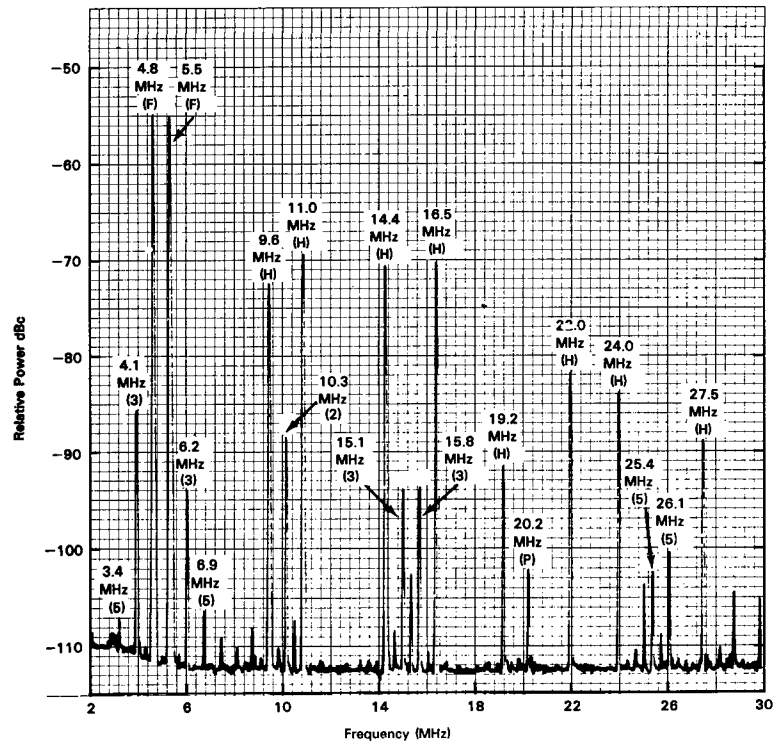


(a) Fixed-weight reference spectrum (Port A)



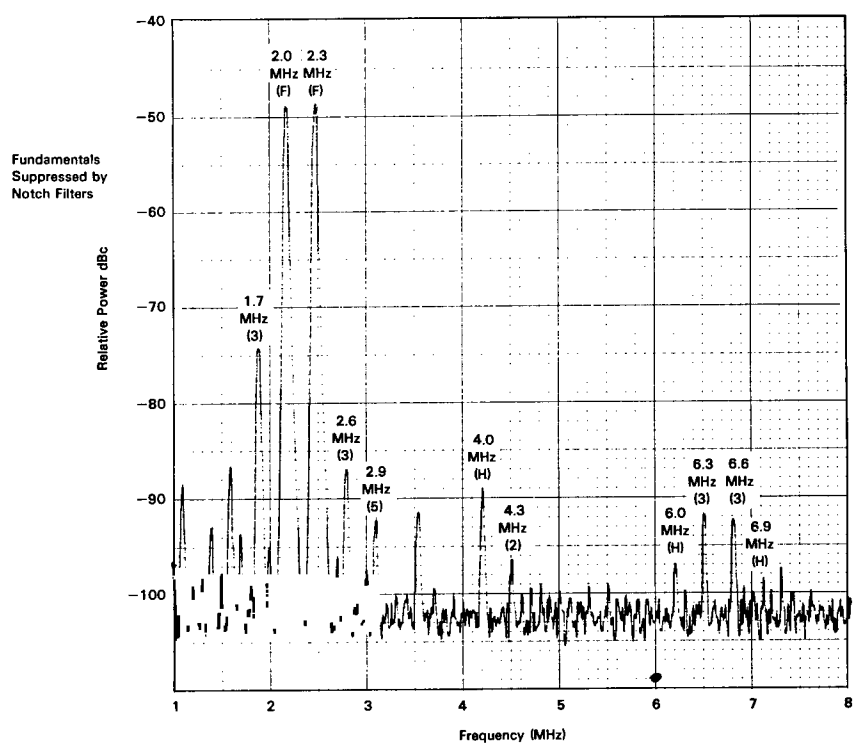
(b) Uncancelled output spectrum (Port B)

Fig. 25 — Performance spectra for fundamental frequencies of 4.8 and 5.5 MHz



(c) Cancelled output spectrum (Port B)

Fig. 25 (Continued) — Performance spectra for fundamental frequencies of 4.8 and 5.5 MHz



(a) Fixed-weight reference spectrum (Port A)

Fig. 26 — Performance spectra for fundamental frequencies of 2.0 and 2.3 MHz (feedforward canceller within power bank disabled)

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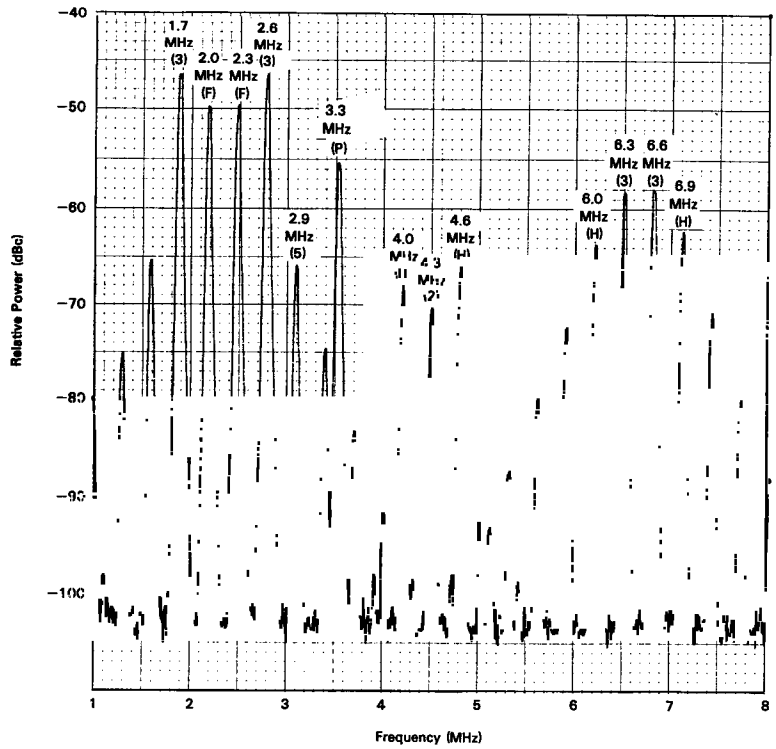
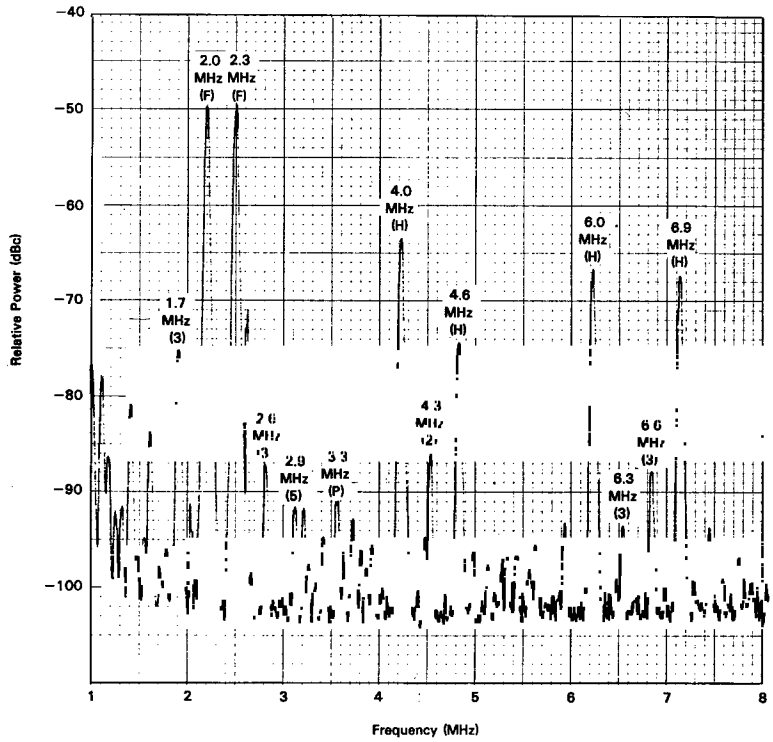


(b) Uncancelled output spectrum (Port B)



(c) Cancelled output spectrum (Port B)

Fig. 26 (Continued) — Performance spectra for fundamental frequencies of 2.0 and 2.3 MHz (feedforward canceller within power bank disabled)

Figure 24 shows a sequence of output spectra for the first set of fundamental frequencies at 11.3 and 16.0 MHz. Figure 24(a) shows a spectral plot of the PBE reference (Port A) for the first pair of fundamentals. Note that the reference is contaminated by IMD, most severely by the third-order-difference distortion products (6.6 and 20.7 MHz) at levels of −89 and −93 dBc. The presence of these products in the reference limits the achievable linearization.

Figure 24(b) shows the linearizer output (Port B) with the cancellation stages turned off. The single in-band second-order product at 27.3 MHz is at about −86 dBc. Third-order products at 6.6 MHz and 20.7 MHz have levels of −80 dBc and −68 dBc. A fifth-order product at 25.4 MHz is at about −90 dBc. Note that a probe tone at 17.5 MHz has been injected at the power-bank output at a level of −58 dBc.

In Fig. 24(c) the cancellation stages are turned on. The probe tone is cancelled by 35 dB to a level of −93 dBc. The second-order sum product at 27.3 MHz is cancelled to −96 dBc, to within 1 dB of the PBE reference level shown in Fig. 24(a). The third-order difference IMD products are also cancelled to levels roughly corresponding to their levels in the PBE reference signal, approximately −90 dBc. Some discrepancy exists between the IMD level in the reference, Fig. 24(a), and in the linearized output, Fig. 24(c). This discrepancy is the result of chance combinations, sometimes constructive, sometimes destructive, of IMD products generated in the linearizing stages with IMD products in the reference signal. The in-band fifth-order product at 25.4 MHz is cancelled to −95 dBc. All other IMD products are cancelled to levels below −95 dBc.

Figure 25 shows a sequence of output spectra for the second set of fundamental frequencies at 4.8 and 5.5 MHz. Figure 25(a) shows the spectrum at the output of the PBE for the second PBL stage. It is observed that significant second-, third, and fifth-order distortion exists at the output of the PBE. Since this distortion does not originate in the power bank, it will not be reduced by feedforward cancellation, and it will appear at the output.

Figure 25(b) shows the output spectrum with both PBL stages inoperative. The single in-band second-order product at 10.3 MHz is at about −68 dBc. The close-in third-order products at 4.1 and 6.2 MHz are at about −72 dBc each, and the outer third-order products at 15.1 and 15.8 MHz are at about −89 dBc. The most prominent fifth-order products vary between −87 dBc and −94 dBc, and seventh-order products are below −95 dBc. The probe signal, at 20.2 MHz, appears in Fig. 25(b) at a level of about −58 dBc.

In Fig. 25(c) both stages of the PBL are activated. The probe signal has been reduced by 43 dB to a value below −100 dBc, while the second-order product is reduced by 20 dB to a level of about −88 dBc. Three out of four of the third-order products have been reduced to an amplitude of about −94 dBc. The strongest third-order product has been reduced to a final value of about −86 dBc. Fifth- and seventh-order products have been reduced to levels below −100 dBc. Some additional products present in Fig. 25(c), and not appearing in Fig. 25(b), are the result of mixing of the probe signal with the fundamental signals in the PBL stages.

The third set of performance data, shown in Fig. 26, is for fundamental frequencies at 2.0 and 2.3 MHz. At these frequencies the power bank is very linear and IMD is below −70 dBc. Since Stage I is designed for linearizing a power bank whose output IMD level is around −60 dBc, the power bank is "delinearized" for this set of results to increase its level of output distortion. This is accomplished by removing the dc-power connection to the power bank's internal feedforward distortion canceller.

Fig. 26(a) shows a spectral plot of the PBE reference (Port A). Once again, the reference is contaminated by IMD products; the strongest is the −74-dBc third-order difference product produced at 1.7 MHz. The source of this particular product is the PBE reference signal.

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Figure 26(b) shows the linearizer output (Port B) with the cancellation stages turned off. Note the relatively high distortion levels, resulting from delinearization of the power bank. The second-order sum product at 4.3 MHz is at about −70 dBc. The in-band third-order difference product at 2.6 MHz has a level of −47 dBc, while the third-order sum products at 6.3 and 6.6 both have levels of −58 dBc. The in-band fifth-order products at 2.9, 5.7, and 7.2 MHz vary from about −66 to −72 dBc. The probe tone at 3.3 MHz is injected at a level of −55 dBc.

Figure 26(c) shows the linearizer output again, but with the cancellation stages turned on. Comparison with Fig. 26(b) shows that the probe tone is cancelled by 36 dB, the third-order difference product at 2.6 MHz by 40 dB, and the third-order sum product at 6.3 MHz by 36 dB. The out-of-band third-order difference product at 1.7 MHz is reduced by only 28 dB, its cancellation being limited by the 1.7-MHz contamination in the reference signal (Fig. 25(a)). The third-order sum product at 6.6 MHz is cancelled by 30 dB, and the second-order sum product at 4.3 MHz is cancelled by only 16 dB. These poor cancellation ratios are not due to contamination of the reference signal (Fig. 26(a)); hence, distortion generation somewhere within the linearizer must be limiting performance at these frequencies. The fifth- and higher-order products are reduced to levels below −90 dBc.

Some low-frequency noise below 2 MHz can be seen in the output spectrum of Fig. 26(c). The source of this noise is suspected to be the adaptive-weight drivers.

Figure 27 summarizes the results appearing in Figs. 24 and 25. The shaded areas illustrate the variation in level from minimum to maximum of the probe signal as well as the second-, third-, and fifth-order products for the two pairs of fundamental frequencies. The results appearing in Fig. 26 are not included since the power bank is delinearized for this set of results.

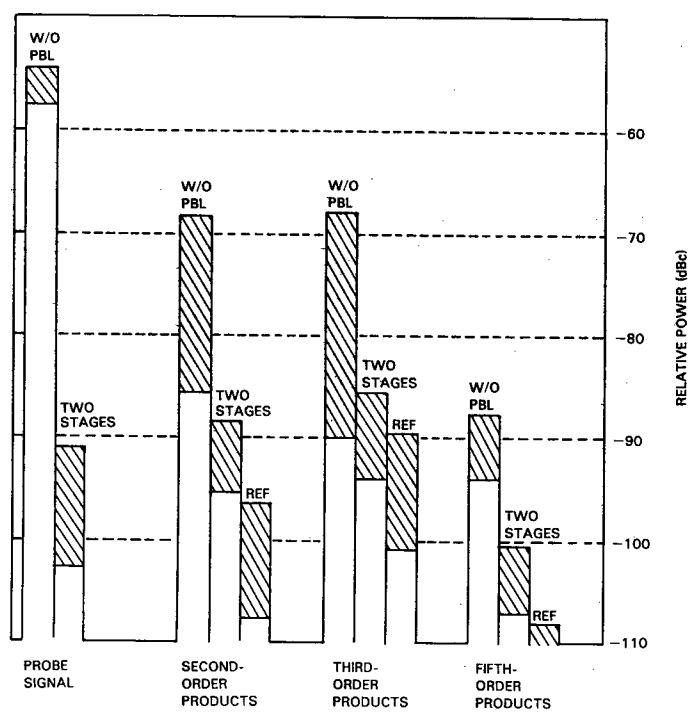

Fig. 27 — Output summary without PBL and with two-stage PBL for fundamental-frequency pairs at 4.8, 5.5 MHz and 11.3, 16.0 MHz

It is observed that, although the PBL has been effective in significantly reducing the amplitude of distortion products, the amount of reduction is not nearly as great as the reduction obtained for the probe signal.

PERFORMANCE LIMITATIONS

In an effort to isolate sources of IMD that limit PBL performance, we examine key points in the linearizer. The output from the FSAIC is an important potential source of IMD.

Figure 28 shows the distortion performance of the FSAICs with the second set of test signals (4.8 and 5.5 MHz) applied to the input of coupler C_4 (in Fig. 15) in place of the signal that would normally come from coupler C_3, −7 dBm per tone for Stage I and 3 dBm per tone for Stage II. These levels are equivalent to those expected when C_3 is providing 20 dB of fundamental-signal cancellation with 100-W fundamental signals on the main line. These input signals are free of power-bank distortion at this point and allow the performance of the FSAIC weights to be evaluated. The notch filters within the testing setup are removed, for the results shown in Fig. 28, so that the fundamental frequencies at 4.8 and 5.5 MHz are not suppressed.

The FSAIC distortion shown in Fig. 28 from Stages I and II is clearly dominated by harmonics generated by the weights. No third-order IMD products are detectable down to −107 dBc for Stage I and down to −120 dBc for Stage II. A second-order product in Fig. 28(b) is detectable at −115 dBc, but this level is more than 20 dB below any second-order product that would be entering Stage II from Stage I. Distortion (other than harmonic) from the FSAIC weights is at an acceptable level.

In Fig. 25(c) the final third-order and fifth-order IMD performance is within approximately 2 to 8 dB of the performance achieved at the output of the PBE for the second PBL stage (Fig. 25(a)). The final second-order performance, −88 dBc, is approximately 20 dB poorer than the corresponding performance obtained at the output of the PBE. Distortion products generated in the PBE will not be reduced by feedforward cancellation, and they will appear at the output of the linearizing stage. Thus, the contaminated reference signal limits the amount of IMD cancellation that the linearizing stages can provide.

Any distortion generated in the PBE will appear at the system output, thereby setting a floor on the system-output distortion-to-signal ratio. The PBE is implemented by quadrature hybrids (similiar to the quadrature hybrids that are used in the power bank) in order to achieve the desired phase-vs-frequency response. These hybrids are ferrite devices, and therefore they can generate distortion. The worst-case in-band distortion component at the PBE output is −87 dBc for two fundamental signal tones whose corresponding output level is 100 W each.

Figure 25(a) shows the spectrum at the output of the PBE for the second PBL stage. Ideally, this spectrum should contain responses corresponding only to the fundamental signals. It is observed, however, that significant second-, third-, and fifth-order distortion exists at the output of the PBE. Since this IMD is not generated by the power bank, its interaction in the feedforward cancellation process is not predictable, and it will most likely appear undiminished at the output of the linearizing stages. Thus, the contaminated reference signal limits the amount of IMD cancellation that the linearization stages can provide. Contamination of the reference signal is mainly from the quadrature hybrids within the PBE, and it is partly from the two directional couplers surrounding (one preceding and one following) the PBE. Obviously, any distortion generated in the feedforward processing by passive components, such as ferrite core transformers or directional couplers, feedforward amplifiers, and adaptive weights, will not be cancelled and will be passed on to the output.

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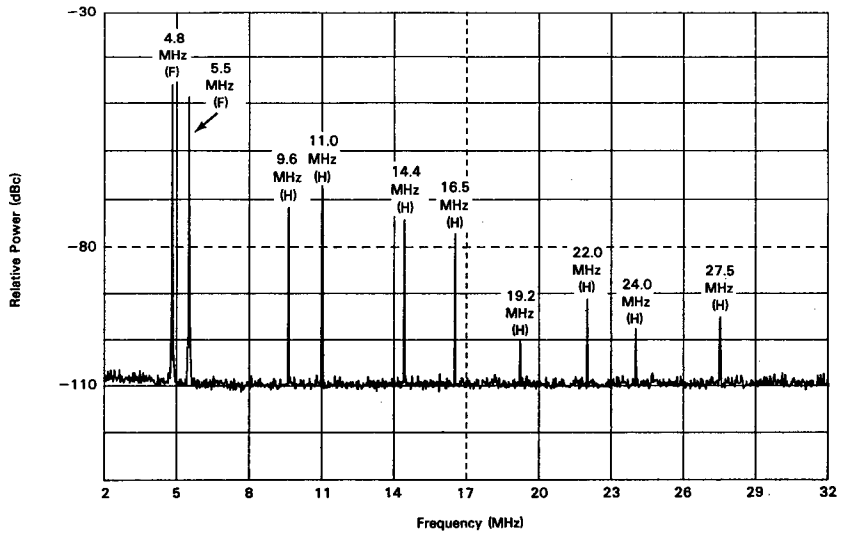
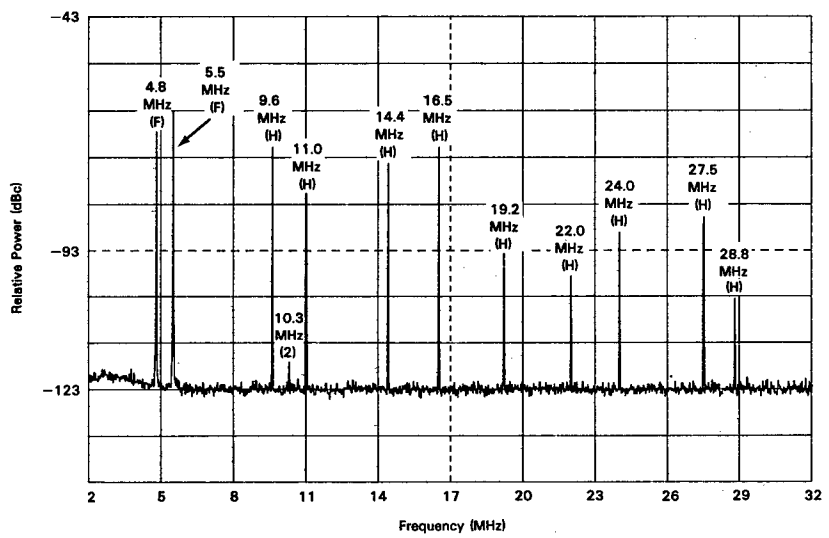


(a) Stage I FSAIC distortion



(b) Stage II FSAIC distortion

Fig. 28 — FSAIC distortion performance

Another possible source of contamination is from IMD originating in the power bank that can enter the PBE path because of imperfect directivity in the directional couplers that supply the PBE signals to Stages I and II. Careful examination of these "sneak paths" reveals no measurable degradation by this mechanism.

Although the PBL is effective in reducing intermodulation distortion, the harmonic performance can be degraded as a result of harmonic distortion originating in the adaptive weights. Observed IMD cancellation is on the order of 20 dB per stage, as expected, except where it is limited by an IMD-contaminated reference signal or by IMD generated within the PBL stages. The internal IMD generation is believed to take place in the high-power sampling and distortion-cancelling couplers. Research effort is currently under way for the development of active weights, ferrite-core transformers, and directional couplers having improved distortion performance.

The PBL does not oscillate when terminated in a broadband 50-Ω load, despite the fact that the stages contain EQRs having excess low-frequency gain [17]. It is anticipated, however, that oscillation will occur if loads having poor low-frequency VSWRs are used to terminate the PBL. This problem will be considered in future PBL designs, either through development of a suitabie main-path equalizer, or through the use of extremely wideband feedforward amplifiers that require little phase equalization and correspondingly small out-of-band excess gain.

CONCLUSIONS

An HF linear amplifier has been developed that is capable of delivering 500-W PEP with intermodulation-distortion performance significantly better than previously available. This performance has been achieved through a combination of negative feedback, feedforward, and multiphase amplification applied to the most linear power devices available. Multiphase amplification inherently discriminates against many types of distortion products. The basic low-distortion performance of the linear amplifier has been extended by means of a power-bank linearizer that consists of an iteration of feedforward stages. Although three stages have been planned, only two have been implemented. To minimize power handling and distortion requirements of the feedforward amplifiers, adaptive weights are used to augment a broadband power-bank equalizer in the cancellation of fundamental energy for each stage.

Performance measurements have verified the concept, although overall goals have not been completely realized. The major limitation in the implementation of the power-bank linearizer is the distortion introduced by components containing ferrite material, particularly the broadband power-bank equalizer and high-power sampling and distortion-cancelling couplers. Other sources of distortion-product generation are other passive components containing ferrite material, such as transformers and other directional couplers, and from active components such as adaptive weights and amplifiers. Research effort is currently under way for the development of active weights, ferrite-core transformers, and directional couplers having improved distortion performance.

RECOMMENDATIONS

It is recommended that an effort be made to extend the performance measurements reported herein to other frequencies, for various load terminations, and to initiate investigations into various transient-response effects. Components that are now limiting distortion performance should be identified and replaced by components having improved characteristics as they become available. It is further recommended that the power bank and PBL hardware be exploited as a test bed to the greatest extent possible in aiding the development of the power amplifier currently being developed by the Naval Electronic Systems Command for the High Frequency Improvement Program.

ACKNOWLEDGMENTS

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