

1200-to-1300-MHz 100-Watt Transistor Power Amplifier

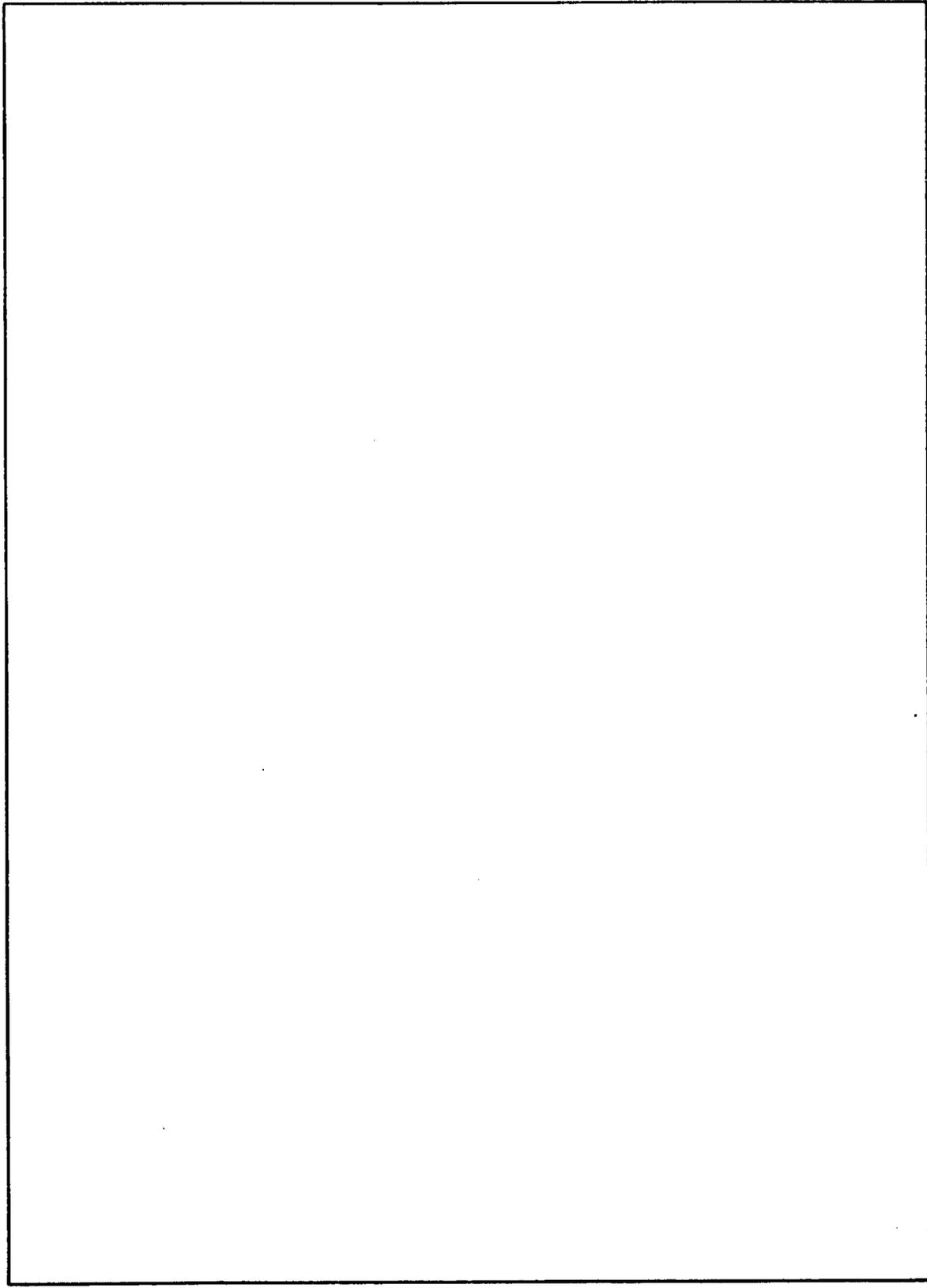
R. E. NEIDERT AND H. E. HEDDINGS

*Microwave Techniques Branch
Electronics Division*

March 5, 1974



NAVAL RESEARCH LABORATORY
Washington, D.C.



CONTENTS

INTRODUCTION	1
TRANSISTORS	2
EMITTER BIAS RESISTANCE	4
DIVIDE/COMBINE NETWORKS	5
ISOLATED OUTPUT PORTS.....	5
MULTISTAGE TUNING.....	6
CONCLUSIONS	8

1200-to-1300-MHz 100-WATT TRANSISTOR POWER AMPLIFIER

INTRODUCTION

The modern phased-array radar antenna may consist of a large number of small radiating elements, with each element containing its own transmitter. By proper phasing of the signals transmitted from each individual element, the outputs can be summed and directed into space. Microwave transistor amplifiers are being considered for such transmitter applications. For example, a planar grid containing one thousand 100-W transmitters has a total output power of 100 kW, and its beam direction can be electronically steered.

Microwave transistor power amplifiers are being investigated at the Naval Research Laboratory for the phased-array antenna and other applications. This report describes the development of a 100-W transistor power amplifier in the 1200-to-1300-MHz frequency range. It discusses practical problems and solutions related to transistors and biasing and to the high-dielectric-constant microstrip circuitry being universally proposed for such applications. It also describes some tuning and fault-analysis aids relevant to such amplifiers. Figure 1 is a photograph of the amplifier. It is a two-stage amplifier with one transistor driving four. Input power is 6.5 W; output power is over 100 W. The following sections give some development details and conclude with the amplifier-power-output performance curves.

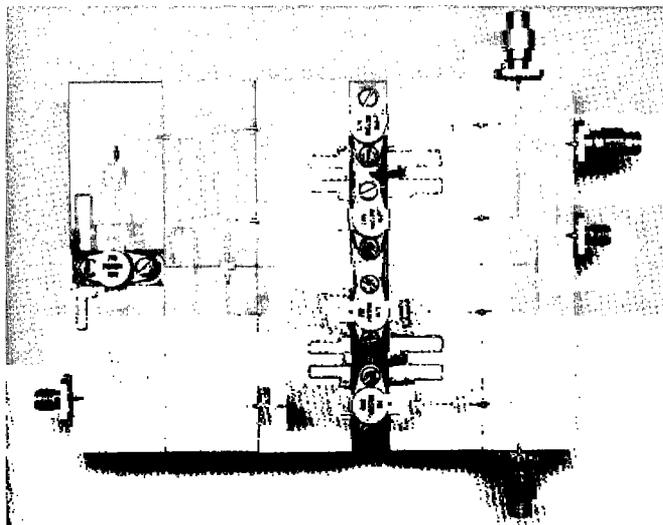


Fig. 1 — Microwave transistor power amplifier

TRANSISTORS

The problem of transistor selection was compounded due to the wide performance variations, even among devices of the same type. As an example, Table 1 contains data which show major differences among PHI 1520H transistors.

Table 1
Performance Variations in PHI 1520H Transistors*

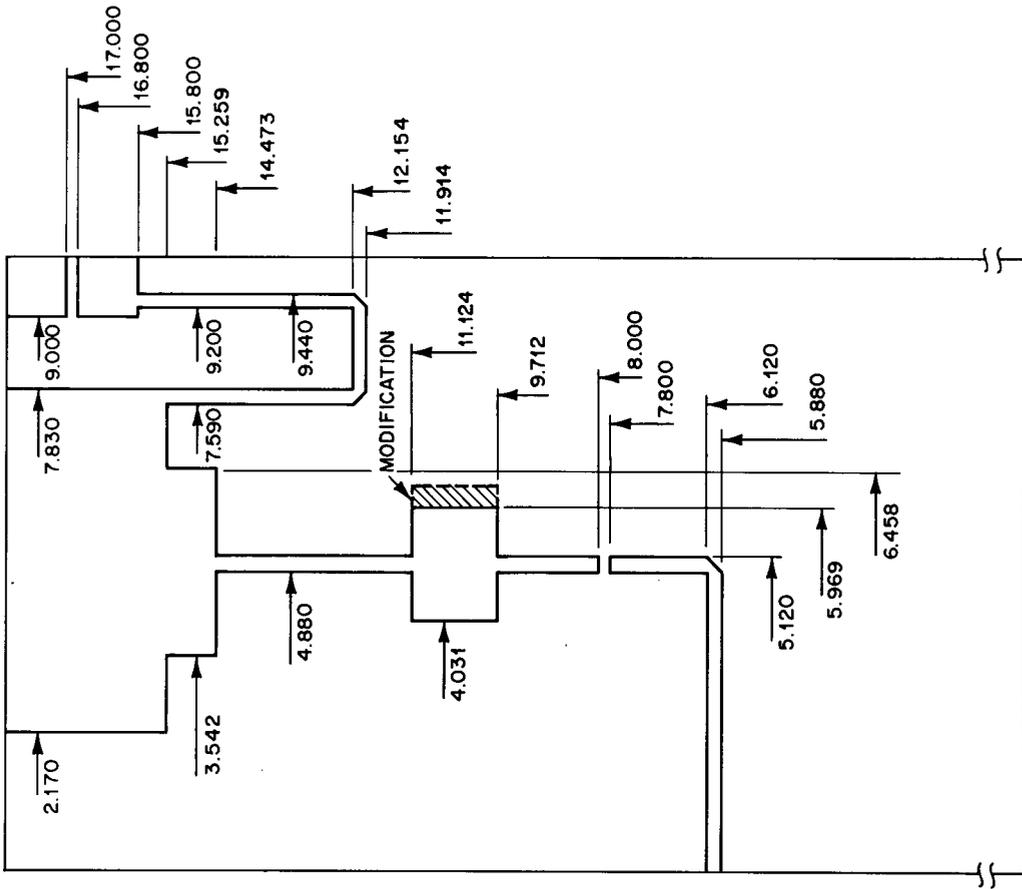
Transistor	Output Power (W)		
	1200 MHz	1250 MHz	1300 MHz
Design	33.0	35.0	29.0
West. #1	5.5	27.5	18.2
West. #2	2.2	22.8	17.0
Test #1	24.6	23.0	16.5
Test #2	28.1	27.8	21.2
2-1	0.0	19.0	10.5
2-2	OSCILLATION		
2-3	0.0	25.0	18.0
2-4	0.0	20.0	11.0
2-5	1.0	23.5	17.0
2-6	24.5	20.0	13.0
2-7	2.0	25.0	18.0
2-8	22.0	17.0	10.0

* $P_{in} = 6.5$ W
10- μ s pulse
 $V_{cc} = 28$ V

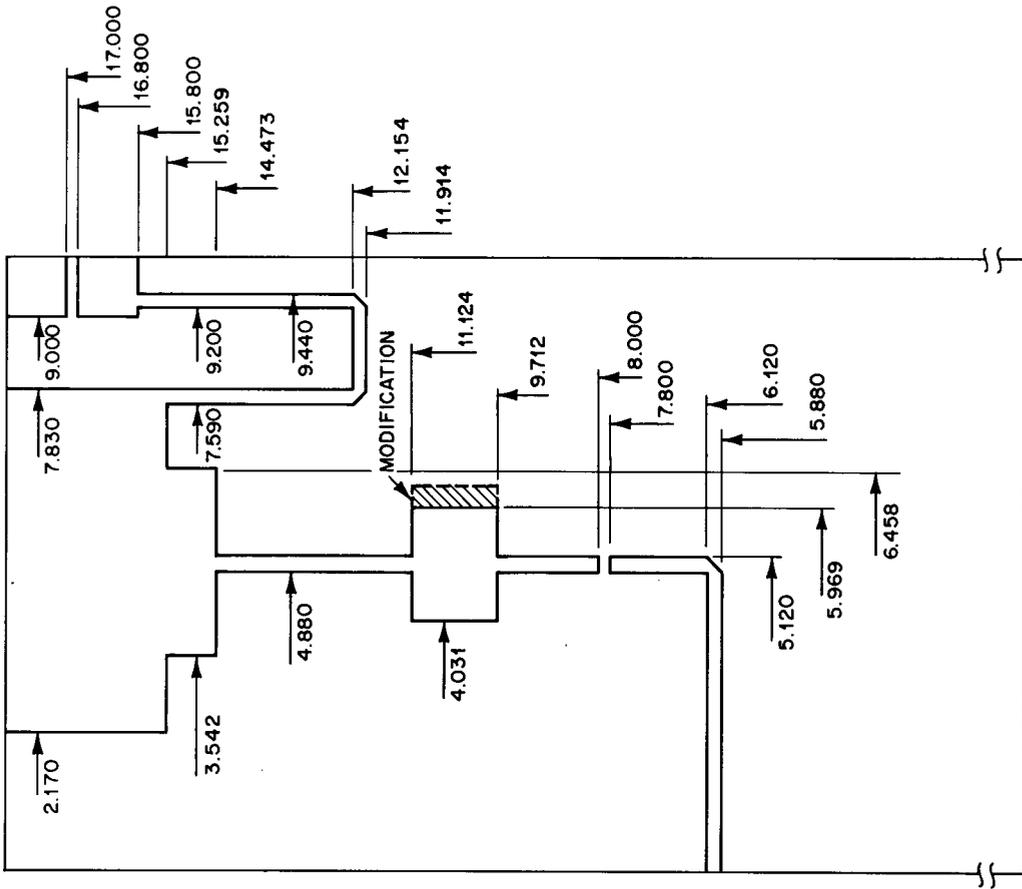
The circuit employed (Fig. 2) was constructed of chrome/gold metallization on 0.0025-in.-thick alumina and designed using the transistor of first entry in Table 1. As indicated, the data for the 12 other transistors show poor transistor interchangeability over a 10% bandwidth.

Table 2 shows the data for the same transistors used in a circuit modified for a more constant output among the transistors. The results show approximately a two-to-one variation of output power at the end points of a 10% band; also the output power is typically lower than desirable.

When this problem was recognized, alternate courses of action were considered: to search for a more consistent transistor type, to develop a separate circuit for each transistor, or to touch up each transistor circuit after assembly. In this case it was decided to use the transistors on hand and see what could be done with them using in-circuit tuning.



(a) Emitter



(b) Collector

Fig. 2 — Matching circuits for the PHI 1520H transistor; xy coordinate system at 10:1 scale.

Table 2
Performance Variations in PHI 1520H Transistors*
Using the Modified Circuit

Transistor	V _{cc}	Output Power		
		1200 MHz	1250 MHz	1300 MHz
West. #1	28	24.5	28.5	21.0
West. #1	30	27.0	37.5	24.5
West. #2	28	14.0	22.0	14.0
West. #2	30	16.0	24.5	16.5
2-1	28	31.0	27.0	17.0
2-1	30	34.0	31.0	20.0
2-3	28	30.0	26.0	16.0
2-3	30	33.0	29.0	19.0
2-4	28	24.0	20.0	10.5
2-4	30	28.0	23.5	13.0
2-5	28	0	0	0
2-7	28	19.0	30.0	20.0
2-7	30	16.0	34.0	24.0
2-8	28	26.5	20.0	11.5
2-8	30	31.0	24.0	14.0

*P_{in} = 6.5 W
10- μ s pulse

EMITTER BIAS RESISTANCE

Referring again to Fig. 2, solder coating of the quarter-wavelength stubs from emitter to ground and from collector to DC supply voltage was required. This was used because the DC resistance of these lines, resulting from the original 0.00025-in.-thick gold metallization, was too high (0.4 ohms). The amplifier stages were designed using 0.05 ohms for the emitter return resistance, and they put out 20% to 30% more power with the lower emitter resistance. In particular, the collector resistance should be as low as possible, since total output power from the amplifier varies about 14 W per volt. Reduction from 0.4 to 0.05 ohms in the collector DC circuit results in about 0.7 V less drop to each transistor and about 10 W more total output.

DIVIDE/COMBINE NETWORKS

The divide/combine networks employed were similar to Lange-type couplers. Figure 3 shows the crossover bonds and a portion of the coupling lines.

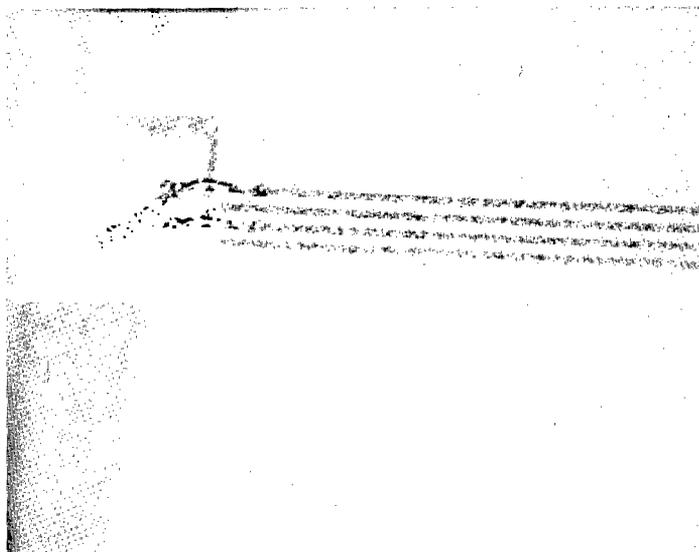


Fig. 3 — Coupler bonds

Figure 4 shows the amplifier divide-by-four network. The first group of substrates etched for this application gave the output-amplitude data shown in parentheses (at band center). This was not acceptable—the coupling lines and spaces varied over a wide range, with spacing reaching 0.0028 in. in one coupler. The second group, etched with a more complex procedure, yielded consistent 0.0022-in. line spacings and 0.0024-in. line widths. These produced the final data shown, a nearly ideal four-way split with about 0.7-dB insertion loss.

Phase of the outputs was within about 2° . Individual coupler isolation was over 35 dB in the band of interest. One of the output-combine-network substrates was not RF tested prior to final assembly. (It was visually inspected and dimensionally checked.) It was later found to have a bad bond which was not detectable by visual inspection. The DC-resistance difference between one crossover bond and two bonds was a detectable 0.1 ohms.

ISOLATED OUTPUT PORTS

In Fig. 1, four connectors are visible at the output end of the amplifier. All four arms of the combine network were intentionally made accessible to facilitate measurements

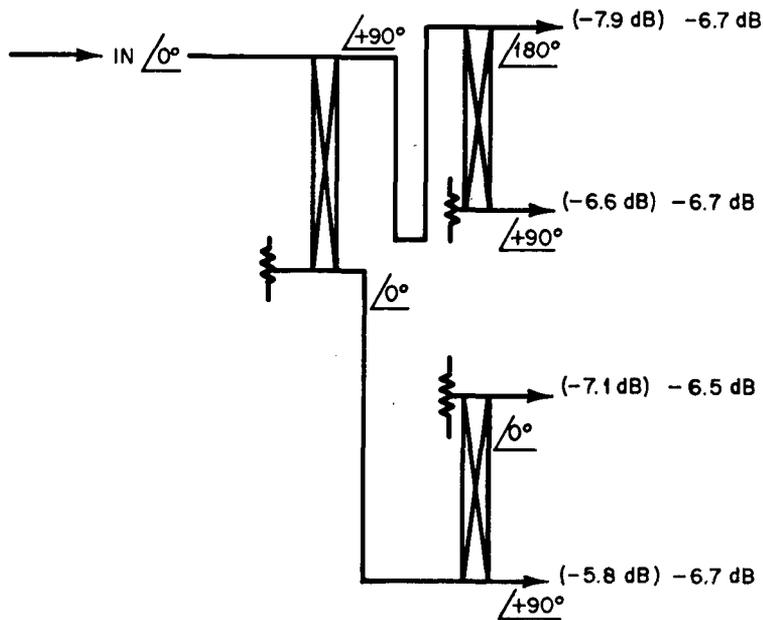


Fig. 4 — Divide-by-four network

of the nonquadrature components of transistor output power. At various times in the tuning procedure, the outputs from all ports were sampled, with levels as high as 20 W from ports other than the desired output port. After final tuning, however, the sum of the powers from all three of the "isolated" ports was only a few watts. In the course of the work, a technique for fault analysis using these output ports was developed and tested. Assuming only that the four input signals to the four-way combiner are approximately at their intended phase, the output power of each transistor individually can be deduced from measurement of the four output levels from the combiner. For example, one case tested was at a frequency where the combiner outputs were 16, 5, 40, and 5 W. The fault-analysis technique properly pointed out that one transistor was putting out nothing and told which one.

MULTISTAGE TUNING

The experimental touchup tuning of microstrip matching circuits for transistor power amplifiers can be done in many ways. Sometimes it is accomplished by bonding to small auxiliary metallization pads adjacent to large metallized areas. This touchup tuning is simple, in the hands of an experienced technician, for single-stage, single-transistor amplifiers, since input power, reflected power, and output power are all readily and independently accessible for measurement.

However, multistage amplifiers or single-stage, multitransistor amplifiers present a formidable touchup tuning problem. Consider the block diagram of Fig. 5 showing a circuit for two stages of a power amplifier.

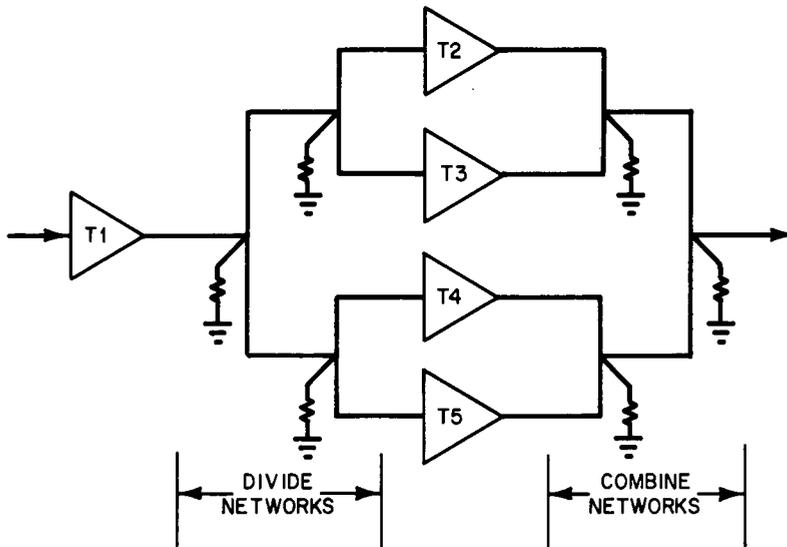


Fig. 5 — Two-stage power amplifier

Several problems can arise in the construction of such an amplifier which could cause one or more of the transistors to be performing improperly at initial turnon. For example, the transistor source and terminating impedances may not be the ideal 50 ohms used for the initial circuit development; the divide/combine networks may not split perfectly for various reasons; damage to circuit components or transistors may have been sustained during construction; and so forth. If the signal from the output port is not as expected, then the problem is to establish which stage or which transistor is at fault.

A small coupling loop for qualitatively sampling the field intensity at various points in a circuit has been used for fault location. Construction details of an experimental loop for the lower D band are given in Fig. 6 along with an abbreviated diagram of a test setup.

Before such a loop is employed over a significant bandwidth, its response should be tested by sampling the field near a length of matched microstrip transmission line; loop size can then be adjusted, if necessary, for reasonable response flatness.

The curves of Fig. 7 are swept response data taken on an amplifier like that shown in Fig. 5. The input-power and output-power curves were taken in the usual way, with crystal detectors on directional couplers before and after the amplifier. The T1 curve

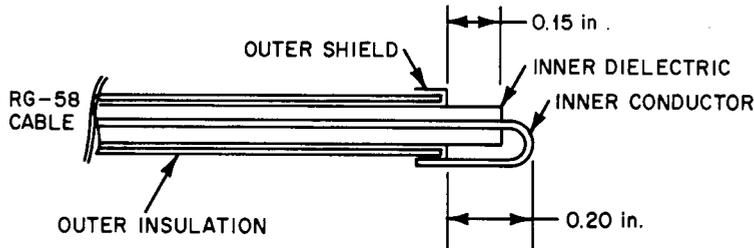
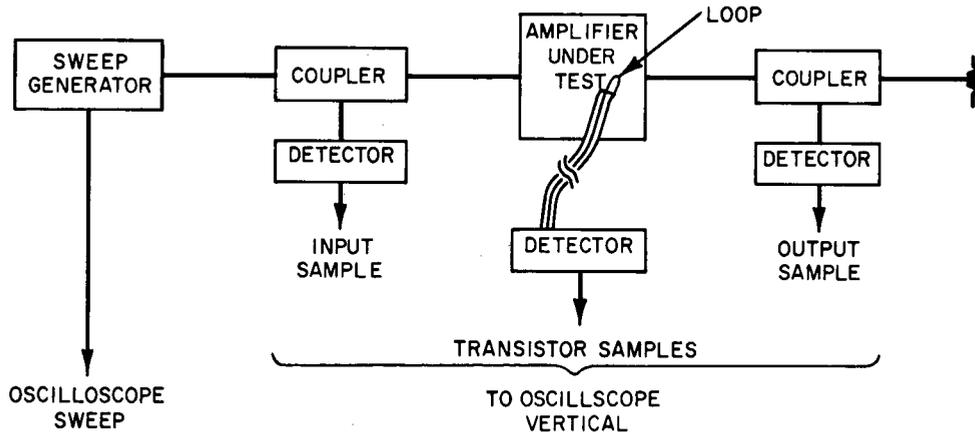


Fig. 6 — Test setup and loop

is the detected response with the loop held directly over and as close as possible to the driver transistor. The loop was rotated for maximum signal strength. The T2 through T5 curves were similarly obtained. Fault analysis from these curves is simple—T2 and T3 are not being turned on over portions of the band. This information could not be deduced from the output-power curve alone; although, interestingly, the converse is true. Touchup tuning was done on the matching circuits of T2 and T3 by observing the fields in their vicinity independently, after which all curves were continuous and the output power had risen to its normal level.

CONCLUSIONS

Figure 8 shows the final output-power performance data of the amplifier described in this report. For a constant input power of 6.5 W, the output-power curves are shown for collector supply voltages of 28, 29, and 30 V. The maximum pulse width used was 100 μ s, and the duty factor was constant at 1%. This performance is the state of the art in this frequency range for power transistors available in mid-1973.

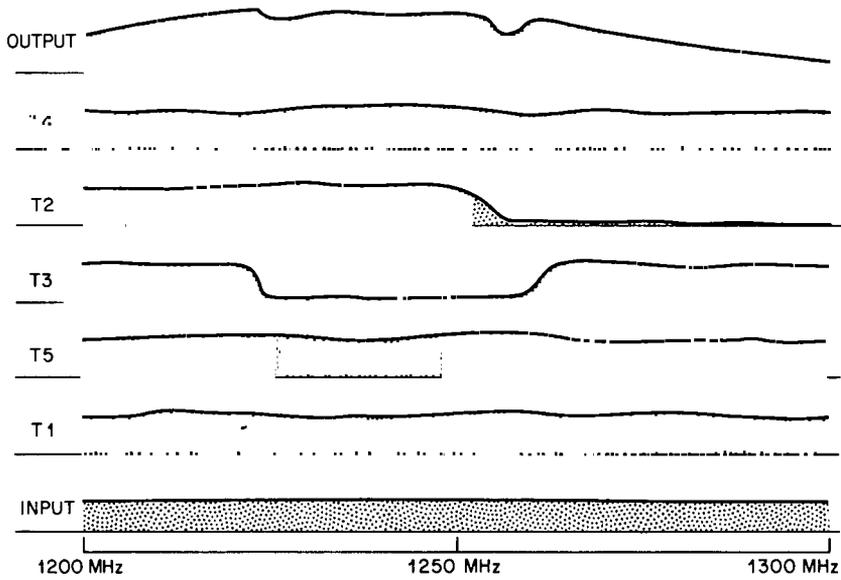


Fig. 7 — Detected response vs frequency

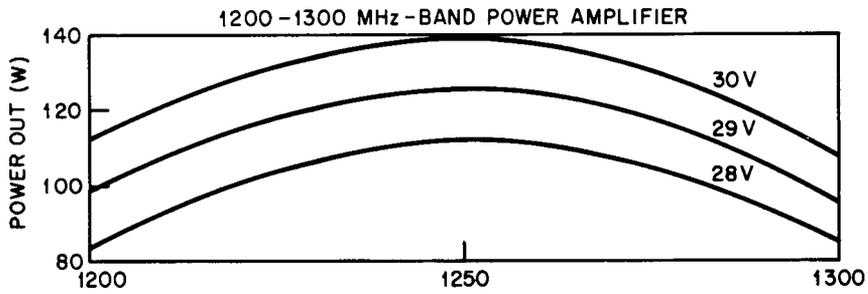


Fig. 8 — Output power vs frequency for 6.5-W input power at three supply voltages