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Tape Playback and Serial-Time Decoder for IFF Flight Test Instrumentation

CHARLES E. QUIGLEY

Security Systems Branch
Communications Sciences Division

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NAVAL RESEARCH LABORATORY
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ABSTRACT

The tape playback and serial-time decoder described in this report has been developed for evaluating event data recorded on magnetic tape during flight tests of the Hartlobe/Diversity dual-antenna system for airborne IFF transponders. Means are provided to recover pulse-duration-modulated (PDM)-multiplexed data from five playback channels of the instrumentation tape recorder to provide ten data channels for 35-mm oscillographic film records. Also, a serial-time code from another playback channel is used to synchronize an internal clock to provide the capability to superimpose on the oscillographic film record the time of day that the flight test data were originally recorded. Though the internal clock is primarily intended for use with the magnetic tape playback, a means is also available for operation as a completely self-contained, crystal-controlled, electronic clock with serial and parallel output signals.

PROBLEM STATUS

This is an interim report; work is continuing on other phases of the problem.

AUTHORIZATION

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TAPE PLAYBACK AND SERIAL TIME DECODER FOR IFF FLIGHT TEST INSTRUMENTATION

INTRODUCTION

A project at the Naval Research Laboratory, extending over almost ten years, has been devoted to research on a method for improving the radiation coverage of the IFF airborne transponder system. In October 1966, a detailed description was published in NRL Report 6401 of a method for using two physically separated antennas together with associated receivers and one or more transmitters in such a manner that the reply path is selected on the basis of which antenna receives the greater signal strength for a valid interrogation; this was termed the Hartlobe/Diversity dual-antenna system for airborne IFF transponders. Special measuring techniques and new instrumentation have been required to establish in quantitative terms that the Hartlobe/Diversity system provides a significant improvement under conditions where other pattern-improvement systems have proved inadequate.

In connection with flight tests conducted during Jan.-Mar. 1972 in cooperation with the Naval Air Training Center, Patuxent River, Md., the Aeronautical Systems Division, Wright-Patterson Air Force Base, Ohio, and the Air Force Aerospace Defense Command facility at Ft. Meade, Md., NRL equipped a single target aircraft with provisions for 35-mm oscillographic cameras, an electronic clock to provide time-of-day records on all data for subsequent time correlation with other data-collection sites, and strip-chart and magnetic-tape event records on an interrogation-by-interrogation basis. Though high-speed oscillographic waveforms were recorded on film in flight, evaluation of magnetic-tape event records requires subsequent tape playback onto 35-mm film by the use of a playback decoder and serial-time decoder designed to reproduce almost completely the events as they occurred during the actual flight. This report describes the playback decoder and serial-time decoder.

GENERAL DESCRIPTION

The playback decoder and serial-time decoder is designed to accept analog (gate) signals from six channels of a Lockheed Model 417 instrumentation tape recorder, which is equipped for FM recording, and to perform pulse-duration-modulated (PDM) decoding of up to two data channels on each of five playback channels. In addition, a serial-time code, shown in Fig. 1, is recovered from a sixth playback channel to generate a parallel-time word suitable to operate an electronic-readout numeric display designed to superimpose a six-digit, blinking-light time indication on the 35-mm, oscillographic continuous-film record of other data being recovered simultaneously from other tape-playback channels.

Figure 2 is a block diagram of the unit. In addition to the playback decoder, the unit includes an internal clock which provides a continuously available parallel-time word for use by the electronic-readout numeric display and a means to synchronize the internal clock periodically with a word derived from the serial-time code. To accomplish this

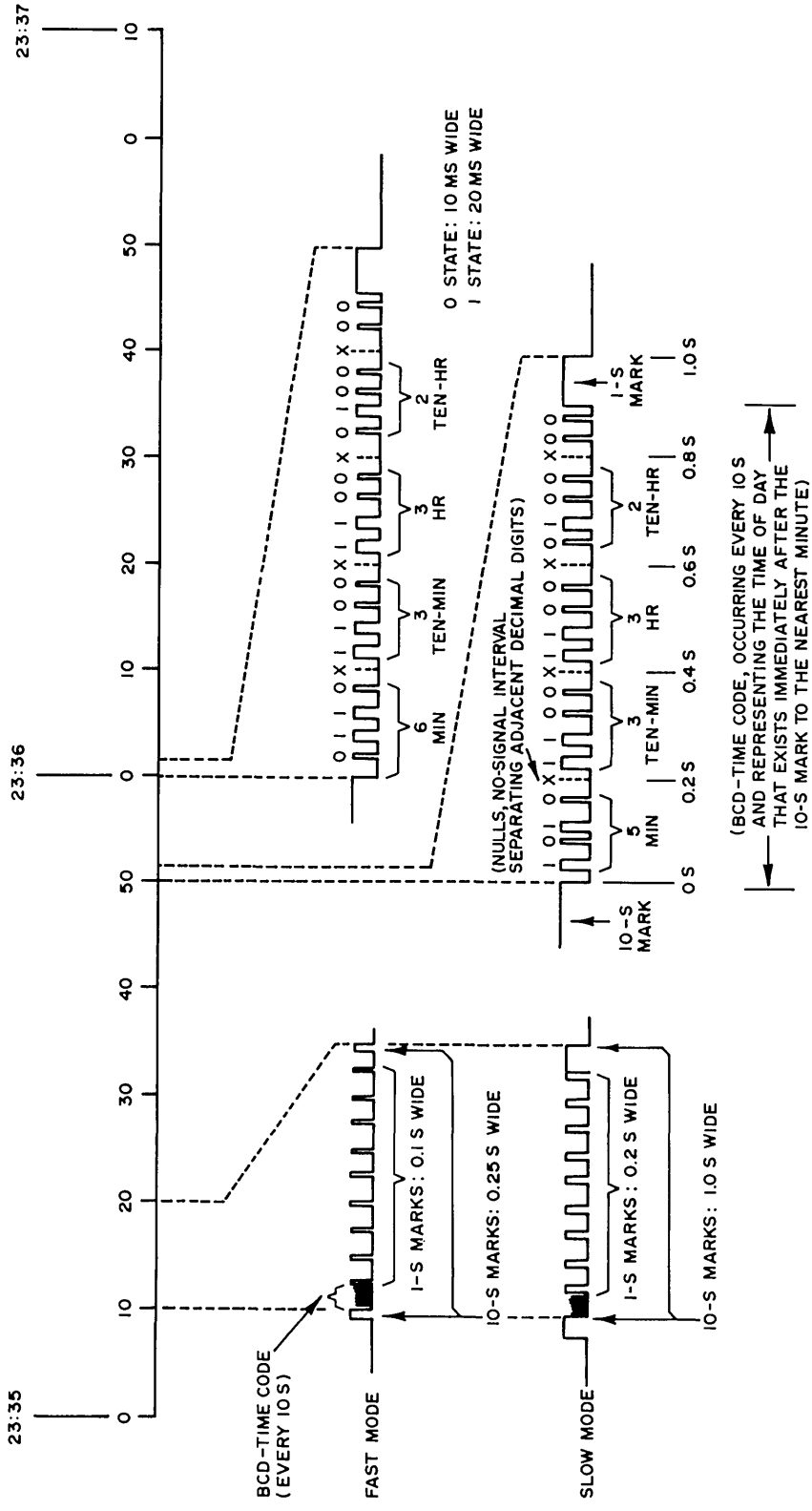

Fig. 1—Series-time code

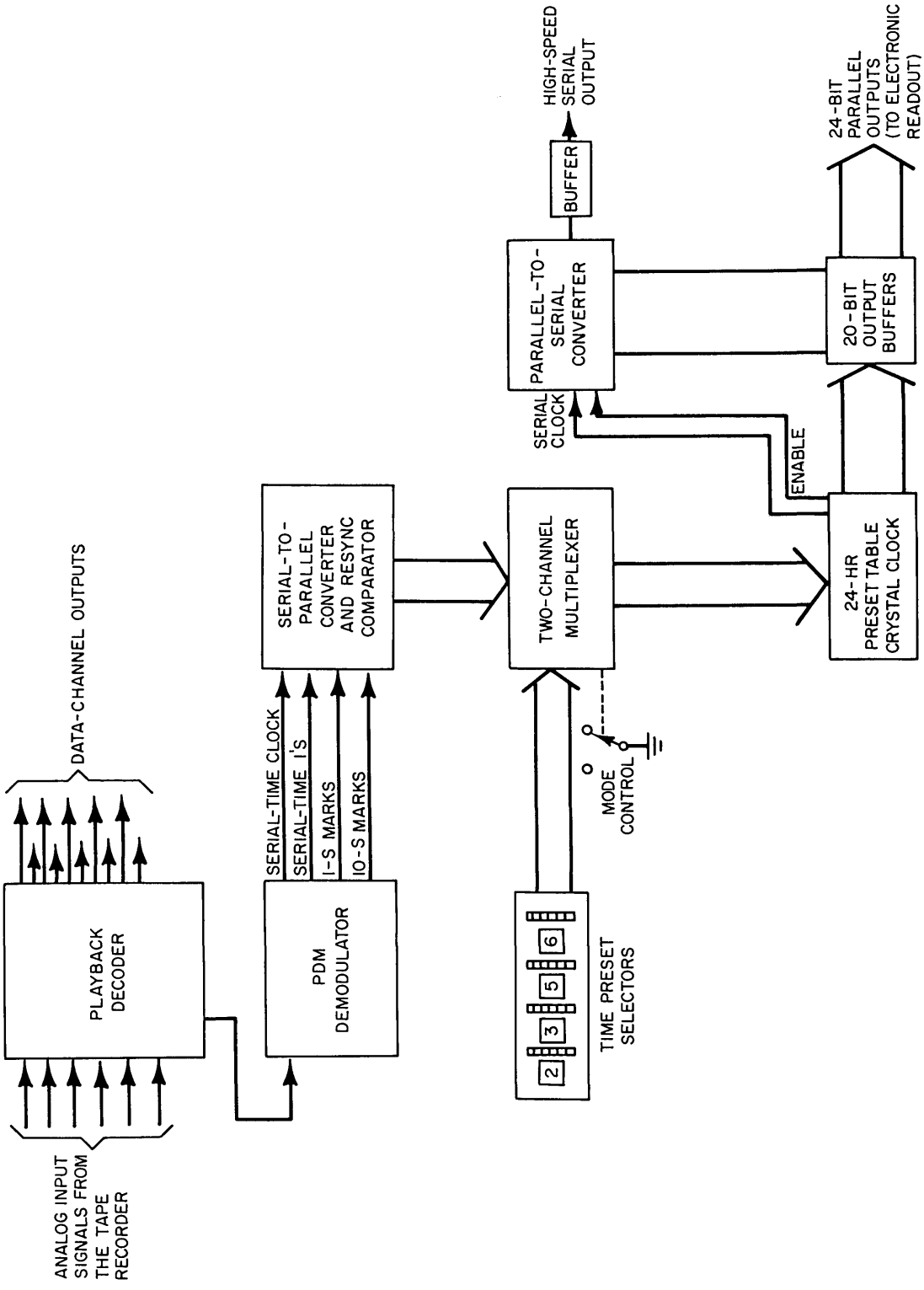

Fig. 2—Playback decoder and serial-time decoder

function, the serial-time PDM Demodulator separates the serial-time word into its component signals and periodically shifts the serial word into a serial-to-parallel converter. When a sync decoder determines that certain conditions about the serial-time word have been met, it instructs the internal clock to be preset in agreement with the serial-time word. In this manner, the internal clock is synchronized to the serial-time word to the nearest microsecond once each minute, minimizing any long-term time shift that might occur due to slight shift of the crystal-oscillator frequency used in the internal clock and also due to tape-speed variations and tape stretch resulting from normal handling. In addition to a parallel-time word, the clock has provisions for a high-speed, six-digit, serial-time code for operation of other displays or instrumentation.

PLAYBACK DECODER

The playback decoder section is equipped to accept six input channels of analog signals from an FM instrumentation tape recorder such as the Lockheed Model 417. The serial-time signal from the recorder is converted directly to fast-rise-time and fast-fall-time signals having levels and source impedances compatible with TTL logic. The signals from the remaining five channels are, in addition, PDM demodulated to produce ten output signal channels suitable for producing oscilloscope waveforms for 35-mm, moving-film oscilloscope photography or for use by other digital logic.

Tapes made during early 1972 Hartlobe/Diversity flight tests were recorded in the target aircraft at 7-1/2 inches per second by the FM method. Under these conditions, the manufacturer reports the frequency response to be 0 to 2500 Hz between the ±0.5-dB points. Maximum allowable input and output signal levels are ±1.4 V peak (1.0 V RMS) for full carrier deviation, with RMS-signal-to-RMS-noise quoted at 40 dB, measured across the recorder pass band. The FM record system is employed because of its excellent phase response, allowing faithful reproduction of gates as narrow as 300 μs in width. This method allows a number of possible schemes for simultaneously multiplexing several channels of data on a single record channel, including the use of positive-going and negative-going gates or of PDM signals, the method employed here. These techniques are all relatively limited in data rate by the restricted pass band, though the problem is partially solved by carefully pairing the data channels on each record channel in such a way that signals can never occur simultaneously on both data channels.

For purposes of data recovery during tape playback, a general-purpose, dual-Schmitt-trigger board QST1 has been developed to perform the functions of adjustable thresholding, high-speed leading-and-trailing-edge transition, and the majority of PDM decoding functions on a single logic card for each signal input channel from the tape recorder. Figure 3 comprises a logic diagram of the complete playback decoder section and a schematic diagram for a tpyical schmitt-trigger board. An integrated-circuit comparator is used to compare the analog input signal from the tape recorder against a threshold of +0.5 V. Whenever the analog input signal exceeds this threshold, the comparator output rapidly swings positive, driving transistor Q1 into conduction. Time constant C1 and R4 provides frequency compensation for the comparator to help speed up the positive-going transition. Transistors Q1 and Q2 together with associated resistors and capacitor C2 constitute the basic Schmitt-trigger circuit; transistor Q3 is an inverting output amplifier.

The inverted output $\overline{Q}$ of the Schmitt trigger is fed to a network of four monostable flip-flops (FF), two of which are located on the Schmitt-trigger board and two of which are part of an output monostable board. The positive-going trailing edge of the Schmitt-trigger

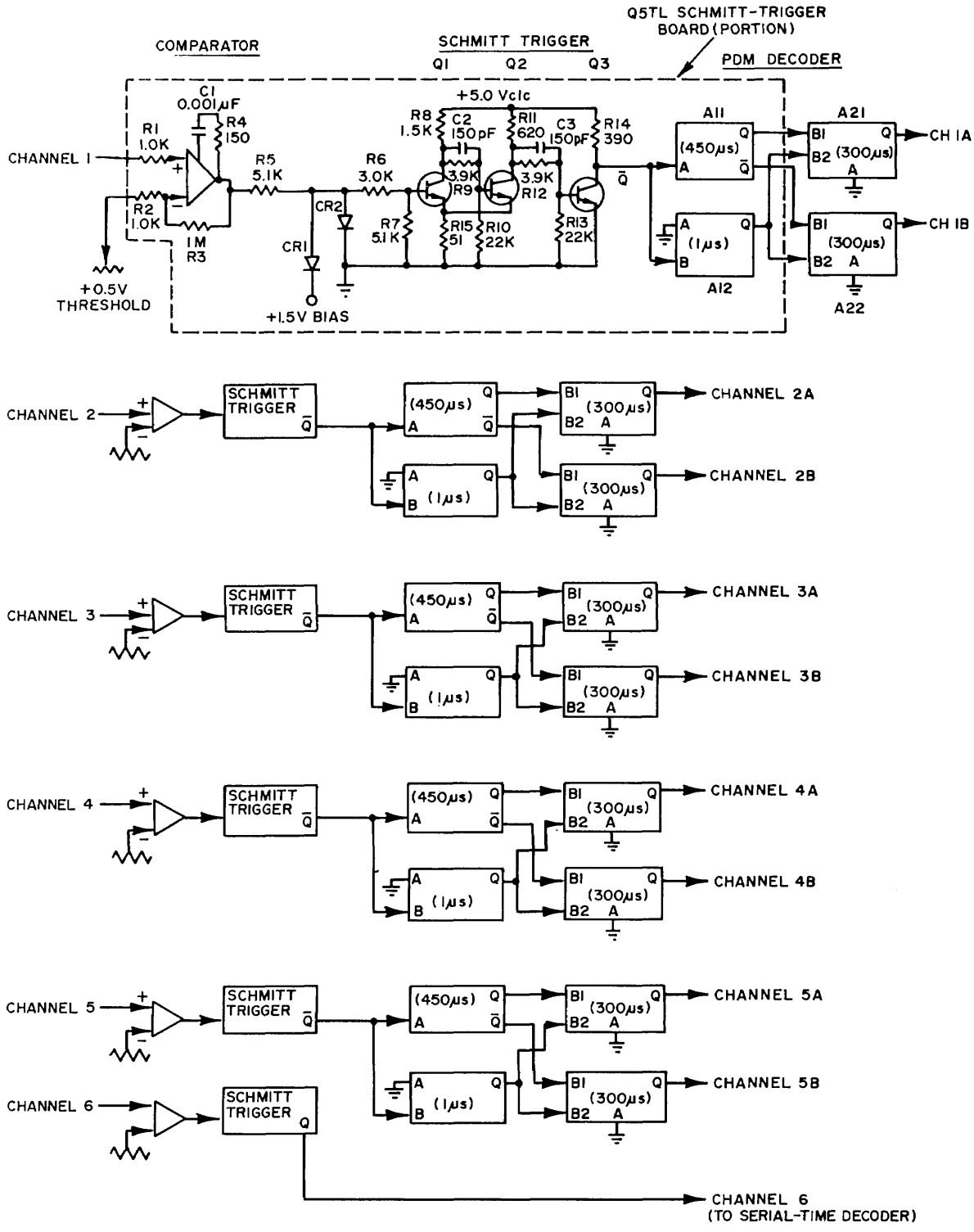

Fig. 3—Playback decoder

$\overline{Q}$ output triggers monostable FF A12-Q high for approximately 1 μs. The negative-going leading edge of Schmitt-trigger $\overline{Q}$ output triggers monostable FF A11-Q high for 450 μs, enabling a NAND with monostable FF A21 and inhibiting a NAND within monostable FF A21 for the same time interval. If the Schmitt-trigger output gate is less than 450 μs, the positive trigger corresponding to the trailing edge will trigger monostable FF A21-Q high for 300 μs, but not FF A22-Q. If the Schmitt-trigger output gate is greater than 450 μs, then the positive trigger corresponding to the trailing edge will instead trigger monostable FF A22-Q high for 300 μs, but not FF A21-Q. In general, the two different pulse widths multiplexed on the same signal channel are approximately 300 to 600 μs, so that PDM decoding can be accomplished reliably, despite moderate variations in signal gate widths due to tape noise and despite expected variations in the 450-μs gate width with normal operating conditions. It should be noted that the PDM-decoder output in each case occurs coincident with the trailing edge of the signal input from the tape recorder, so that one must take account of the original signal width to establish the time of occurrence of a given event. This is important when attempting to establish simultaneity of two events occurring on two different signal input channels.

SERIAL-TIME PDM DEMODULATOR

Logic board X01 together with the appropriate interface circuits provide all the functions required to separate the serial-time code into its component parts which are suitable for subsequent serial-to-parallel-conversion and sync-comparison functions. Fig. 1 shows the serial-time code generated by the electronic clock on board the target aircraft to record time serially on strip charts and on one channel of the Lockheed 417 tape recorder. The choice of this relatively slow serial code, consisting of 1-s and 10-s time marks together with a four-digit, BCD-time code every 10s, was determined primarily by pen-response limitations of the associated strip-chart recorders rather than by the somewhat wider pass band of the tape recorder. The BCD-time code consists of a 16-bit PDM pulse train grouped in sets of four bits, each group separated by a gap or null which is provided to simplify determination of bit position on an oscilloscope or strip-chart record. Within the BCD-time code, a binary-0 pulse is only 10 ms wide, and a binary-1 pulse is 20 ms wide. Also included in the electronic clock is a means for providing the serial-time code to the tape recorder for a fast-or-slow-time-mark mode, depending on whether a fast or slow chart speed is selected on the accompanying strip-chart recorder.

Figure 4 is a schematic diagram of the interface circuit required for use with the serial-time PDM demodulator. Functionally, it accepts inputs from either a front-panel connector or from the uninverted output of the associated Schmitt-trigger board and consists of an inverter (Q1, Q2, and Q3) and a gated relaxation oscillator and output buffer (Q4 and Q5). The inverter output ($\overline{\text{Serial Time}}$) is buffered to drive up to three unit loads of DTL or TTL logic. The relaxation oscillator consisting of unijunction transistor Q4 and time constant R9, R10, and C1 and is gated on by amplifier Q2 to produce a 15-ms clock train during the time interval of each serial-time pulse. Following each serial-time pulse, timing capacitor C1 discharges through diode CR2 and resistors R5 and R6 to ensure that the first clock pulse always occurs at the same time interval following the leading edge of each new serial-time pulse.

Figure 5 is a simplified logic diagram of the serial-time PDM demodulator, and Fig. 6 is a set of timing diagrams for each of the four possible pulse widths evaluated (Fig. 6a shows examples of the two different-width, BCD-time code pulses; Fig. 6b shows the case of the two different-width time marks). The PDM demodulator consists of two

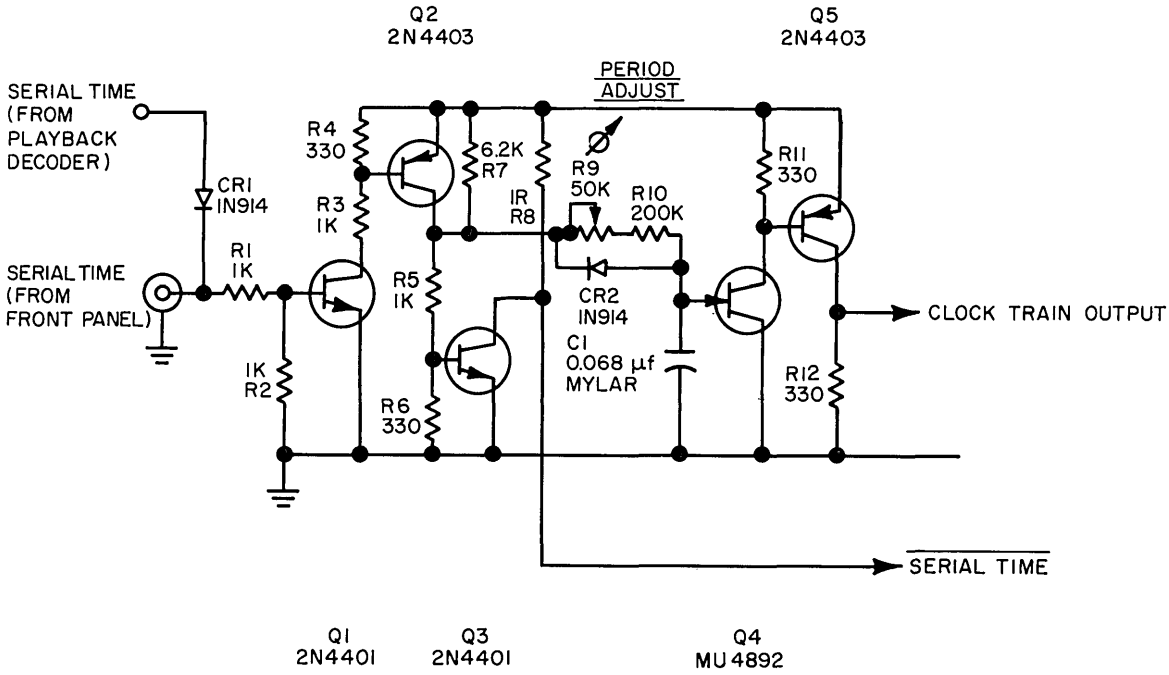

Fig. 4—Shaper and clock-train generator for the serial-time decoder

monostable flip-flops (A14 and A12) to differentiate the leading and traling edges of the incoming serial-time pulse, a set of acceptance gates derived from the 15-ms clock by means of two cascaded BCD counters (A11 and A7), associated BCD-to-decimal decoders (A9 and A5), bistable FF A13b, NAND gates A3, A4a, A4b, and A4c, and output monostable flip-flops A10, A8, and A6.

Operation can be described as follows. Initially FF A13a-$\overline{Q}$ is high, resetting counters A11 and A7, and FF A13b-Q is low. The leading edge of the serial-time pulse switches monostable FF A14-$\overline{Q}$ (TP11) low for 1 μs, setting FF A13a-$\overline{Q}$ low and allowing counters A11 and A7 to begin accepting 15-ms clock input triggers, which commence 15 ms after the serial-time-pulse leading edge. The trailing edge of the serial-time pulse switches monostable FF A12-Q (TP13) high for 1 μs, passing whichever of NAND's A3, A4a, A4b, and A4c are enabled at that instant by the acceptance gates. The negative-going trailing edge of the pulse from A12-Q also clocks flip-flops A13a-$\overline{Q}$ and A13b-$\overline{Q}$ high, thereby restoring the PDM demodulator to its rest condition in preparation for the next serial-time pulse.

Operation of the acceptance gates can be seen by examining the timing diagrams of Fig. 6. If the serial-time pulse corresponds to a BCD-code pulse of binary-0 state, then the trailing-edge pulse from A12-Q (TP13) occurs about 10 ms after the leading-edge pulse, prior to the first 15-ms clock input pulse. At this time, counter A11 is in the decimal-0 state, so that decoder A9-$\overline{0}$ is low, thus inhibiting one input of NAND A4a. Also at this time, FF A13b-Q is high, enabling one input of NAND's A3 and A4a, and the Serial-Time Clock Enable gate from the Serial-to-Parallel Converter is high, having been triggered high for 0.8 s by the 10-Second Trigger output just preceding the BCD-time code. Consequently, the trailing-edge trigger from A12-Q (TP13) passes NAND A3 (and is inverted) to appear at the $\overline{\text{Serial Clock}}$ output (TP35).

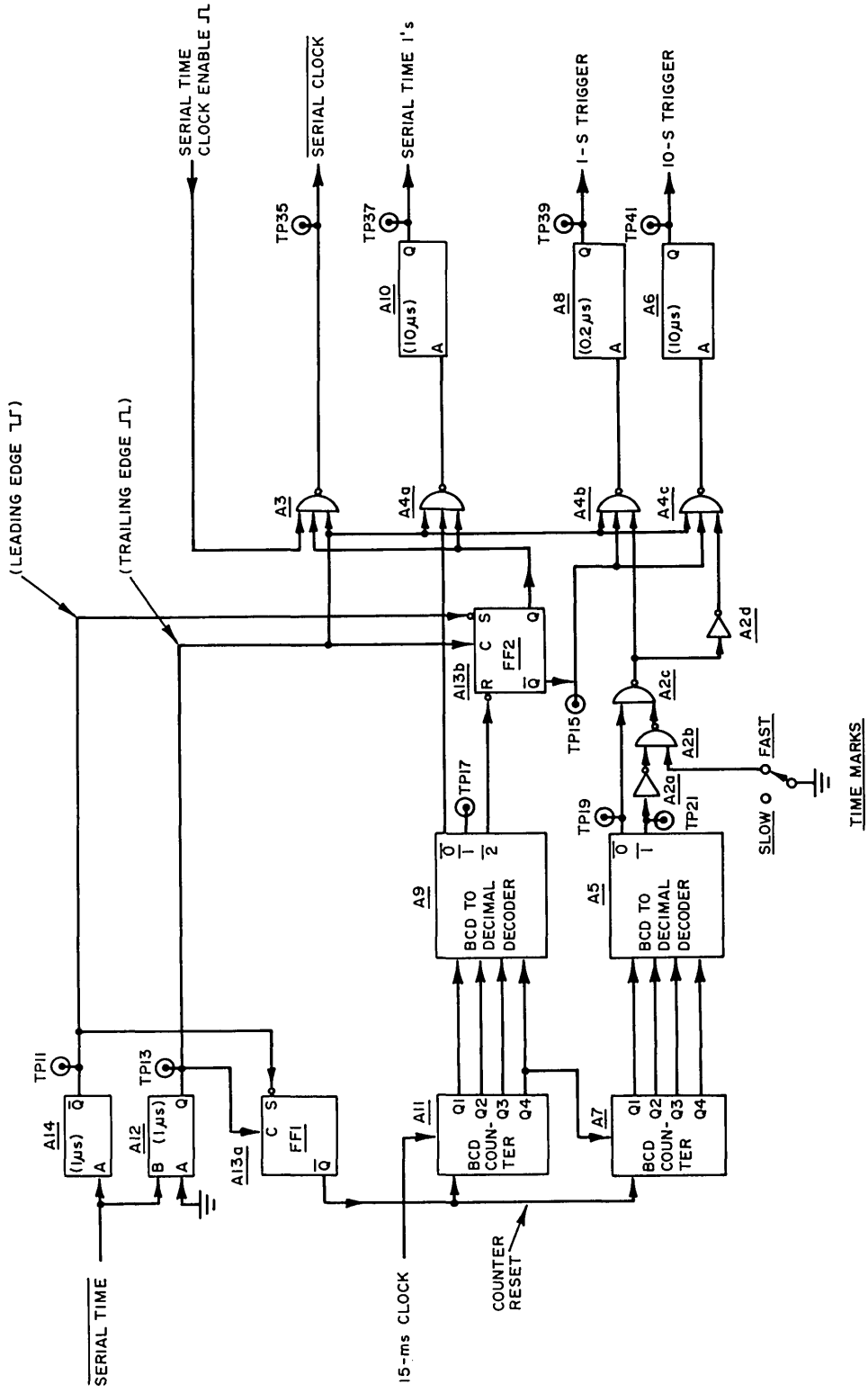

Fig. 5—Serial-time PDM demodulator

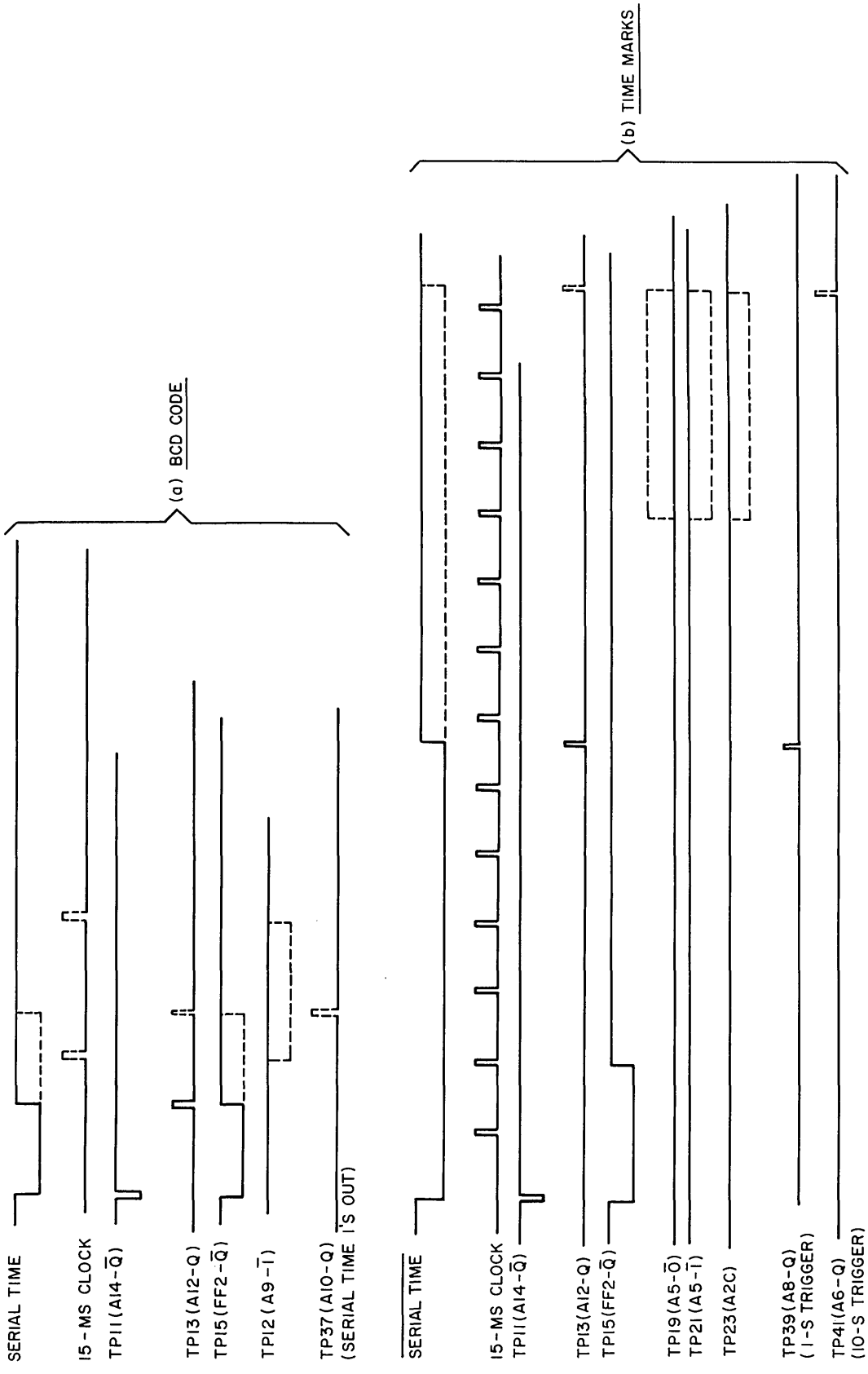

Fig. 6—Timing for the serial-time PDM demodulator

If the serial-time pulse corresponds to a BCD-code pulse of binary-1 state, then the trailing-edge pulse from A12-Q (TP13) occurs about 20 ms after the leading edge and after the first clock input pulse, at which time counter A11 steps to the decimal-1 state, causing decoder A9-$\overline{0}$ to go high and A9-$\overline{1}$ (TP17) to go low, enabling one input of NAND A4a. Consequently, since FF A13b-Q remains high without change, the trailing-edge trigger from A12-Q (TP13) passes NAND A4a to trigger monostable FF A10-Q (TP37) high for 10 μs (Serial-Time 1S output), as well as passing NAND A3 to appear (inverted) at the $\overline{\text{Serial Clock}}$ output (TP35).

If the serial-time pulse corresponds to a time mark, the trailing-edge pulse occurs long after the second clock input pulse, at which time counter A11 steps to the decimal-2 state, causing decoder A9-$\overline{2}$ to go low, thereby resetting FF A13b-Q low, inhibiting NAND's A3 and A4a, and preventing subsequent-occurring trailing-edge pulses from appearing at the $\overline{\text{Serial Clock}}$ output (TP35). If the fast-time-marks mode has been selected, one input of NAND A2b is inhibited, forcing its output high and enabling NAND A2a to pass (and invert) decoder A5-$\overline{0}$ to one input of NAND A4b and to pass (uninverted) the same signal to one input of NAND A4c. (The second input to both NAND's A4b and A4c from FF A13b-$\overline{Q}$ (TP15) is high following the second clock input pulse.) Consequently, if the serial-time pulse corresponds to a 1-s time mark, then the trailing-edge pulse occurs about 100 ms after the leading edge, namely after the sixth clock pulse; at this time counter A7 remains in the decimal-0 state, so that decoder A5-$\overline{0}$ (TP19) is low, thereby enabling NAND A4b to pass the trailing-edge trigger and causing monstable A8-Q (TP39) (1-s Trigger output) to switch high for 0.2 μs (essentially coincident with the serial-time-pulse trailing edge).

If the serial-time pulse corresponds to a 10-s time mark, then the trailing-edge pulse occurs about 200 ms (fast-time-mark mode) following the leading edge, namely after the thirteenth 15-ms clock input pulse; at this time counter A7 has stepped to the decimal-1 state, so that decoder A5-$\overline{0}$ (TP19) has switched high, thereby inhibiting NAND A4b and enabling NAND A4c to pass the trailing-edge trigger, which causes monostable FF A6-Q (TP41) (10-Second Trigger out) to switch high for 10 μs coincident with the serial-time-pulse trailing edge.

Returning to Fig. 5, one should notice that if the time-marks switch is instead in the SLOW position, the output of NAND A2c is high as long as either decoder A5-$\overline{0}$ or A5-$\overline{1}$ is low. Consequently, NAND A4b is enabled (and NAND A4c is inhibited) from passing trailing-edge triggers in the slow-time-marks mode up to the twentieth clock input trigger (namely for the first 300 ms), so that the trailing-edge trigger for a 1-s time mark occurring 200 ms following the leading edge passes NAND A4b and generates a 1-s trigger.

However, if the slow-time-mark mode is selected, then a 10-s-time-mark trailing edge occurs one second following the leading edge (actually merging with the next previous 0.2-s wide, 1-s time mark to form a pulse having a total width of approximately 1.2 s). At this time, approximately 79 or 80 clock input triggers have occurred, at which time counter A7 has stepped to the decimal-7 or decimal-8 state, so that decoder A5-$\overline{0}$ and A5-$\overline{1}$ are both high, inhibiting NAND A4b and enabling NAND A4c to pass the trailing-edge trigger thereby generating a 10-s trigger.

Note that the character of the serial-time code in the slow-time-marks mode makes it impossible to avoid loss of the ninth 1-s mark each 10-s period. However, the remainder of the serial-time decoder is so configured that this loss has no effect on synchronization of the internal clock or on the parallel-time world.

SERIAL-TO-PARALLEL CONVERTER AND SYNC COMPARATOR

Logic board X02 performs the dual function of serial-to-parallel conversion of the BCD-time code and of sync comparison to determine when to update the internal clock with the resulting parallel-time word. It can be seen by examining the serial-time code shown in Fig. 1 that, in the event the tape playback of the serial-time code from the electronic clock in the target aircraft is abruptly restarted at some new time of day, the new time could be established to the nearest minute following the next complete BCD-time code no more than 10 s after the interruption. To reestablish the time of day to the nearest second, one would have to wait until the end of the sixtieth second of a given minute, at which time the BCD-time code immediately following would signify a time of day different from that of the previous 10-s interval. Precise synchronization using this new time word can be performed at the trailing edge of the first 1-s time mark immediately following the new BCD-time code. Synchronization is obtainable to better than 1 μs (on the average) at this instant, since the negative-going trailing edge of any time mark is precisely timed with respect to the timing source in the electronic clock.

Figure 7 is a simplified logic diagram of the serial-to-parallel converter and sync comparator. It consists of two shift registers, a parallel-word comparator, and enable and decision-storage logic. Each shift register is as long as a single 16-bit, BCD-time-code word, so that following each serial word, shift register A holds the current time word and shift register B holds the previous time word. The words are so located that corresponding bits of the time word are compared. Immediately following the storage of a new time word in shift register A, the comparator decision is strobed, and if the two words are not equal, this condition is stored until the beginning of the next second, at which time the internal clock is synchronized to the current time word.

Figure 8 shows a timing diagram for the serial-to-parallel converter for a more detailed analysis of the time-word comparison. For this example, one assumes that the electronic clock delivering the serial-time code has been running without interruption for more than a minute and that the time of day is now 23:35:59, namely 23 hours, 35 minutes, 59 seconds. Initially, then, just prior to the instant shown in Fig. 8, the 16-bit serial word, representing the four most significant decimal digits and stored in shift register B in parallel form, is exactly the same as the word in shift register A, and bit-for-bit comparison indicates that the two words are equal. At the end of the sixtieth second, the 10-s-trigger output of the PDM demodulator, representing the trailing edge of the 10-s mark, causes monostable FF A5-Q to switch high for approximately 0.8 s, a sufficient interval to enable shift registers A and B to accept the full 16-bit, BCD-time-code word and to enable NAND A3 in the PDM demodulator to pass no more than 16 serial-time clock pulses.

At this instant, the left half of Fig. 8 shows the timing diagram as the new time of day 23:36 (word 2) enters shift register A, reading from left to right, and is shown for bit position 1 (TP13) on the top line through bit position 16 on the bottom line. One should notice that the word appearing at any bit position is delayed in time by one clock-pulse interval from that word in the next lower order bit position, so that at the end of 16 serial-time clock pulses the current serial-time word is entirely contained within shift register A, with the least significant bit at bit position 16 and the most significant bit at bit position 1.

In the same time interval, the right side of Fig. 8 shows a timing diagram as the previous time word 23:35 (word 1) enters shift register B, reading in the same order, with the word entering bit position 1 (TP15) of shift register B from bit position 16 of shift

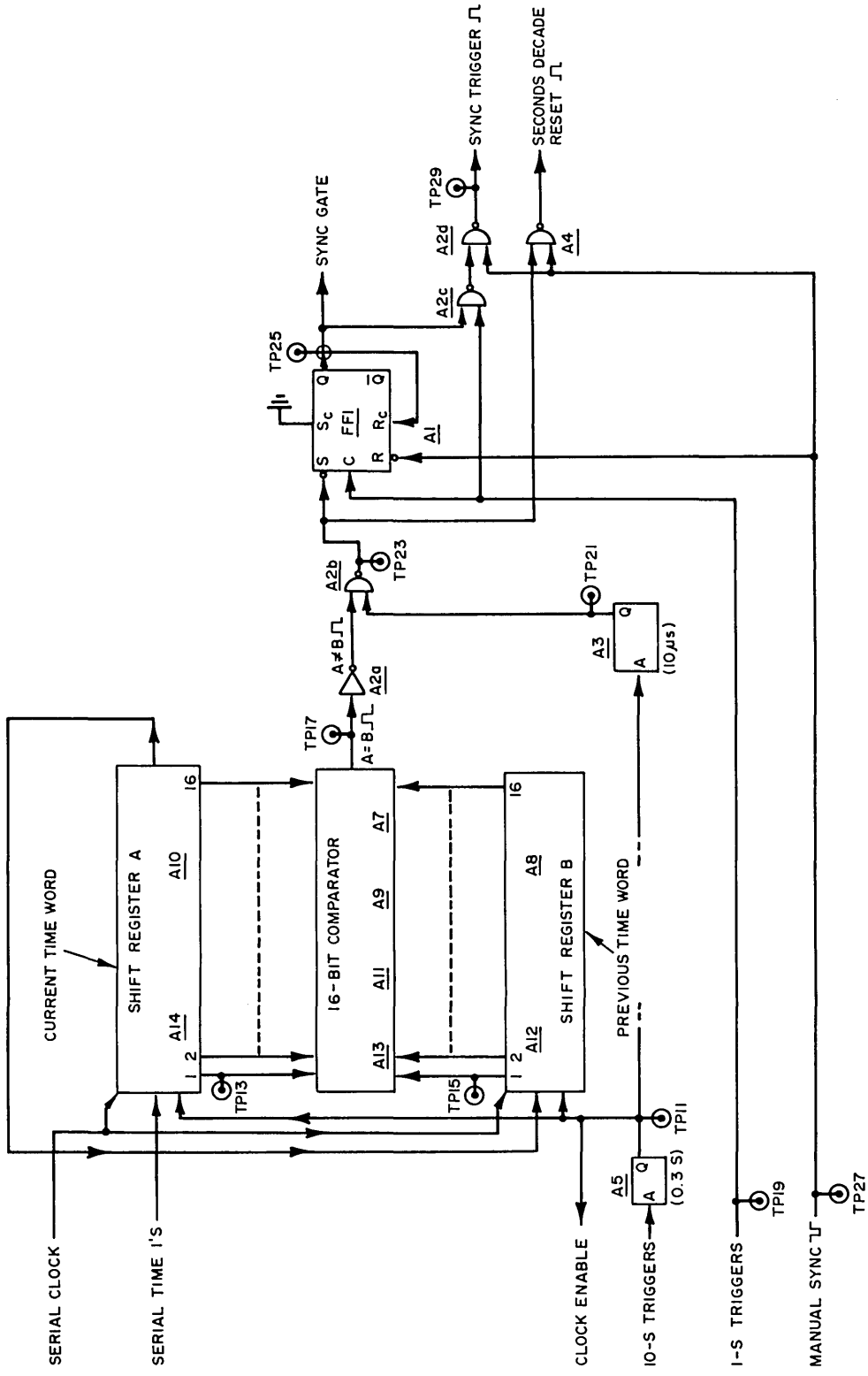

Fig. 7—Serial-to-parallel converter and sync comparator

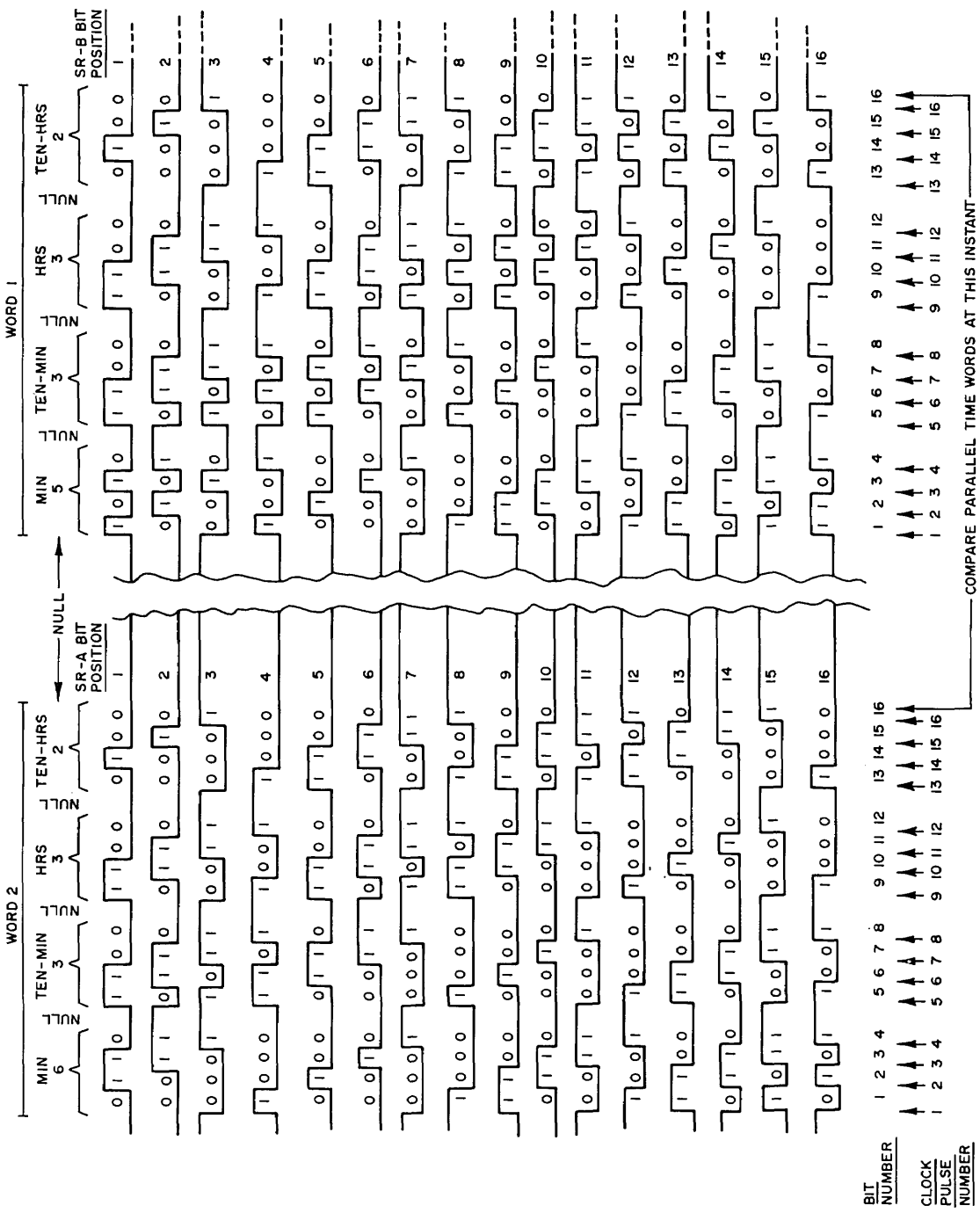

Fig. 8—Timing for the serial-to-parallel converter

register A. In the same manner, the previous serial-time word appears at the various bit positions of shift register B at the end of the serial-time clock train.

Following clock pulse 16, word 2, appearing at the taps of shift register A, and word 1, appearing at the taps of shift register B, are compared. The trailing edge of the 0.8-s gate from monostable FF A5-Q (TP11) triggers monostable FF A3-Q (TP21) high for 10 μs. If inequality exists at this instant, the comparator A = B output (TP17) is low at this time, and the output of inverter A2a is high, thereby enabling NAND A2b to pass (and invert) the trigger from A3-Q to appear (uninverted) as the seconds-decade reset trigger output and to set FF A1-Q (TP25) high, enabling NAND A2c. The next 1-s trigger input (TP19) from the PDM demodulator, approximately 0.2 μs wide, passes NAND's A2c and A2d to appear at the sync trigger output (TP29); also the negative-going trailing edge of the 1-s trigger input (TP19) from the PDM demodulator resets FF A1-Q (TP25) low, thereby inhibiting NAND A2c from passing any subsequent 1-s triggers. The sync gate appearing at FF A1-Q (TP25), approximately 0.2 s wide, also energizes a front-panel sync lamp through a transistor buffer amplifier (not shown).

In addition to synchronization of the internal clock to a parallel-time word derived from the BCD-time code by the PDM demodulator and serial-to-parallel converter, this unit also is equipped to synchronize to a manually selected four-digit time word. Consequently, the sync comparator also has provisions to synchonrize manually either by means of a pushbutton or by an external trigger using a transistor inverter (not shown). In this mode of operation, the seconds-decade reset trigger and the sync trigger are generally sinultaneous. Also, FF A1-Q is reset low by this means, thereby avoiding continuous illumination by the sync lamp should FF A1 happen to be set inadvertently at the time primary power is first applied.

INTERNAL 24-HR CLOCK AND OUTPUT SHIFT REGISTER

Logic boards X03 and X04 function together as a completely self-contained, crystal-controlled, 24-hr clock and include the crystal oscillator. In addition to providing continuously available parallel outputs, the clock also includes a serial-output coder providing the complete 6-digit time of day at the beginning of each new second. Though these two boards are functionally separable, they are discussed together in this section.

Figure 9 is a simplified logic diagram of the internal clock and output shift register. Logic board X03 contains a 10-MHz crystal oscillator and a seven-decade BCD counter, together with provisions to reset the last six decades, thereby allowing synchronization to the entire internal clock to the nearest microsecond. The board also contains all timing and gating logic necessary to generate the output-shift-register clock, the output-BCD-coder clock, and a shift-register-preset enable gate (shift/load control), required for the serial-output circuit. Logic board X04, in addition to the serial-output shift register and output BCD coder, contains a six-decade, BCD counter with feedback loops necessary to count 1-s triggers from board X03 and generate six-decimal digits representing the time of day.

Synchronization of logic board X04 to an external time source, such as serial-to-parallel converter board X02 or the front-panel time selector switches, is accomplished in the following manner. The seconds decade is reset by a second-reset trigger from the sync comparator, board X02, immediately on recognizing that the current and previous BCD-time codes do not agree, at which time the front-panel sync lamp turns on. Approximately 0.2 s later, when the sync lamp extinguishes, the sync comparator generates a sync trigger

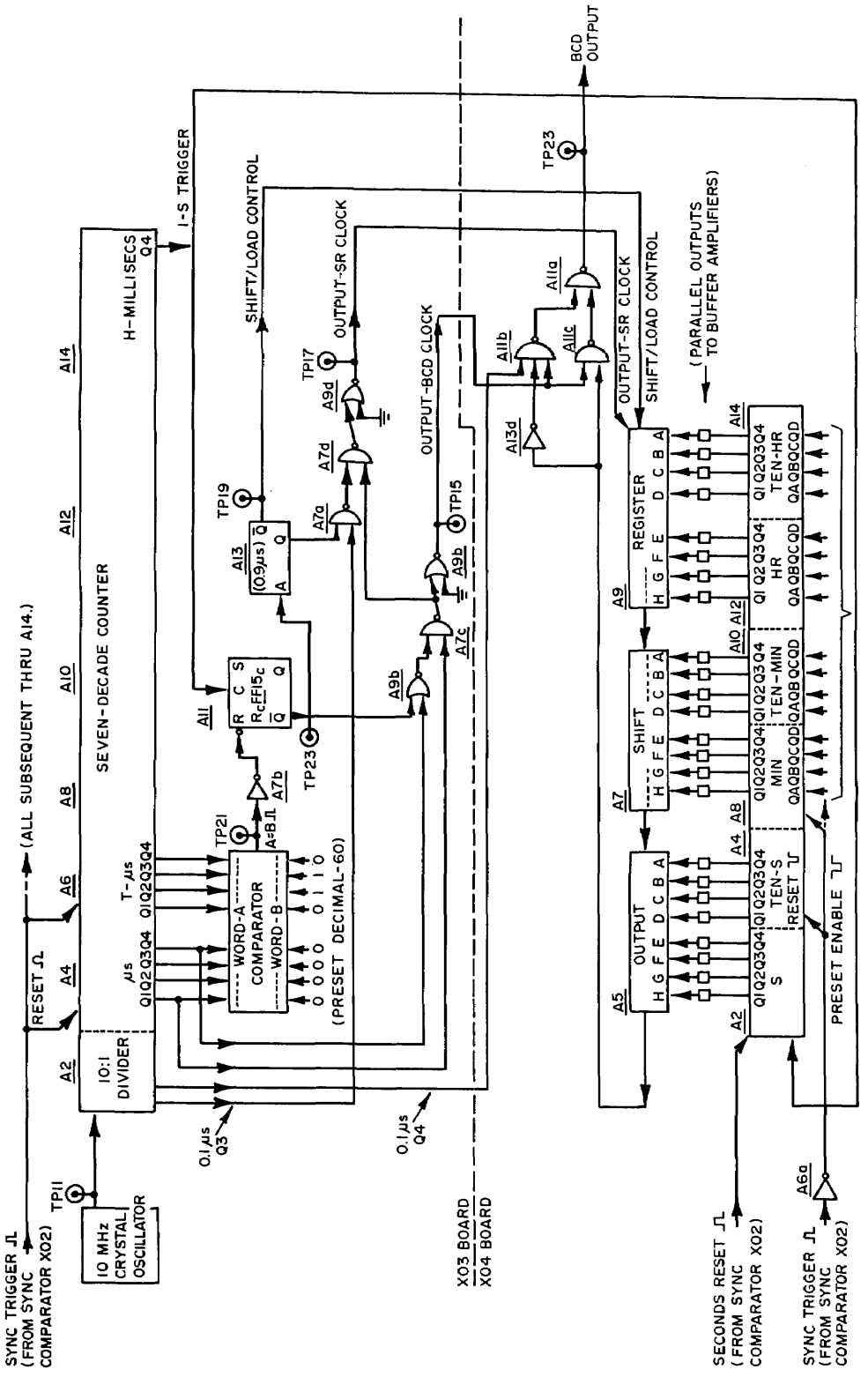

Fig. 9—Internal clock and output shift register

which resets the last six decades of internal clock board X03 and the ten-seconds decade of board X04 and also presets the last four decades of board X04 to agree with the selected external time source at that instant (within 0.2 μs of the 1-s-time-mark trailing edge). Provided that the hundred-milliseconds Q4 output from board X03 is high at the instant the sync trigger resets that decade, the negative-going 1-s trigger to the seconds decade on board X04 steps that decade (previously reset) to the decimal-1 state at the same instant the five remaining decades on board X04 are synchronized. In this manner, correct synchronization occurs at the end of the first second in each new minute of the (externally supplied) BCD-time code.

Operation of the output shift register and output BCD coder located on board X04 can be described as follows. The timing waveforms are shown in Fig. 10. At the beginning of each new (internal-clock) second, the clock timing logic on board X03 delivers a train of output-SR clock pulses and a preset enable gate such that the leading edge of the first clock pulse presets the 24-bit shift register to accept the contents of the six decade counters at that instant. Subsequent output-SR clock pulses shift the time word to the left, starting with the least significant bit of the seconds digit and ending with the most significant bit of the ten-hours digit. Prior to each shift of the time-word, the left-most bit is read into the BCD coder in such a way as to select either of two output pulse widths, namely 0.2 μs in the event of a binary 0 and 1.0 μs in case of a binary 1, such that the negative-going trailing edges are spaced 2 μs within a single 4-bit group, with 4 μs separating consecutive groups. In this manner, the time word is initially loaded into the output shift register, the first bit is read by the output-BCD coder, the word is shifted one bit, the second bit is read, the word is shifted another bit, the third bit is read, and so on. The entire 24-bit time word is read out serially at the beginning of each new second, requiring a time interval of slightly less than 60 μs, as shown in the example of Fig. 8.

Generation of the various clock-train and control waveforms required to operate the shift register and BCD coder can be described as follows. Timing waveforms are shown in Fig. 11. The negative-going trailing edge of each 1-s trigger (hundred-milliseconds-Q4) clocks bistable FF 1-$\overline{Q}$ low, triggering monostable FF A13-$\overline{Q}$ (TP19) for 0.9 μs and allowing NOR A9b to pass 2.0-μs-duration gates from the microseconds-decade Q4 output. So long as the output of NOR A9b is high, occurring whenever FF 1-$\overline{Q}$ and microseconds-decade Q4 output are both low, then NAND A7c will pass 1-μs gates from the microseconds-decade Q1 output through NOR A9b, connected as an inverter, to become the output-BCD clock. However, whenever the microseconds-decade Q4 is high, NAND A7c blocks one 1-μs gate from the microseconds-decade Q1 from reaching the output-BCD clock line, thereby resulting in bursts of four successive 1-μs gates, followed by a gap where a 1-μs gate would otherwise appear.

In like manner, the inverted output-BCD clock train appearing at the output of NAND A7c is passed by NAND A7d and inverted by NOR A9b (TP17) to become the output-SR clock whenever the output of NAND A7a is high, namely whenever either the monostable FF A13-Q or 0.1-μs-decade Q3 output is low. Since a ripple-through, TTL, seven-decade counter is used to generate 1-s triggers, the trailing edge of the hundred-millisecond Q4 output occurs approximately 0.2 μs after the negative-going trailing edge of the 0.1-μs-decade Q4 output which produces it. The duration of monostable FF A13 is timed such that NAND A7a passes only the first 0.4-μs gate from the 0.1-μs decade Q3 each second, and NAND A7d negative-OR's this 0.4-μs gate with the inverted output-BCD clock to obtain the output-SR clock train. The function of the preset enable gate provided by monostable FF A13-$\overline{Q}$ (TP19) is to instruct the shift register to be preset with a new time word on the positive-going leading edge of the output-SR-clock first pulse (when the

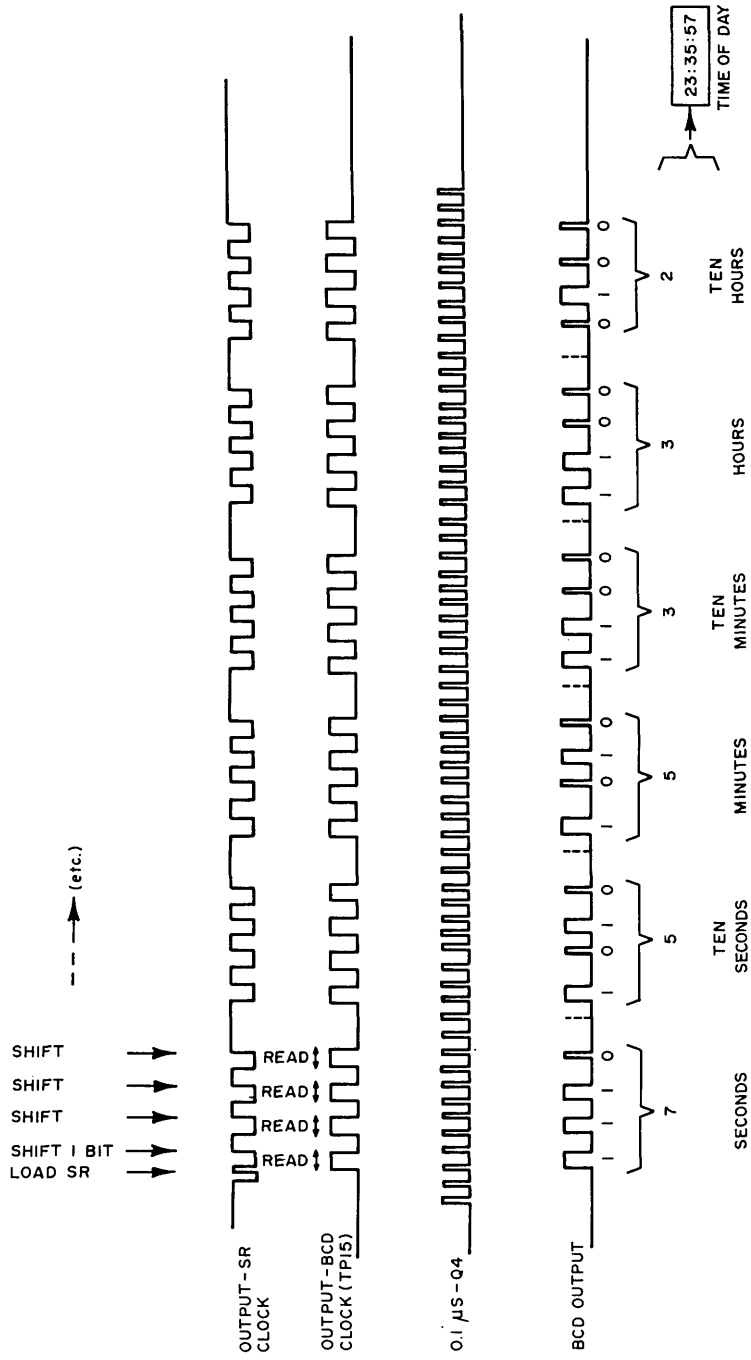

Fig. 10—Timing waveforms for the output shift register and output BCD coder

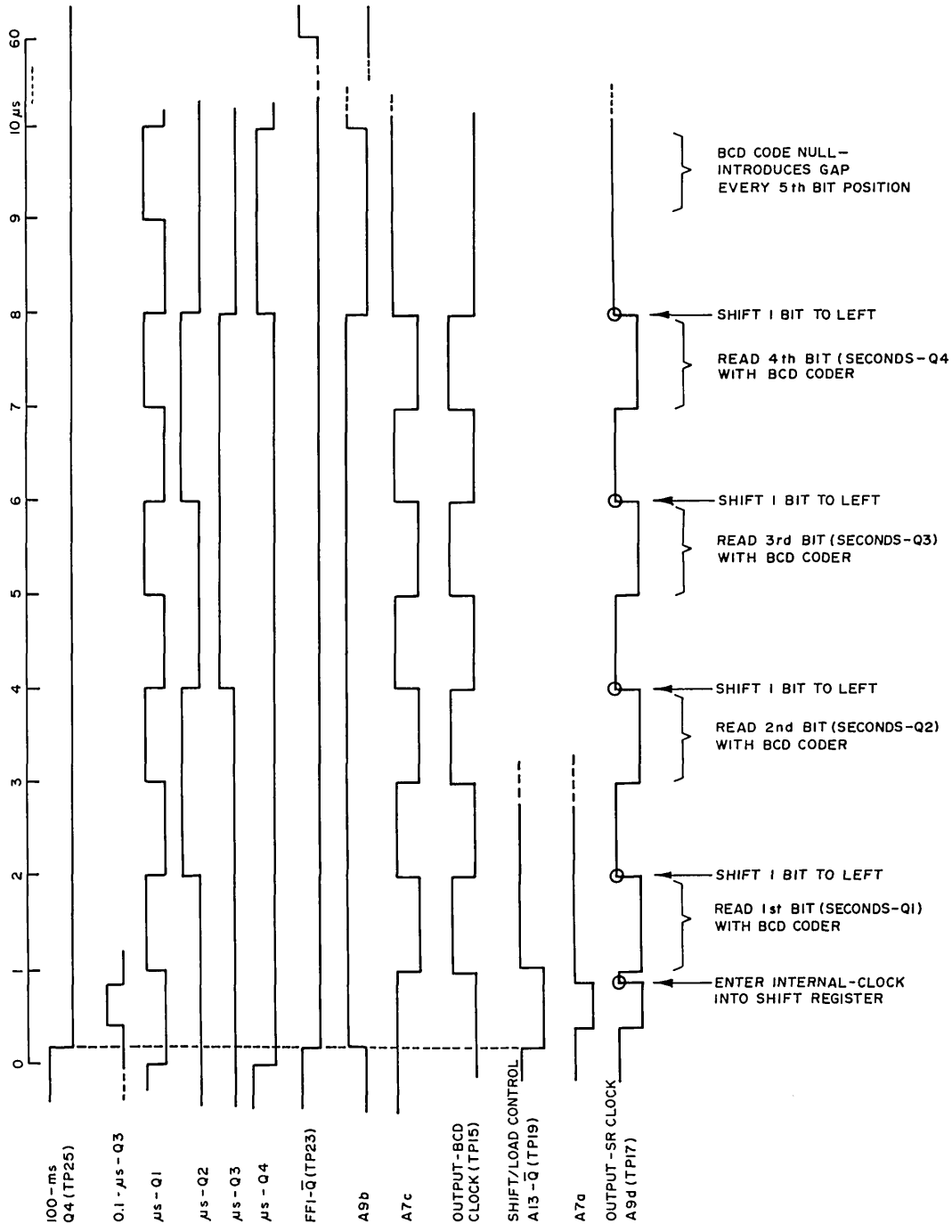

Fig. 11—Timing for operating the output shift register and output BCD coder

shift/load control is low) but to shift the time-word one bit to the left for each subsequent positive-going leading edge of the output-SR clock (when the shift/load control is high).

Generation of subsequent Output-SR and Output-BCD Clock pulses proceed in like manner until the μs-decade and 10-μs-decade counters reach a cumulative count of decimal 60, at which time the 8-bit, parallel-comparator, A = B output goes high, resetting FF 1-$\overline{Q}$ high. Consequently, the NOR A9b output switches low, blocking passage by NAND A7a of any subsequent 1-μs gates from the μs decade Q1 and preventing any further Output-BCD and Output-SR Clock pulses.

PRESET MULTIPLEXER AND OUTPUT BUFFERS

The serial-time decoder is equipped to operate either in synchronism with an external time source or independently as a self-contained electronic clock. Consequently, a preset multiplexer board X05 provides a capability for front-panel selection of the mode of counter preset, either by the serial-to-parallel converter board X02 or by time-selector switches mounted on the front panel.

Figure 12 shows a logic diagram of the complete preset multiplexer board X05. Provisions only for 13 bits have been made in the multiplexer, since in most applications it is only necessary to preset time to the nearest minute (that is, at the instant the external source reaches a preestablished 01 seconds). The remaining three bits (ten-minutes decade Q4 and ten-hours decade Q3 and Q4) are always reset to zero.

Each bit multiplexer uses the mode-control signal M and its complement $\overline{M}$ by means of three NAND gates to select which of the two input channels A or B to pass to the bit output C in a manner obeying the following logic equation:

$$C = (\overline{M} * A) + (M * B) .$$

When the mode control is grounded (external position of the sync switch), M goes low, forcing the channel-B NAND output high, thereby allowing the output NAND to pass (and invert) the signal from the output of the Channel-A NAND. But grounding of the mode control makes $\overline{M}$ high, thereby passing (and inverting) the channel-A signal of each bit to the output NAND. Consequently, the channel-A signal passes uninverted to the bit output. Conversely, when the mode control lead is ungrounded, M is high and $\overline{M}$ is low, reversing the conditions of the two input NANDs and thereby passing the channel-B signal uninverted to the bit output.

Figure 13 comprises schematic diagrams of the output buffer amplifiers used for the parallel-time-word outputs and for the serial-time-word outputs. Both circuits provide uninverted outputs, but whereas the parallel-time word is relatively low frequency in character (a given word remains for essentially one second without change), the serial-time word is relatively rapid (the narrowest pulse being 0.2 μs wide). Also, whereas the parallel-time word is fed directly to TTL logic in remotely located equipment, the serial-time word must feed a 90-Ω matched coaxial cable to provide minimum distortion for subsequent PDM demodulation by remote equipment.

Figure 13a is a schematic diagram of a typical buffer amplifier for the parallel-time word. In the serial-time decoder unit, the parallel-time word consists of 24 bits representing six 4-bit BCD digits (an additional ten-milliseconds Q4 gate is provided externally for

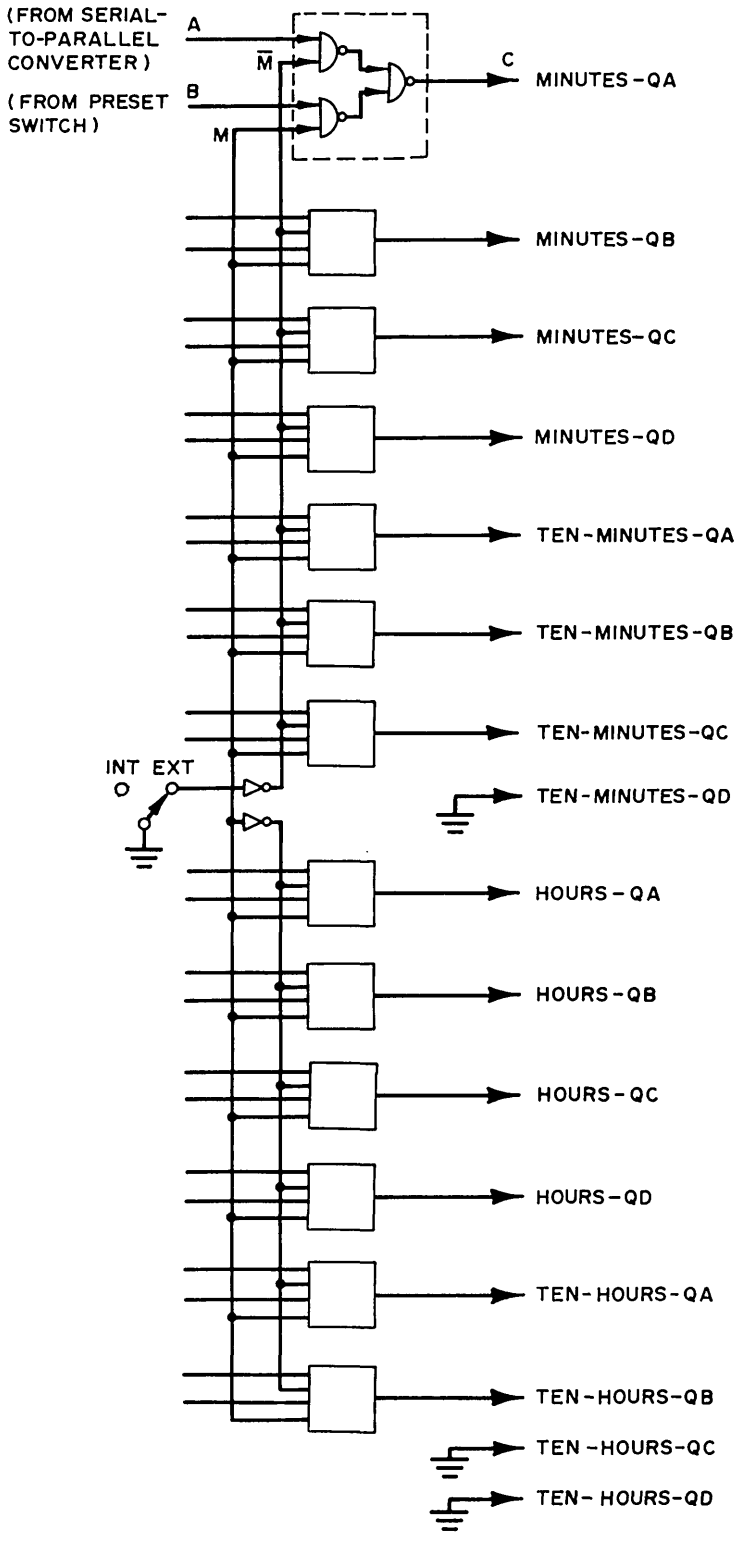

Fig. 12—Preset multiplexer

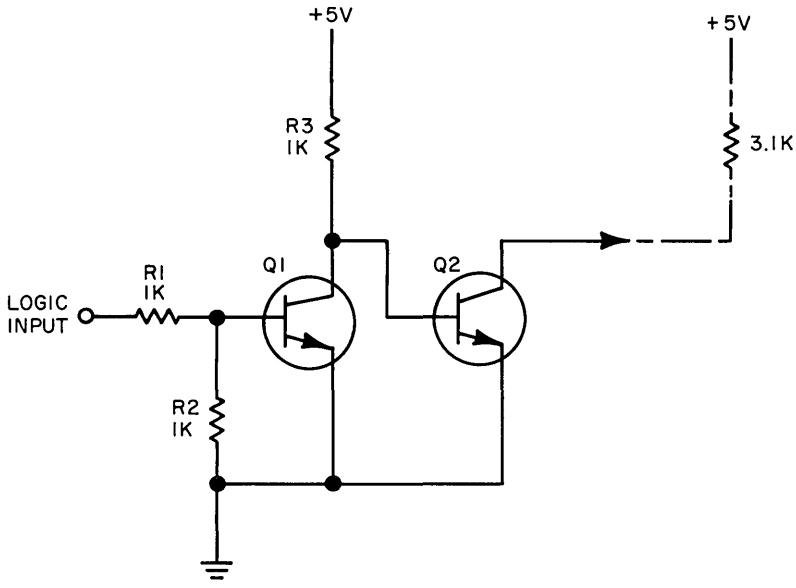

Fig. 13a—Parallel-output buffer amplifier

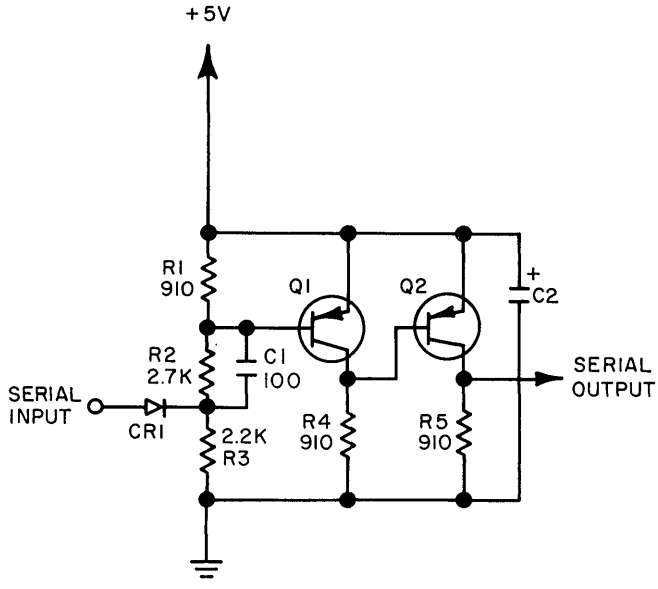

Fig. 13b—Serial-output buffer and amplifier

timing of a blinking-light time display for use with 35-mm oscilloscope cameras). However, only 21 buffer amplifiers are required, since four bits of the 24-bit, parallel-time word are always a binary-0 state. One should recall that the output of each decade-counter stage delivers TTL logic levels, so that a binary 0 is represented by a signal of 0 to +0.5 V, whereas a binary 1 is represented by a signal of +2.5 to +5.0V. The input signal to the buffer amplifier shown in Fig. 13a must exceed a +1.5-V threshold for the output of input resistance divider R1 and R2 to exceed the approximately +0.7-V forward base-emitter voltage required for the transistor to commence conduction. Due to the high current gain and low collector saturation voltage of transistor Q1, this stage quickly reaches

saturation with further increase of the input signal level, at which point the base-emitter voltage of output transistor Q2 drops below the conduction threshold, causing Q2 to cut off. No collector supply return resistance is provided within the time decoder unit for transistor Q2, since the TTL logic element located in the remote unit delivers approximately 1.6 mA (conventional) current into any load approximating a short circuit to ground (representing a binary-0 state).

Figure 13b is the schematic diagram of the serial-output buffer amplifier. Resistance divider R1, R2, and R3 delivers a bias voltage at the base of transistor Q1 just sufficient to drive transistor Q1 slightly into saturation. The low saturation voltage for this type of transistor ensures that under these (no-signal) conditions, the base-emitter voltage of transistor Q2 will be below the conduction threshold, allowing resistor R5 to pull the output lead to ground potential. When a fast-rise-time pulse is applied to the anode of diode CR1, this signal is transferred to the base of transistor Q1 partly through the voltage-divider action of resistors R1, R2, and R3, and partly through the input coupling time constant of R2 and C, rapidly driving the base of transistor Q1 into cutoff and thereby allowing the collector of Q1 to drop toward ground potential sufficiently to drive the base of transistor Q2 rapidly into conduction. Experience with this type of driver indicates that, for the values shown for the divider resistors, conduction commences at an input level of +2.7 V and that output saturation is reached at an input level of approximately +2.8 V. The B-supply lead must be heavily bypassed by capacitor C2, having an excellent high-frequency response, or oscillation in excess of 10 MHz will occur in the output. This circuit readily drives a 90-Ω coaxial line terminated in 90 Ω with only a few tenths of a volt drop in output amplitude. However, the relatively large value of the output dc-return resistance makes the circuit unsuitable for sinking moderate logic currents from other TTL or DTL logic circuits to which it might be coupled.

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13. ABSTRACT

The tape playback and serial-time decoder described in this report has been developed for evaluating event data recorded on magnetic tape during flight tests of the Hartlobe/Diversity dual-antenna system for airborne IFF transponders. Means are provided to recover pulse-duration-modulated (PDM)-multiplexed data from five playback channels of the instrumentation tape recorder to provide ten data channels for 35-mm oscillographic film records. Also, a serial-time code from another playback channel is used to synchronize an internal clock to provide the capability to superimpose on the oscillographic film record the time of day that the flight test data were originally recorded. Though the internal clock is primarily intended for use with the magnetic tape playback, a means is also available for operation as a completely self-contained, crystal-controlled, electronic clock with serial and parallel output signals.

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