

NRL Report 7139

A Polarization Diversity VHF Receiver

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Space Technology Branch
Electronic Warfare Division

December 14, 1970

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DOCUMENT CONTROL DATA - R & D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY (Corporate author) Naval Research Laboratory Washington, D. C. 20390		2a. REPORT SECURITY CLASSIFICATION Unclassified	
		2b. GROUP	
3. REPORT TITLE A POLARIZATION DIVERSITY VHF RECEIVER			
4. DESCRIPTIVE NOTES (Type of report and inclusive dates) A final report on one phase of the NRL Problem.			
5. AUTHOR(S) (First name, middle initial, last name) George E. Price and Mark Van de Walle			
6. REPORT DATE December 14, 1970		7a. TOTAL NO. OF PAGES 38	7b. NO. OF REFS 3
8a. CONTRACT OR GRANT NO. NRL Problem R06-29		9a. ORIGINATOR'S REPORT NUMBER(S) NRL Report 7139	
b. PROJECT NO. FN 2822-70-00300		9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report)	
c.			
d.			
10. DISTRIBUTION STATEMENT This document has been approved for public release and sale; its distribution is unlimited.			
11. SUPPLEMENTARY NOTES		12. SPONSORING MILITARY ACTIVITY Department of The Air Force Washington, D. C.	
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14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Receivers Radio receivers Superheterodyne receivers Very high frequencies Polarization (waves) Diversity reception Polarization diversity Frequency synthesizer Digital frequency synthesizer						

CONTENTS

Abstract	ii
Problem Status	ii
Authorization	ii
INTRODUCTION	1
DESIGN GOALS	1
GENERAL DESCRIPTION	4
DESIGN OF THE VHF RECEIVING PORTION	5
Theory	5
System Constraints	5
Required Gain	6
Circuit Design	8
DESIGN OF THE FREQUENCY SYNTHESIZER	12
RF Circuitry	12
Digital Part of Frequency Synthesizer	16
DESIGN OF THE COMPARATOR CIRCUITRY	31
ACKNOWLEDGMENTS	31
BIBLIOGRAPHY	33

ABSTRACT

One of the most important aspects in designing a VHF receiver is the system constraints that are imposed by the environment that the receiver must operate in. A systematic technique for designing a receiver as an integral part of an overall system has been developed. This technique allows straightforward receiver design considering all the pertinent system constraints. The major design considerations are: (a) all pertinent existing system constraints, (b) optimization of the received S/N for given intermodulation, dynamic range, and bandwidth, (c) ease of operation, and (d) ease of maintenance. A resulting polarization-diversity VHF receiver for a specific application was built using this technique.

PROBLEM STATUS

This is a final report on one phase of the NRL Problem; work on other phases is continuing.

AUTHORIZATION

NRL Problem R06-29
Project FN 2822-70-00300

Manuscript submitted June 16, 1970.

A POLARIZATION DIVERSITY VHF RECEIVER

INTRODUCTION

The VHF receiver to be described was designed to operate with a special-purpose receiving system. A simplified block diagram of this system is shown in Fig. 1. The antenna is two orthogonally polarized yagi arrays with horizontal and vertical elements. Two matched preamplifiers are remotely located on an antenna tower to overcome line loss and determine the system noise figure (NF). The signal environment is such that the optimum receiving polarization is constantly changing. The incoming signal is amplitude-modulated with sine-wave-type information at rates varying from 4 kHz to 20 kHz.

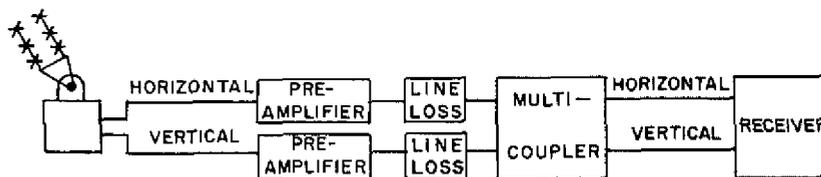


Fig. 1 - Simplified diagram of the system with which the receiver was designed to operate

DESIGN GOALS

The three main design goals considered are (a) optimization of the received signal-to-noise ratio (S/N) for given intermodulation, dynamic range, and bandwidth, (b) ease of operation, and (c) ease of maintenance.

There are only a limited number of ways to optimize the received S/N. The transmitted signal level and bandwidth are fixed and cannot be improved upon by the receiver. However, by minimizing the noise added by the receiving process and optimizing the received signal the received S/N can be maximized. The S/N is maximized in this receiver by (a) minimizing the noise figure of the receiver by using a low-noise RF amplifier in the front end, (b) providing proper gains through the system, (c) prefiltering the incoming RF signal to minimize intermodulation, crossmodulation, and spurious-impulse signal response, (d) using polarization diversity to insure the maximum available S/N while still retaining operational reliability, (e) using optimum bandwidths which have sharp-rolloff characteristics, (f) using a proper IF frequency, and well designed circuitry which will keep interfering signals to a minimum, and (g) providing a stable local oscillator.

This receiver must perform with minimum operator adjustment and monitoring 24 hours a day. Hence any operator adjustments which can be eliminated add to the overall system efficiency. Experience has shown that operators have varying degrees of training and motivation, which means that system efficiency increases toward a constant when the human operator interface is decreased. Therefore this receiver uses automatic

polarization diversity, automatic gain control, well lighted and labeled front-panel switches, and digital tuning of the receiver.

When designing equipment for use in an operational environment, special emphasis must be placed on reliability and ease of maintenance. Generally reliability is more important than performance in an operational environment. Equipment should be designed so that a failure can be isolated and remedied quickly. Hence this receiver is completely solid state, has modular construction with easily accessible modules for fast replacement, has troubleshooting aids designed into it, has fault detection circuitry with warning lights on the front panel for easy problem recognition, and has conventional field-tested circuits.

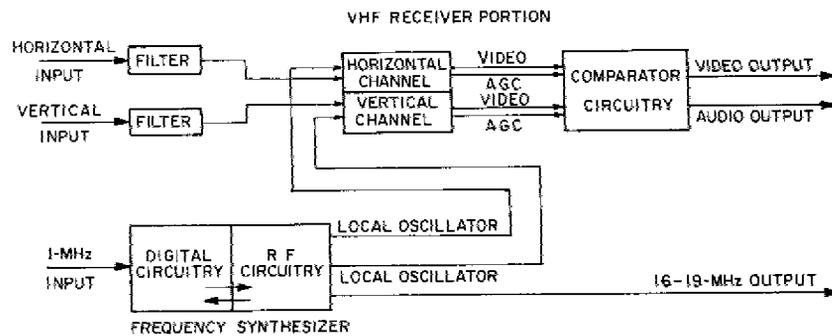


Fig. 2 - The polarization diversity VHF receiver

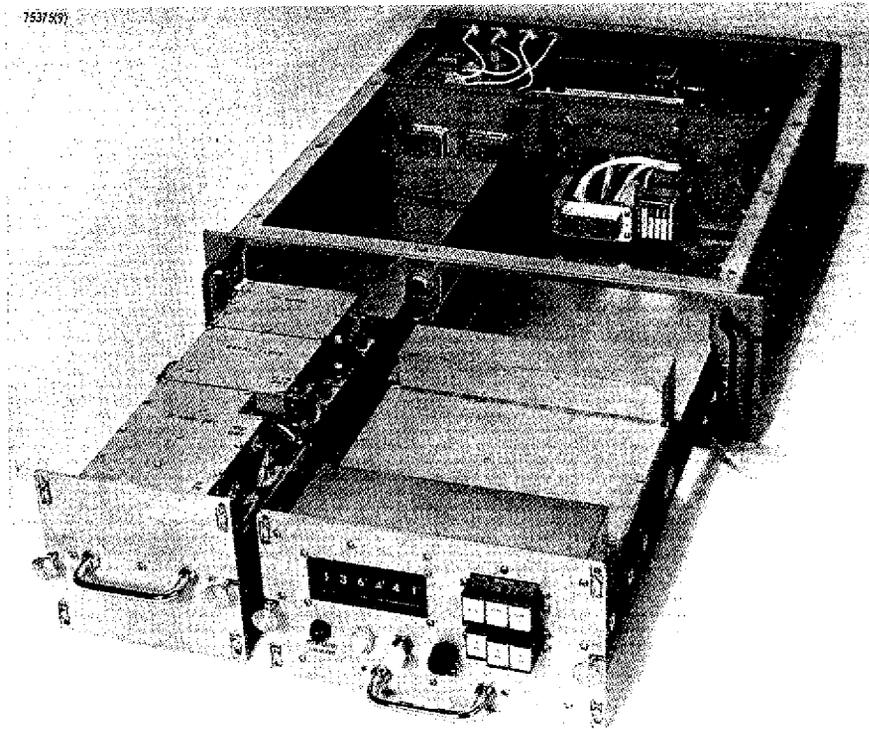


Fig. 3 - The receiver with the module drawers pulled out



Fig. 4 - Top view of the receiver

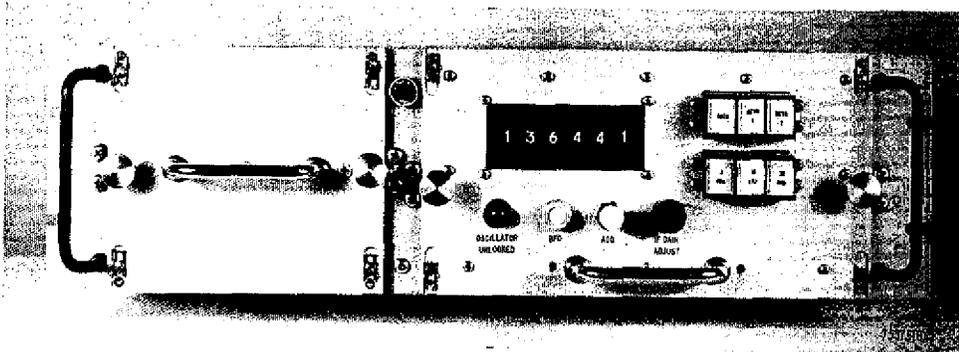


Fig. 5 - Front view of the receiver

GENERAL DESCRIPTION

This receiver is a digitally tunable, dual-channel, single-conversion superheterodyne that is connected to receive horizontal polarization on one channel and vertical polarization on the other for polarization diversity. The polarizations are combined by a sharp-selection diversity combiner; therefore the theoretical discussions will need cover only single-channel effects. A block diagram of the receiver is shown in Fig. 2. Figures 3, 4, and 5 show the completed receiver. This receiver is of modular construction, so that two of the three major parts are accessible without removing the receiver from the rack in which it is mounted. The three major portions of this receiver are: the VHF receiving portion (left-hand drawer), the digital frequency synthesizer (right-hand drawer) the comparator circuitry (at the left rear). Table 1 is a brief summary of the receiver characteristics. The design of each of the three major parts of this receiver will be discussed individually.

Table 1
Receiver Specifications

Item	Specification
Receiver type	Single-conversion superheterodyne
Frequency range	136.0 to 139.0 MHz
Receiver noise figure	6 dB maximum
Minimum saturable dynamic range	45 dB
Local-oscillator frequency	166 to 169 MHz
RF 3-dB bandwidth	5 MHz
Type of detector	Quadratic envelope detector
IF frequency	30 MHz
IF bandwidth	8, 16, or 32 kHz
IF shape factor	3:1 at 8 kHz and 2:1 at 16 and 32 kHz
Method of frequency control	Digitally tuned frequency synthesizer
Stability	3 parts per million
Number of channels	Two (vertical and horizontal polarization)
Spurious response	65 dB minimum
Image response	100 dB minimum
Method of Installation	Rack mountable
Operating temperature range	30 to 130°
Video bandwidth	10 kHz

DESIGN OF THE VHF RECEIVING PORTION

Theory

The thermal noise power can be found from

$$P_N = kTB_{eq}$$

where k is Boltzmann's constant, T is the noise temperature of the receiver, and B_{eq} is the equivalent bandwidth of the receiver. If $B_v < B_{IF}$, where B_v is the video bandwidth and B_{IF} is the IF bandwidth, then

$$B_{eq} \approx (2B_v B_{IF} - B_v^2)^{1/2} \quad (1)$$

The noise temperature T of a system can be related to the noise figure NF and the thermodynamic temperature of the system T_0 (taken by convention to be 290°K) by

$$T = (NF - 1) T_0$$

or

$$NF = 1 + \frac{T}{T_0}$$

For cascaded systems

$$T = T_1 + \frac{T_2}{G_1} + \frac{T_3}{G_1 G_2} + \dots + \frac{T_N}{G_1 G_2 \dots G_{N-1}}$$

and

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \dots + \frac{NF_N - 1}{G_1 G_2 \dots G_{N-1}}$$

where NF is the ratio of the signal-to-noise ratio of the source divided by the signal-to-noise ratio at the output:

$$NF = \frac{S_s/N_s}{S_o/N_o}$$

System Constraints

The system constraints which must be defined at this point are the following:

	<u>Maximum</u>	<u>Typical</u>	<u>Minimum</u>
Antenna noise temperature			290°K
Preamplifier power gain	25 dB	23 dB	21 dB
Preamplifier noise temperature	212°K	192°K	180°K
Line loss	6 dB	4 dB	3 dB
Multicoupler gain		6 dB	
Multicoupler noise temperature	435°K	290°K	290°K
Prefiltering loss		15 dB	
Estimated receiver noise temperature	865°K	435°K	290°K
IF bandwidth	32 kHz		8 kHz
Video bandwidth = B_v		10 kHz	
Detector sensitivity	-35 dBm		-40 dBm

Required Gain

The required gain can be calculated by first calculating the equivalent bandwidth B_{eq} , the system noise temperature T , and the noise figure NF. As stated previously,

$$B_{eq} = (2B_v B_{IF} - B_v^2)^{1/2} \quad (1)$$

Thus

$$\begin{aligned} B_{eq}(\min) &\approx (2 \times 10^4 \times 8 \times 10^3 - 10^8)^{1/2} \\ &\approx 0.78 \times 10^4 \\ &\approx 8 \text{ kHz} \end{aligned}$$

and

$$\begin{aligned} B_{eq}(\max) &\approx (2 \times 10^4 \times 32 \times 10^3 - 10^8)^{1/2} \\ &\approx 23 \text{ kHz} \end{aligned}$$

The minimum system noise temperature can be calculated using the minimum estimated receiver noise temperature and the other appropriate values previously given:

$$T = T_1 + \frac{T_2}{G_1} + \frac{T_3}{G_1 G_2} + \frac{T_4}{G_1 G_2 G_3}$$

where T_1 is the noise temperature of the preamplifier plus the noise temperature of the antenna ($180^\circ\text{K} + 290^\circ\text{K} = 470^\circ\text{K}$), G_1 is the maximum gain of the preamplifier (25 dB = 360), T_2 is the noise temperature of minimum line loss (290°K), G_2 is the minimum line loss (3 dB = 0.5), T_3 is the minimum noise temperature of the multicoupler (290°K), G_3 is the gain of the multicoupler (6 dB = 4), and T_4 is the estimated minimum receiver noise temperature (290°K), so that

$$\begin{aligned}
 T &= 470^\circ\text{K} + \frac{290^\circ\text{K}}{360} + \frac{290^\circ\text{K}}{(360)(0.5)} + \frac{290^\circ\text{K}}{(360)(0.5)(4)} \\
 &= 470^\circ\text{K} + 0.80^\circ + 1.60^\circ\text{K} + 0.40^\circ\text{K} \\
 &= 472.8^\circ\text{K}
 \end{aligned}$$

and

$$\text{NF} = 1 + \frac{T}{T_0} = 1 + \frac{472.8^\circ\text{K}}{290^\circ\text{K}} = 2.63 = 4.2 \text{ dB} .$$

Note that a receiver noise figure in the range of 3 to 6 dB will not have a significant effect on the system noise figure.

The tangential sensitivity T.S. by convention is a signal-to-noise ratio of

$$\text{S/N} = 8.5 \text{ dB} .$$

Since $\text{S/N} = 0$ when the signal power P_s equals the noise power P_n , or

$$P_s = P_n = kTB_{eq} ,$$

then

$$\text{T.S.} = kTB_{eq} + 8.5 \text{ dB} .$$

The minimum detectable signal in this system would occur when the system noise figure and bandwidth are a minimum. The power of this signal is calculated from

$$\text{T.S.} = kTB_{eq} + 8.5 \text{ dB} + \text{NF} ,$$

where $kTB = 174 \text{ dBm}$ for a 0-dB noise figure at 1 Hz, so that

$$kTB_{eq} = 133 \text{ dB}$$

for $B_{eq}(\text{min}) \approx 8 \text{ kHz}$, and where

$$\text{NF}(\text{min}) = 4.2 \text{ dB}$$

Hence the minimum detectable signal is

$$\text{T.S.} = -133 \text{ dB} + 8.5 \text{ dB} + 4.2 \text{ dB} = -120.3 \text{ dBm} .$$

The gain required to detect the calculated signal of power -120.3 dBm is equal to the detector sensitivity minus the tangential sensitivity. This is the maximum gain G_{max} required in the receiving system:

$$\begin{aligned}
 G_{\text{max}} &= \text{maximum detector sensitivity} - \text{T.S.} \\
 &= -35 \text{ dB} - (-120.3) \text{ dB} = 85.3 \text{ dB} .
 \end{aligned}$$

The receiving system must have this amount of gain or it will be gain limited. To determine how much of this gain is needed in the receiver, a worst-case system analysis is used:

Preamplifier gain	21 dB
Line loss	-6 dB
Multicoupler gain	6 dB
Prefiltering loss	-0.5 dB
Gain external to the receiver	<u>20.5 dB</u>

The gain needed in the receiver is then

$$G_{revr} = G_{max} - G_{ext} = 85.3 \text{ dB} - 20.5 \text{ dB} = 65 \text{ dB}$$

Circuit Design

A block diagram of the receiving portion of the receiver is shown in Fig. 6. Figure 7 shows a more detailed block diagram of one channel. Figure 8 shows one channel of the actual receiver. Figure 9 is the schematic diagram of this channel.

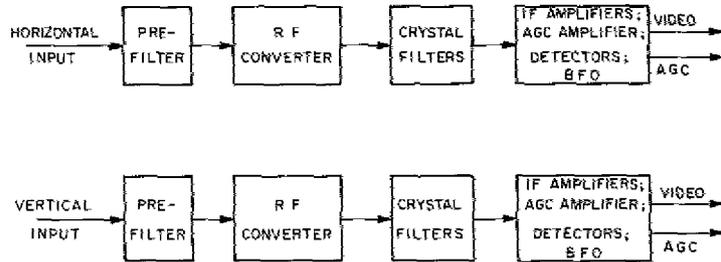


Fig. 6 - VHF receiving portion of the system

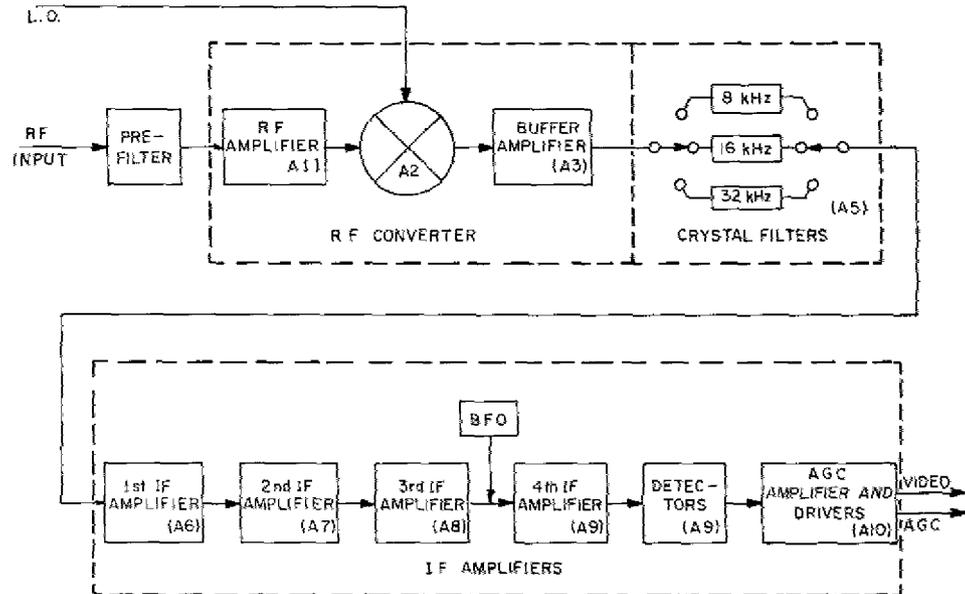


Fig. 7 - One channel of the VHF receiving portion

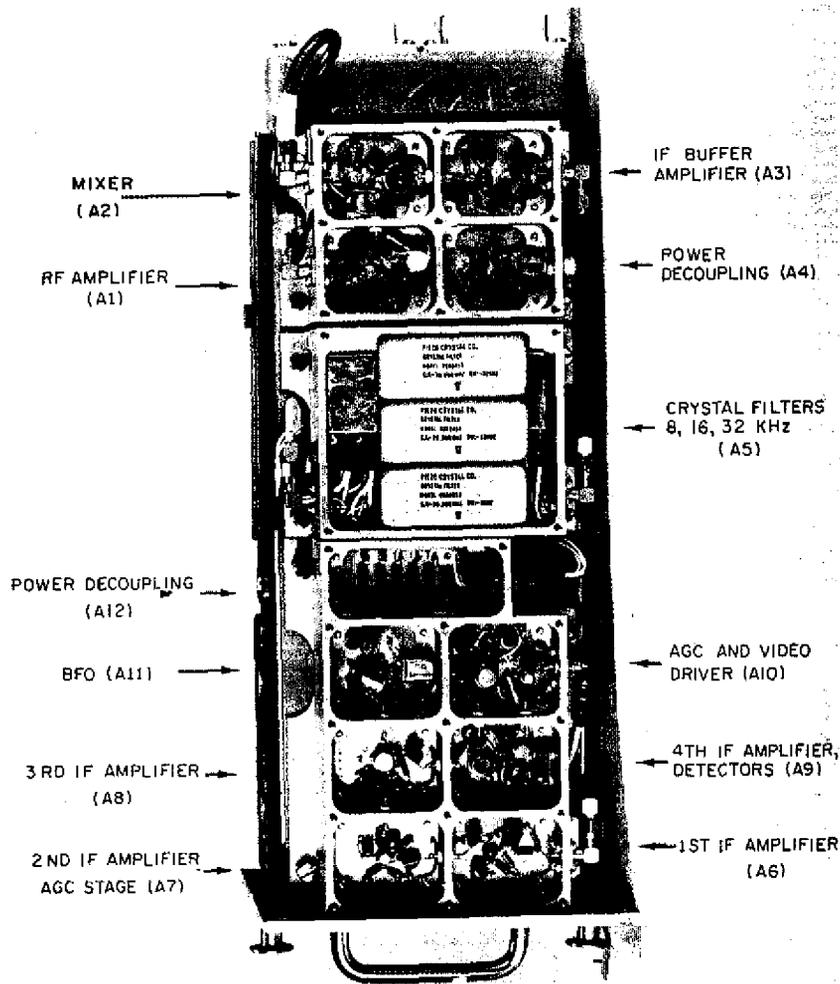


Fig. 8 - One channel of the VHF receiving portion

The receiver gain distribution is:

RF converter	30 dB
Crystal filters	-10 dB
IF amplifiers	45 dB
Total	<u>65 dB</u>

The RF gain is needed to establish a reasonable receiver NF, but too much RF gain causes unnecessary intermodulation distortion and cross products. If too much gain is built into the IF or RF section, stability and dynamic range becomes a problem. The crystal-filter loss is fixed.

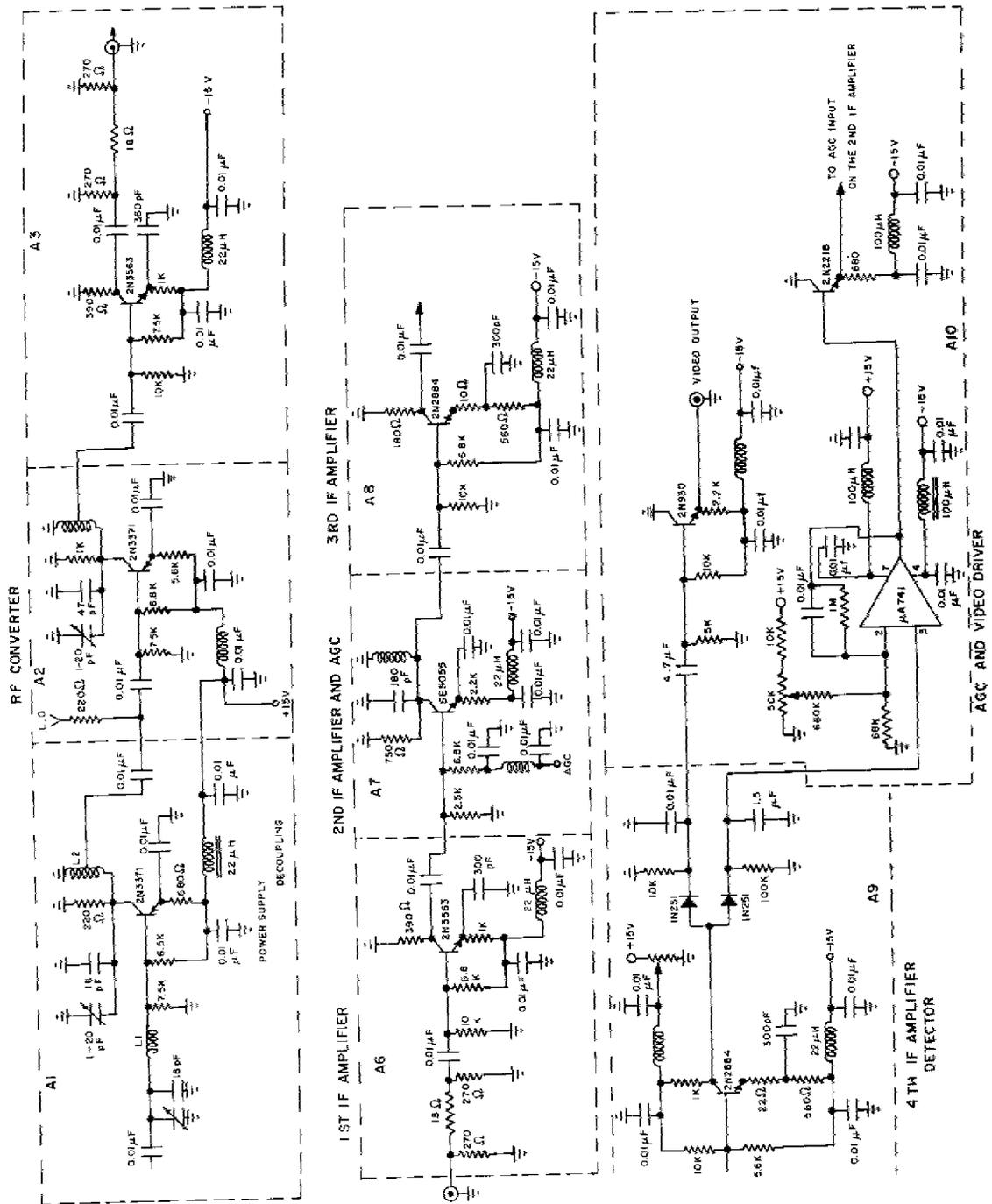


Fig. 9 - One channel of the VHF receiving portion

The prefiltering is accomplished by a four-pole, high-Q, iris-coupled filter. The loss in this filter directly adds to the noise figure of the receiver; however it prevents unwanted out-of-band signals from entering the receiver. If these signals were to enter the receiver, they and their intermodulation products would appear as noise and decrease the S/N of the wanted received signal.

Circuit A1 is the RF front-end amplifier. This solid-state unit provides sufficient RF gain to offset the mixer noise and the noise contributed by the remainder of the receiver. This RF amplifier employs a 2N3371 transistor as a common-emitter amplifier with a matching circuit on the input and a parallel tuned output. The transistor is biased to minimize intermodulation distortion, which is 78 dB down from the main signal. The input matching circuit transforms the input impedance of the RF amplifier to match the output impedance of the input filter. The inductor in the tuned output provides a similar matching into the mixer, circuit A2.

The active mixer, circuit A2, is also a common-emitter amplifier. The transistor is biased so as to take advantage of the nonlinear characteristic of the base emitter junction to provide mixing action. The local-oscillator and the RF signals are fed into the base of this transistor. A high-side conversion is performed, giving a 30-MHz IF frequency. The IF frequency appears at the parallel-tuned collector circuit. The inductor provides the impedance transformation for matching into the buffer amplifier.

Circuit A3 is the IF buffer amplifier, which also employs a common-emitter amplifier. This amplifier provides isolation between the mixer and crystal filters. The output of this circuit is taken off the resistive load that goes into a pi attenuator. This attenuator provides a nonreactive 50-ohm source to drive the crystal filters.

The different bandwidth filters are switched in and out of the circuit by using coaxial relays, which are packaged next to them. This switching is done via a switch on the front panel of the unit. There are three selectable bandwidths: 8, 16, and 32 kHz.

The input to the 1st IF amplifier, circuit A6, is through a pi-attenuator section which presents a 50-ohm impedance to the output of the crystal filters. The 1st IF amplifier is a common-emitter amplifier with a resistive load. Resistive loads are used in all the IF stages except the 2nd IF amplifier and AGC stage, circuit A7. There is no video gain in this unit, all amplification coming from RF and IF stages. This allows compact circuits, but presents stability problems. To insure absolute stability, low-impedance resistive loads were used instead of high-impedance tuned circuits which act as antennas.

The 2nd IF amplifier and agc stage, circuit A7, is forward acting through control of the emitter current. The emitter current is controlled by varying the voltage on the base of the transistor. The SE5055 transistor is used because of its linear gain-versus-emitter-current characteristic.

The 3rd and 4th IF amplifiers, circuits A8 and A9, are common-emitter amplifiers with resistive loads. 2N2884 transistors are used because of the power-handling capability and good power gains. The output of the 4th IF has dc-coupled to it the signal detector and the agc detector. The time constant of the agc circuit is controlled by the agc detector. The agc amplifier and driver is in circuit A10. The gain of the agc loop is controlled by the operational amplifier in this circuit. The emitter-follower stage supplies the necessary drive capability. The drive for the video output is also supplied by an emitter follower in A10.

The beat-frequency oscillator (BFO), circuit A11, is a crystal-controlled oscillator that oscillates at 30MHz, the IF frequency. The transistor has a parallel-tuned circuit in the collector. The positive feedback necessary to sustain oscillation is provided from

the collector through the small capacitor to the emitter. The output is taken from the collector tank circuit, with the inductor acting as the impedance transformer. The output of the BFO is injected into the base of the 4th IF stage.

DESIGN OF THE FREQUENCY SYNTHESIZER

The frequency synthesizer contains the necessary digital and analog circuitry for the accurate control and generation of the local oscillator for the VHF receiving portion of the receiver. This unit also contains the necessary circuitry to detect a malfunction in the oscillator control circuitry and light an indicator lamp on the front panel. The two main parts of this unit, the RF and digital circuitry, will be considered separately for simplicity, even though they are contained in a single modular unit of the receiver. Figure 10 is a block diagram of the frequency synthesizer. Figure 11 is a photograph of this section in the receiver.

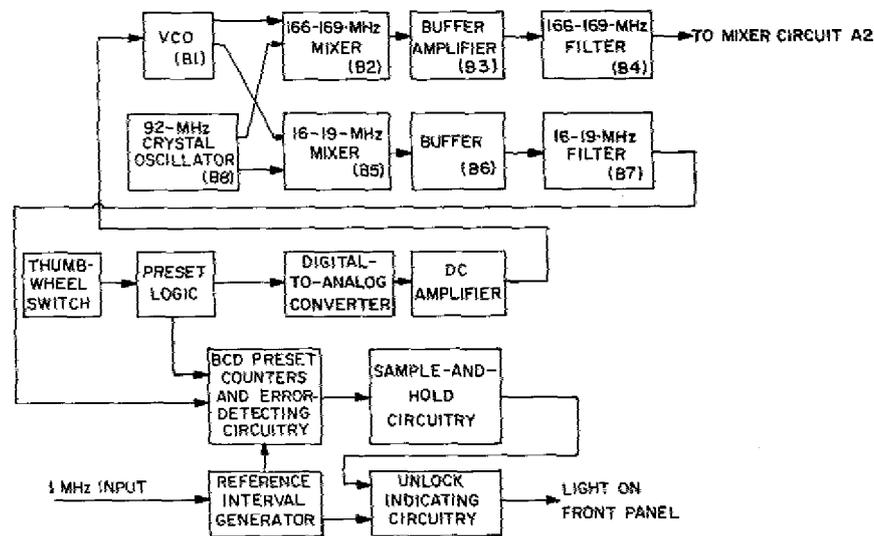


Fig. 10 - Frequency synthesizer

RF Circuitry

The RF circuitry that generates the local oscillator for the receiver is shown in Fig. 12, and a schematic diagram of this section is shown in Figure 13. This part of the receiver contains the voltage-controlled oscillator that the digital portion of the frequency synthesizer controls, a crystal-controlled conversion oscillator, two mixers, and associated drivers and filters.

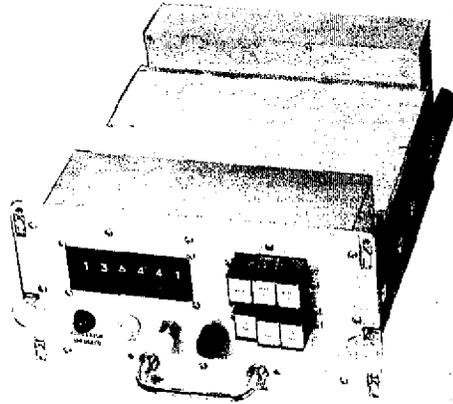
This circuitry supplies the 16-to-19-MHz signal to the digital portion of the synthesizer and a 166-to-169-MHz signal as the local oscillator to each channel of the VHF receiving part of the system. These signals are generated in the two mixers according to

$$f_{co} + f_{vco} = f_{lo} \quad (2)$$

and

$$f_{co} - f_{vco} = f_s \quad (3)$$

Fig. 11 - Frequency synthesizer



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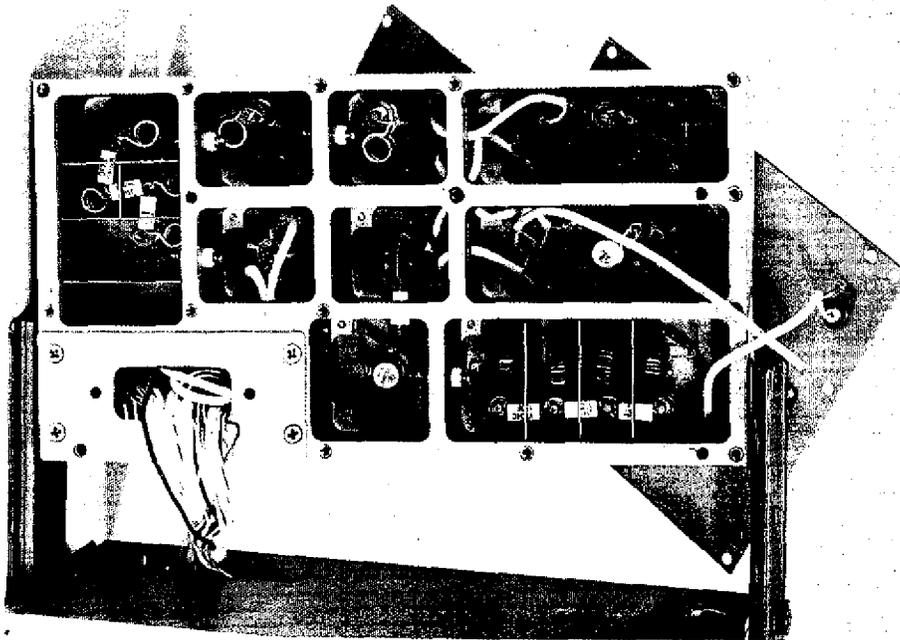


Fig. 12 - RF portion of the frequency synthesizer

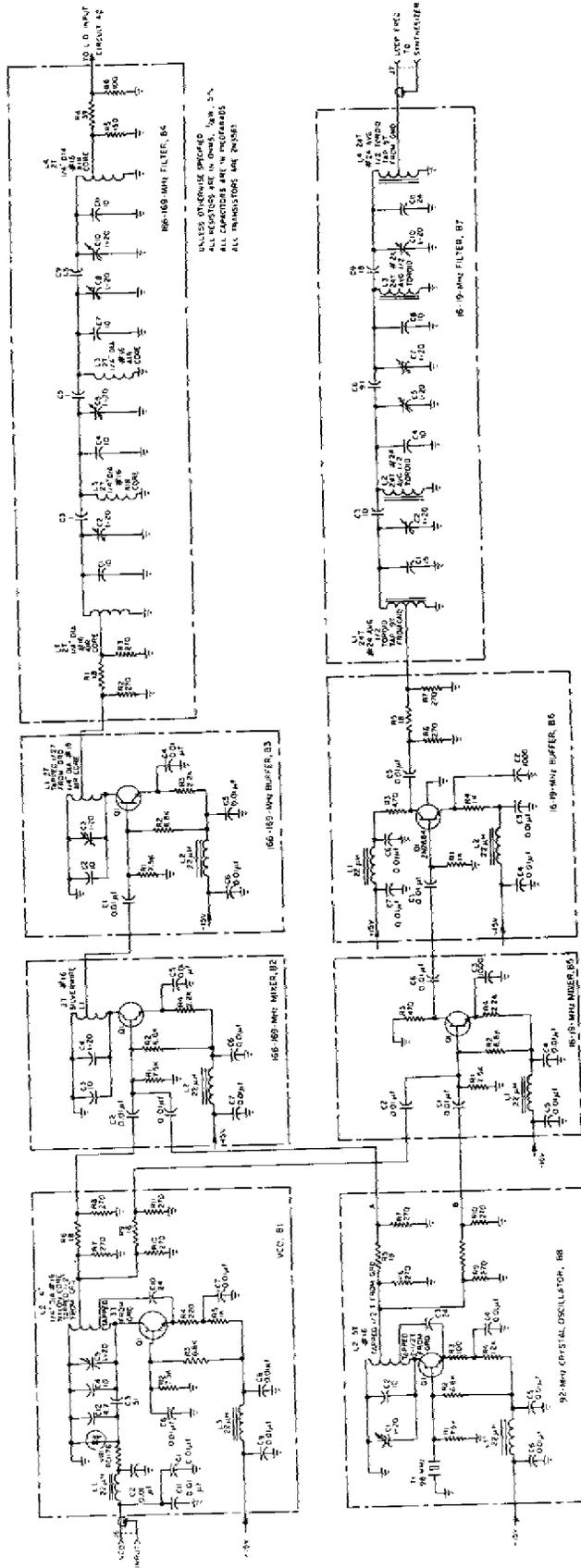


Fig. 13 - RF portion of the frequency synthesizer

where f_{co} (crystal oscillator) is 92.000 MHz, f_{vco} (voltage-controlled oscillator) is 74 to 77 MHz, f_{lo} (receiver local oscillator) is 166 to 169 MHz, f_s (frequency supplied to synthesizer) is 16 to 19 MHz.

As can be seen from Fig. 10 the two signals are generated by mixing the two oscillators and using both the sum frequency, Eq. (2), and the difference frequency, Eq. (3).

Circuit B1 in Fig. 13 is the voltage-controlled oscillator. The frequency of oscillation is determined by the tank circuit in the collector formed by L2, C3, C4, C5, and VR1. VR1 is a varactor or voltage-controlled capacitor. Thus when a dc voltage applied to VR1 and the capacitance in the tank circuit changes, the resonant frequency changes and the frequency of oscillation changes. This dc control voltage is derived in the digital-to-analog converter and is generated in such a way as to bring the VCO to the desired frequency. Two pi-attenuators are impedance-tapped on inductor C2 to provide a VCO output to the two mixers, circuits B2 and B5. It also provides some isolation between these two outputs.

Circuit B8 in Fig. 13 is the 92,000-MHz crystal oscillator. This oscillator also employs a tuned collector, with positive feedback provided from this output tank circuit through capacitor C3 to the emitter. Two pi-attenuators are also impedance-tapped on inductor L2 of this circuit to provide the oscillator output to the two mixers, B2 and B5.

Circuit B2 in Fig. 13 is the sum frequency mixer. This active mixer, whose collector is a parallel resonant circuit tuned to the sum frequency of the crystal and voltage controlled oscillators, supplies the 166-to-169-MHz local oscillator through the buffer amplifier and bandpass filter to the receiver. The two oscillators provide the input to the base of the transistor. The nonlinear base-emitter characteristic produces the sum frequency at the collector of the mixer.

Circuit B5 operates in the same manner as B2, except that the collector circuit is a resistive load and the difference frequency appears there. This supplies the 16-to-19-MHz signal for the buffer amplifier and bandpass filter.

Circuit B6 is the 16-to-19-MHz buffer amplifier. This is an RC-coupled amplifier used to amplify the 16-to-19-MHz signal to a level that is sufficient for the digital circuitry to operate. This circuit is a basic RC-coupled amplifier with some frequency-response shaping done with the emitter-bypass capacitor C1. The output of the buffer amplifier drives a bandpass filter, circuit B7.

The 16-to-19-MHz bandpass filter, circuit B7, is a four-section linear phase Butterworth filter. This filter is used to filter the unwanted harmonics from the 16-to-19-MHz signal generated in the mixers. This provides a low-distortion signal for the digital circuitry to operate on.

Circuit B3 is the 166-to-169-MHz buffer amplifier. This is a common-emitter amplifier. This is a common-emitter amplifier with a parallel resonant tuned collector. This amplifier provides isolation between the mixer circuitry and the bandpass filter, circuit B4. Inductor L1 in the collector circuit forms a transformer, so that an impedance match is achieved between the amplifier output and the filter input.

Circuit B4, the 166-to-169-MHz bandpass filter, is a four-section linear phase Butterworth filter. This circuit is used to filter all the unwanted harmonics generated in the mixing process and feed a low-distortion signal to the local oscillator. The pi-attenuators at the input and output of the filter provide impedance matching, and they also serve to reduce the local-oscillator signal level to a point where optimum mixing action occurs. The output of this filter is split and drives the mixer circuits in both channels of the receiver portion.

Digital Part of the Frequency Synthesizer

General Block Diagram — Figure 10 shows a block diagram of the frequency synthesizer. Figures 14 and 15 show the digital section. This circuitry basically involves a set of thumbwheel switches, preset logic, a five-stage BCD preset counter, a reference interval generator, error-detecting circuitry, sample-and-hold circuitry, and a dc amplifier.

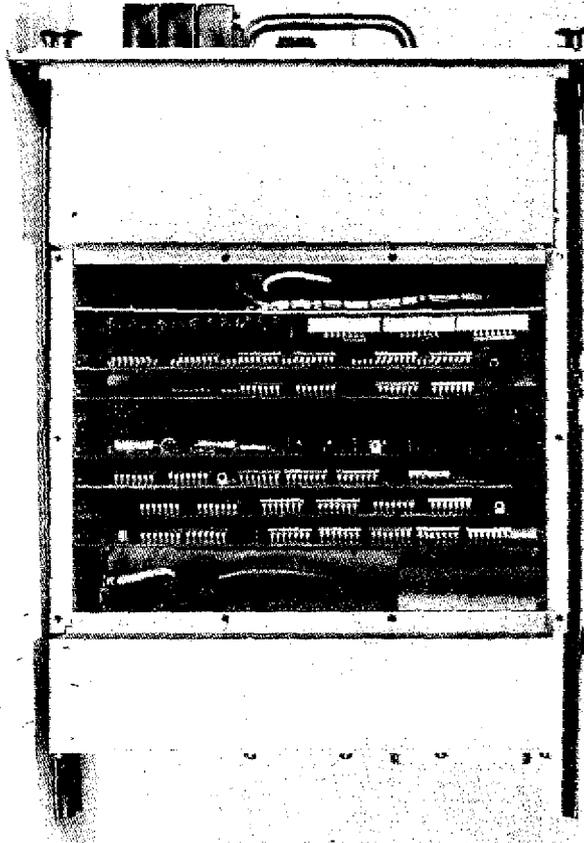


Fig. 14 - Card locations in the digital portion of the frequency synthesizer

The reference interval generator consists of a series of counters which count down the 1-MHz clock signal. This interval generated is basically as stable as the 1-MHz clock signal.

The five-stage BCD counter is preset from the thumbwheel switches through the preset logic shown in Figs. 16 and 17. The counter is preset in such a way that if the voltage-controlled oscillator (VCO) were oscillating at the frequency necessary to tune the receiver to the setting of the thumbwheel switches, the BCD preset counter would reach a count of 99999 in exactly one interval of time as generated in the reference interval generator.

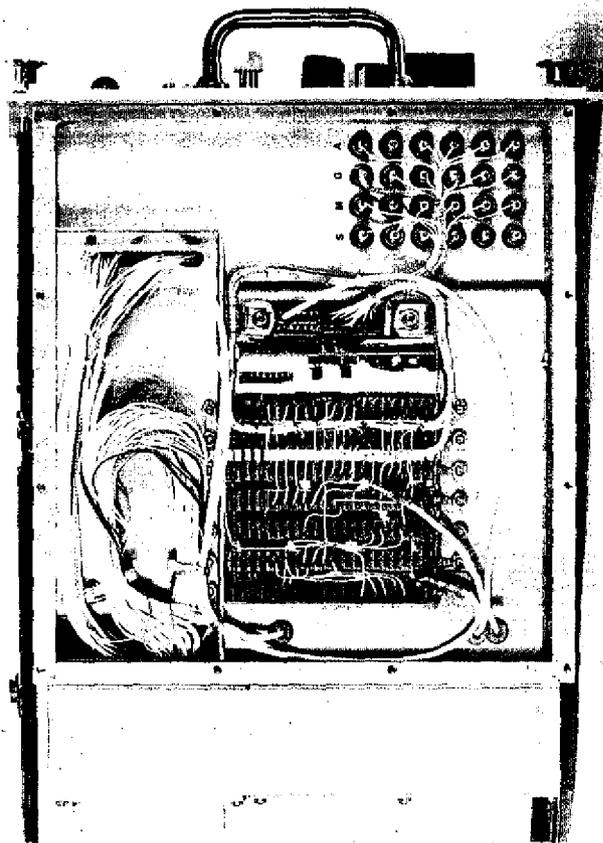


Fig. 15 - Back-plane wiring in the digital part of the frequency synthesizer

If the frequency of the VCO were too high, the five-stage BCD counter would fill up (reach 99999) before the end of the reference interval. The error-detecting circuitry would detect this error, generate a correction voltage in the sample-and-hold circuitry, and through the dc amplifier send this voltage to the VCO in such a way that the VCO would become tuned to the desired frequency. This process would be repeated at the reference interval rate until the VCO became stabilized at the desired frequency. A similar sequence of events would occur if the frequency of the VCO were too low; the difference is that the counter would not be filled up in one reference interval; one error detecting circuit would sense this and create a correction voltage in the direction to bring the VCO to the proper frequency.

Detailed Operation - The four thumbwheel switches, which are located on the front panel as the right-hand four digits, are BCD switches.

The output of the thumbwheel is fed into the unit, through buffering inverters, to the preset logic. The output of the preset logic is used to preset the five-stage BCD counter in such a way that if the correct frequency f_s were applied to the synthesizer, the five-stage BCD counter would reach the 99999 stage in one reference interval. The counter reads one cycle or one zero of the input crossing-signal frequency as one count; the number of counts the BCD counter reads in one reference interval is then

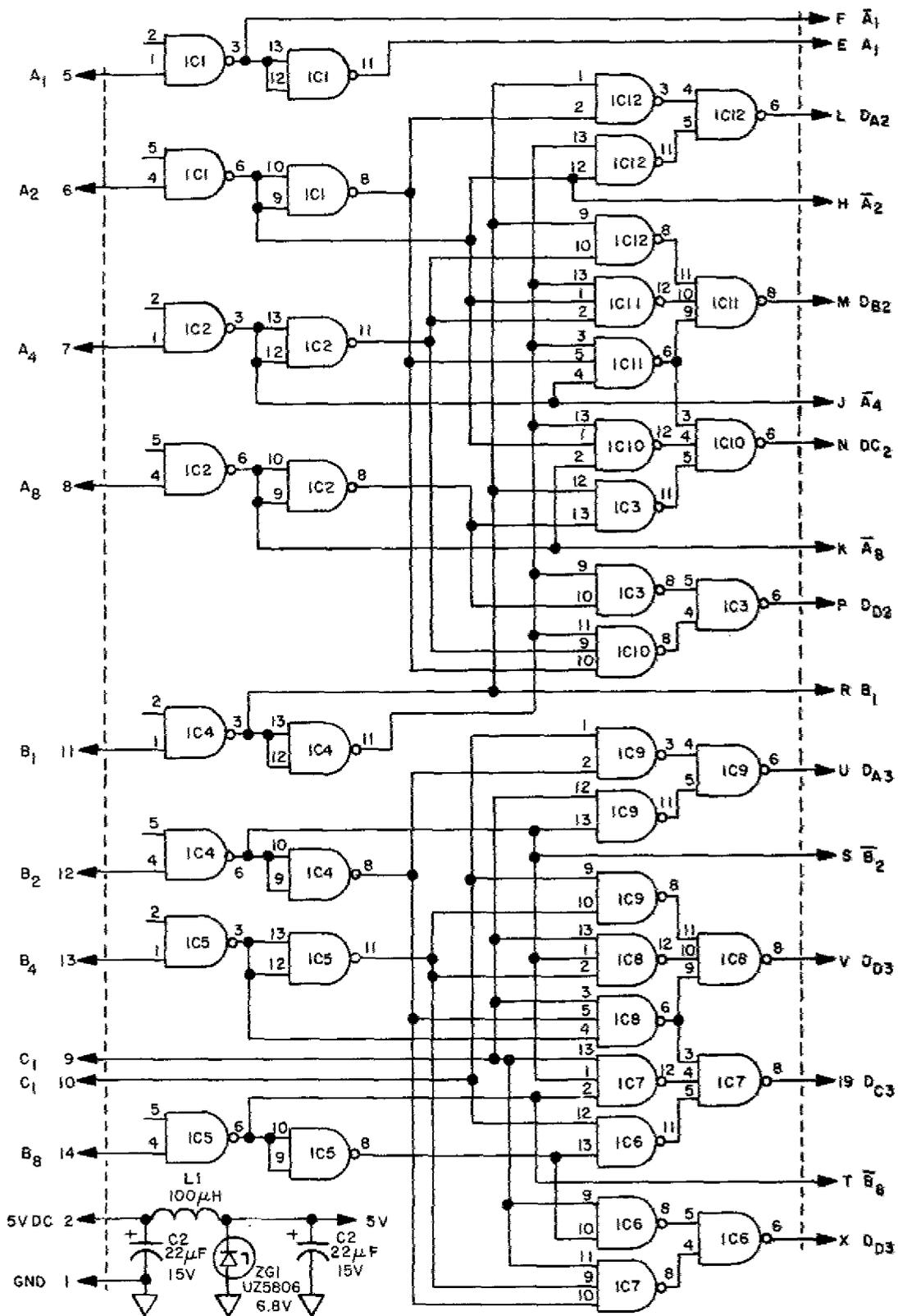


Fig. 16 - Preset logic board A

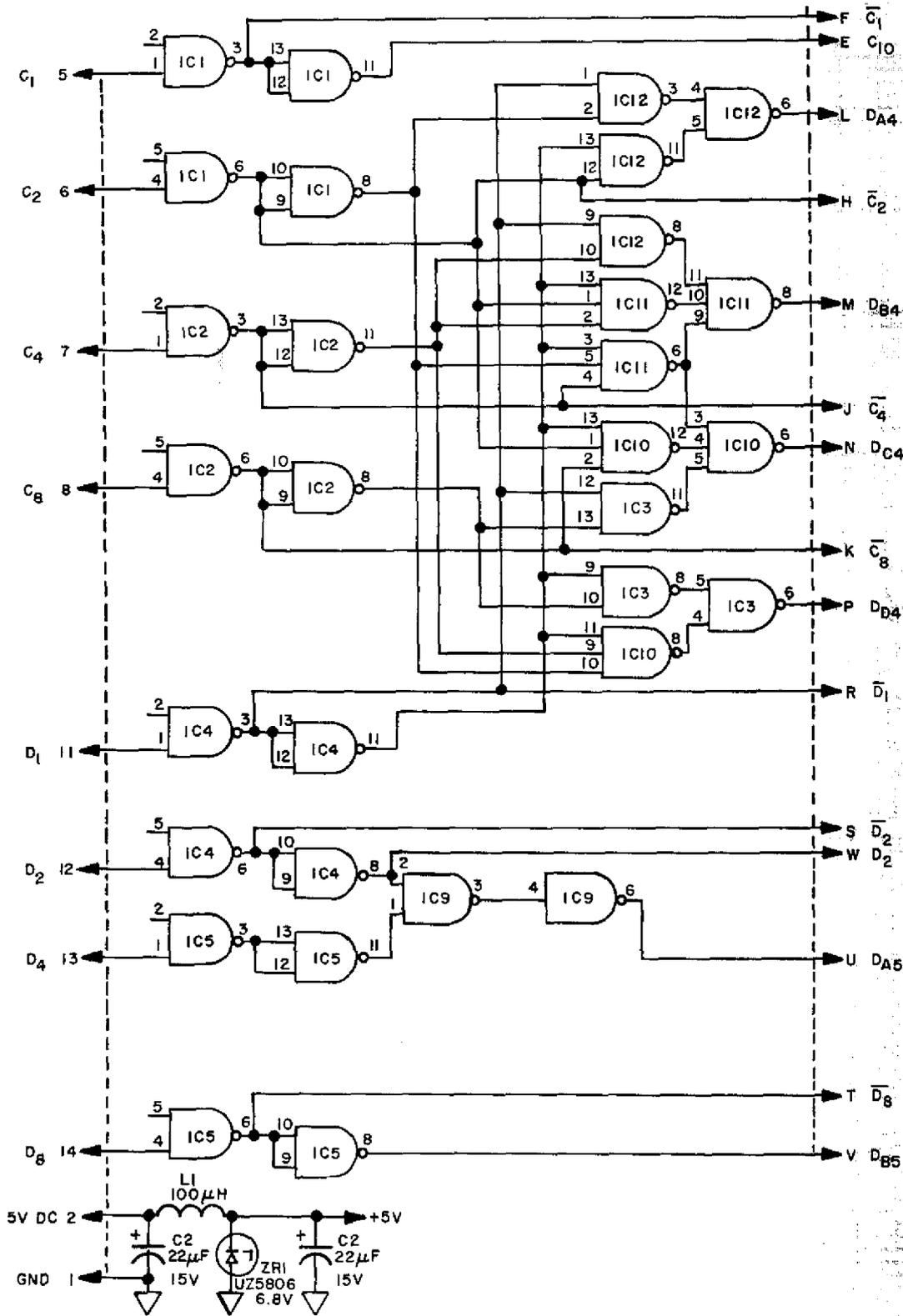


Fig. 17 - Preset logic board B

Since the circuitry actually detects when the BCD counter reaches 99999, the counter is preset to the compliment of the number. The one-count ambiguity is made up in gating-circuit delays.

Using the following information, an expression can be derived relating the actual RF frequency on the thumbwheel switches to the decimal number the five-stage BCD counter is preset to:

$$\text{counts} - f_s \times (\text{reference interval}).$$

Since the circuitry actually detects when the BCD counter reaches 99999, the counter is preset to the compliment of the number. The one-count ambiguity is made up in gating-circuit delays.

Using the following information, an expression can be derived relating the actual RF frequency on the thumbwheel switches to the decimal number the five-stage BCD counter is preset to:

$$f_{RF} = 136.000 \text{ to } 139.000 \text{ MHz} - \text{RF receiver range},$$

$$f_{vco} = 79.000 \text{ to } 82.999 \text{ MHz} - \text{voltage-controlled oscillator},$$

$$f_{co} = 92.000 \text{ MHz} - \text{crystal oscillator},$$

$$f_{lo} = 166.000 \text{ to } 169.000 \text{ MHz} - \text{receiver local oscillator},$$

$$f_{IF} = 30.000 \text{ MHz} - \text{receiver IF frequency}$$

$$f_s = 16.001 \text{ to } 19.000 \text{ MHz} - \text{synthesizer frequency},$$

$$\text{Reference interval} = 5 \times 10^{-3} \text{ sec.}$$

The following equations relate the various frequencies in the receiver to each other:

$$f_{RF} = f_{lo} - f_{IF}$$

$$f_{lo} = f_{co} = f_{vco}$$

$$f_s = f_{co} - f_{vco}$$

The following relationship can be derived from the above:

$$\text{Preset number} = (f_{RF} \times 5 \times 10^{-3}) - 7.3 \times 10^5.$$

Figure 18 shows the five-stage BCD counter, the all-9's gating, and the shaping Schmitt trigger. Transistors Q_1 and Q_2 form the Schmitt trigger that drives the counter.

IC1 through IC5 form the five-stage BCD preset counter. The counter is preset to the BCD number appearing on pins 3, 4, 10, and 11 of each decade. These BCD numbers are strobed into the five-stage counter with signal PS (preset strobe) generated in the reference interval generator. The counter is disabled during the preset time by gate IC9. Each IC is a divide-by-10 counter.

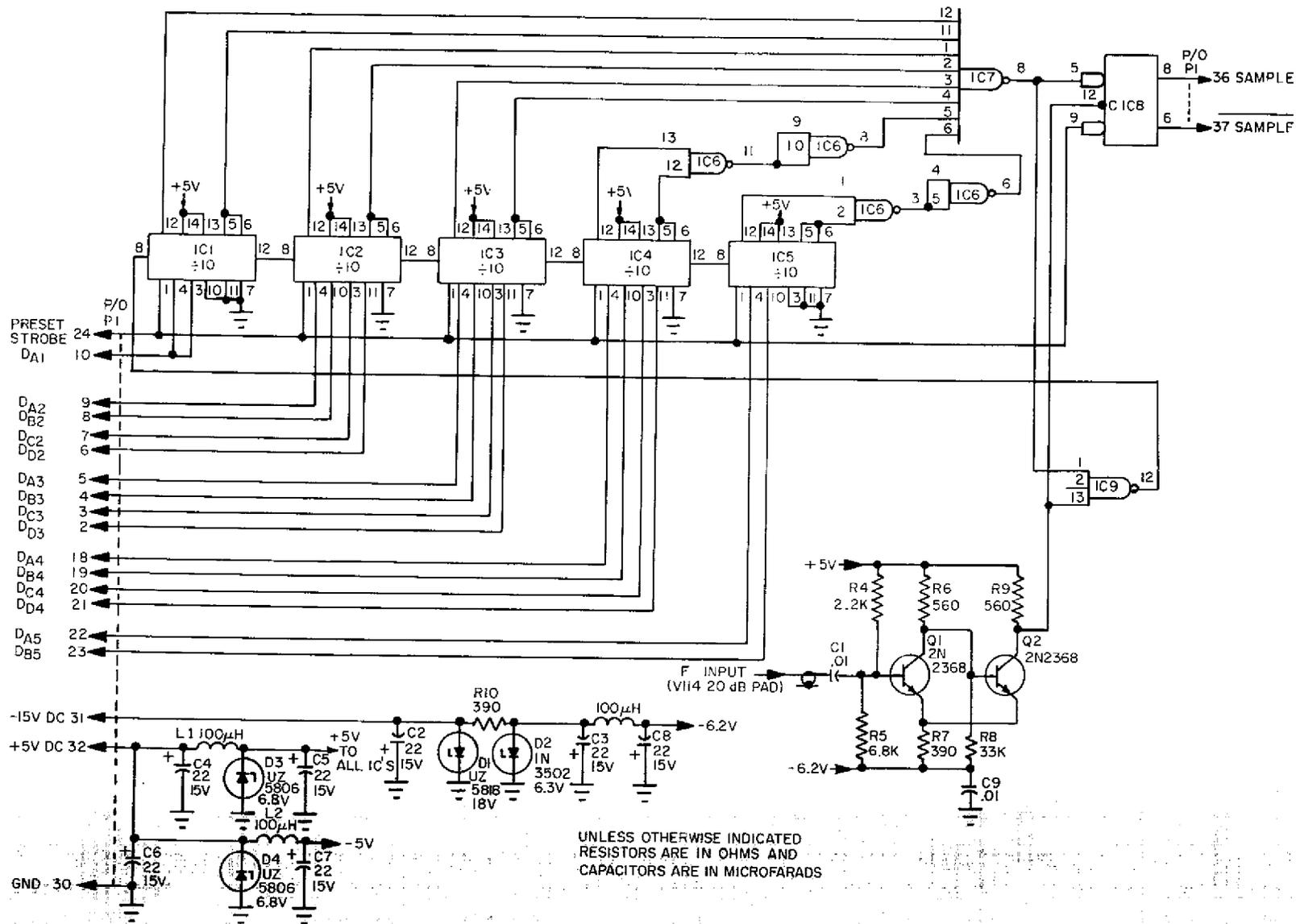


Fig. 18 - Five-stage BCD counter, all-9's gating, and shaping Schmitt trigger)

IC6, IC7, and IC8 form the gating that detects the all-9's condition in the five-stage counter. IC8 is a JK flip-flop used to generate signals $\overline{\text{SAMPLE}}$ and $\overline{\text{SAMPLE}}$. These signals are used in the sample-and-hold circuitry to generate the error or correction voltage signal. This flip-flop is normally reset; but when the all-9's condition is detected, the flip-flop is set-enabled and is then set on the next clock pulse from the Schmitt trigger. The flip-flop is then reset enabled by the signal-preset strobe and reset on the next clock pulse. The preset-strobe signal is generated in the reference interval circuit.

Figure 19 shows the circuitry that generates the reference interval and the preset-strobe signal. This circuitry is basically two divide-by-10 counters, followed by synchronous divide-by-5 and divide-by-11 counters.

The reference interval is thus generated by counting down the stable, external 1-MHz clock signal to the reference interval, which is a signal that has a 5.5 msec period and a 500- μ sec pulse width. This gives the reference interval a time of 5.0 msec.

As seen from Fig. 19 the 1-MHz shaping network is made up by Q_1 and Q_2 . The network transforms the sine-wave input into a square-wave signal, suitable for operation of the logic circuitry. This network requires a minimum signal level of 3 volts peak to peak into 50 ohms to operate properly. IC3 and IC4 are nonsynchronous divide-by-10 counters. These circuits divide the 1-MHz signal to 100 kHz and then to 10 kHz.

As seen from Fig. 20, IC9, IC10, and IC11 form a synchronous divide-by-5 counter. The gating in IC1 in Fig. 20 merely changes the duty cycle of the 10-KHz signal from IC4 in Fig. 19. The 100-kHz signal is used for the clock signal in the divide-by-5 and the divide-by-11 counter. In Fig. 20, IC5, IC6, and IC7 along with the four-input gate of IC3 and the two-input gate of IC-2 form the divide-by-11 counter. The output of this counter provides the REF and $\overline{\text{REF}}$ signals (see Fig. 21 for the timing of these various signals).

The preset-strobe signal is formed with the four-input gate IC3. The preset-strobe signal PS is made to occur 10 msec before each 5.0-msec reference interval. This presets the counter to the new number and allows the counter to start counting as soon as the preset-strobe signal goes down.

As Fig. 19 shows, C3, R1, SW1, and the two four-input gates in IC2 form a network that insures that the counters and flip-flops in the reference interval generator come on in the proper states when the system is energized. If SW1, normally closed, is opened, the preset strobe line is held up so the five-stage BCD counter can be continuously preset for testing purposes.

In the previous discussion on the five-stage BCD counter, the $\overline{\text{SAMPLE}}$ and $\overline{\text{SAMPLE}}$ signals were generated. As will be recalled, in the earlier discussion it is the timing of the reference interval of REF and $\overline{\text{REF}}$ signals and the $\overline{\text{SAMPLE}}$ and $\overline{\text{SAMPLE}}$ signals that generates the error signal and ultimately the VCO correction voltage.

Figure 22 shows the sample-and-hold circuitry. IC5 and 1/4 IC1 perform the gating of the sample and reference signals generating the error signal. The timing of this gating arrangement is shown in Fig. 23. Figure 23A shows the case where VCO frequency is too high and the five-stage BCD counter reaches the all-9's condition before the end of the reference interval and consequently the sample signal is not coincident with the reference signal. Thus the error signal, when the VCO frequency is too high, is made up of $\overline{\text{SAMPLE}} \cdot \overline{\text{REF}}$. This signal occurs on the output of 1/4 IC1 or at TP3 in Fig. 22. Figure 23B illustrates the case where the VCO frequency is too low and the BCD counter is not filled up to the all-9's condition during the reference interval. Again the sample

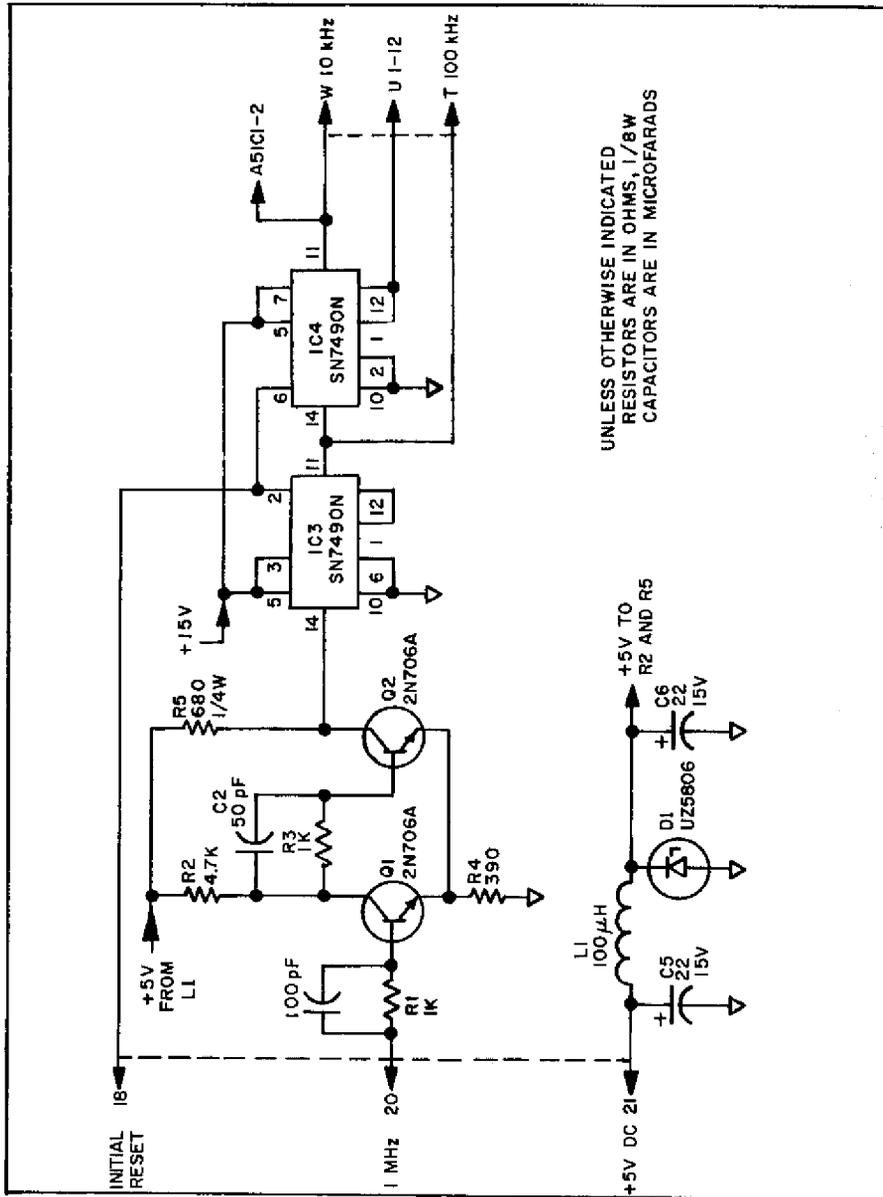


Fig. 19 - Reference interval generator

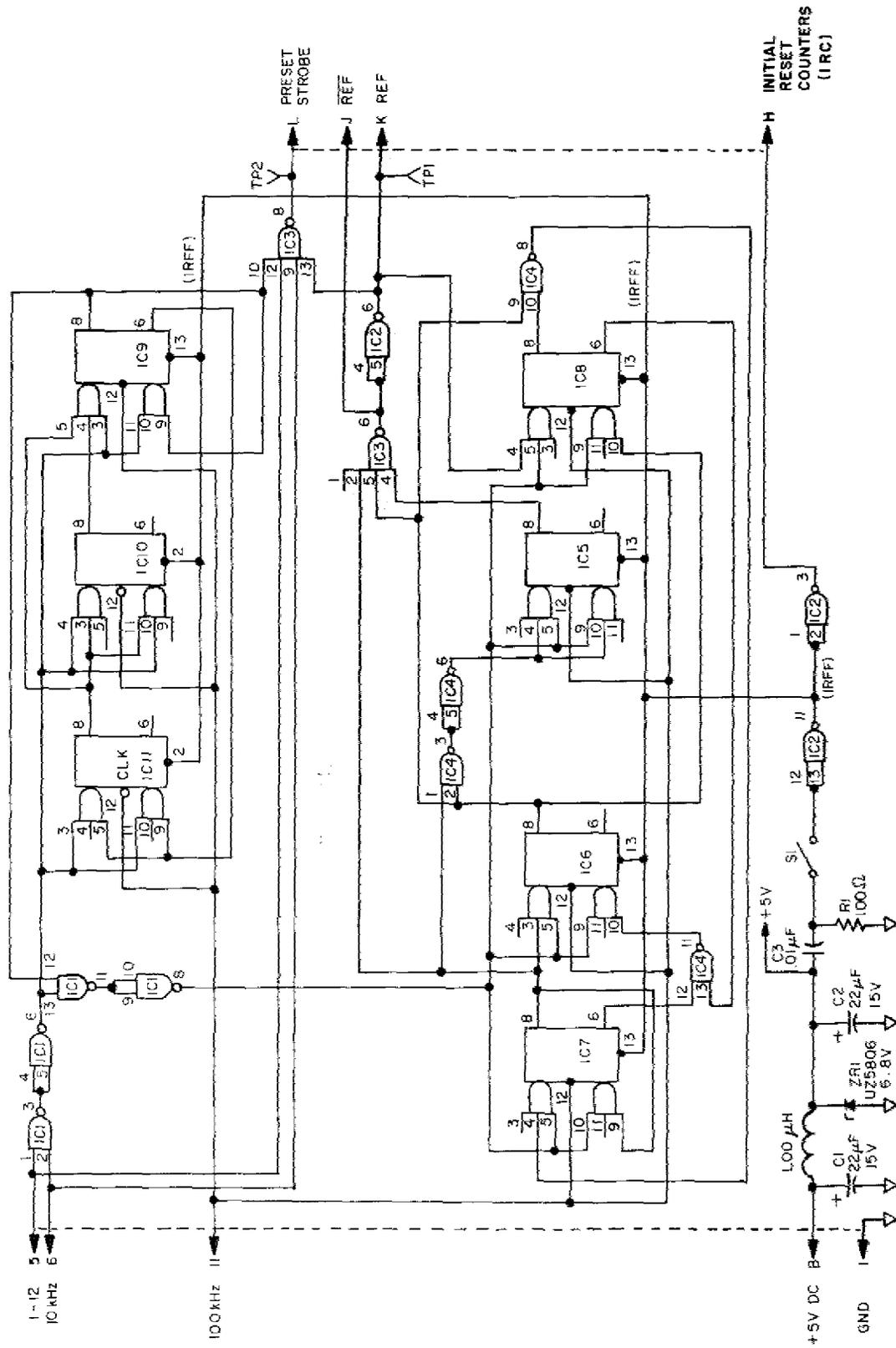
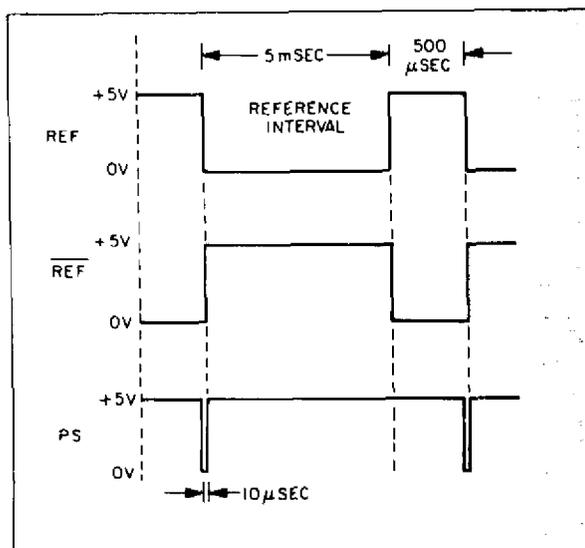


Fig. 20 - Reference generator

Fig. 21 - Timing of the preset-strobe signal



and reference intervals are not in coincidence. Thus, the error signal in this case is made up of $\text{REF} \cdot \overline{\text{SAMPLE}}$ and is inhibited by the preset strobe signal PS in order to prevent corrections from being made during presetting of the BCD counter.

It is well to note that when the VCO frequency is correct, the sample and reference signals are coincident and no output occurs at either of the two error-signal lines described above.

With reference again to Fig. 22, when the VCO is either too high or too low in frequency, the appropriate error signals are generated and applied to IC6. This is a dual-FET analog switch that is used to charge or discharge capacitor C15 through resistors R4 and R5. As described earlier, when the VCO frequency is low, a positive error signal is generated and applied to the input of the analog switch IC6. This causes a positive 5-volt signal to charge capacitor C15 through resistor R4. The capacitor will essentially hold the value it is charged to until the next error voltage is generated at the next sample interval. When the VCO frequency is high, an error voltage is generated on the other input to the analog switch. This generates a negative 5-volt signal to discharge C15 through R5.

It is well to note that the amount that capacitor C15 is charged and discharged is directly proportional to the width of the error signals. The time constants are arranged in such a way that the synthesizer will lock into the proper frequency in less than 200 msec.

The correction voltage generated in this fashion is basically now a dc level. This dc level is isolated by a high-input-impedance voltage-follower amplifier IC7. This amplifier has unity gain and serves merely to isolate the time constant of C15 from the other circuitry. This dc level is then fed to the dc-amplifier circuitry. The digital-to-analog-converter circuit also provides a voltage to the dc-amplifier circuit.

Figure 24 is the schematic diagram of the digital-to-analog converter. The function of this circuitry is to provide a coarse-tuning voltage to the VCO through a buffer amplifier and the dc amplifier. Thus, as the thumbwheel switches are tuned from 136,000 MHz to 139,000 MHz, the BCD output of these switches is converted to a dc level that coarsely tunes the VCO to the approximate frequency. The sample-and-hold circuit then provides the fine tuning of the VCO to the exact frequency.

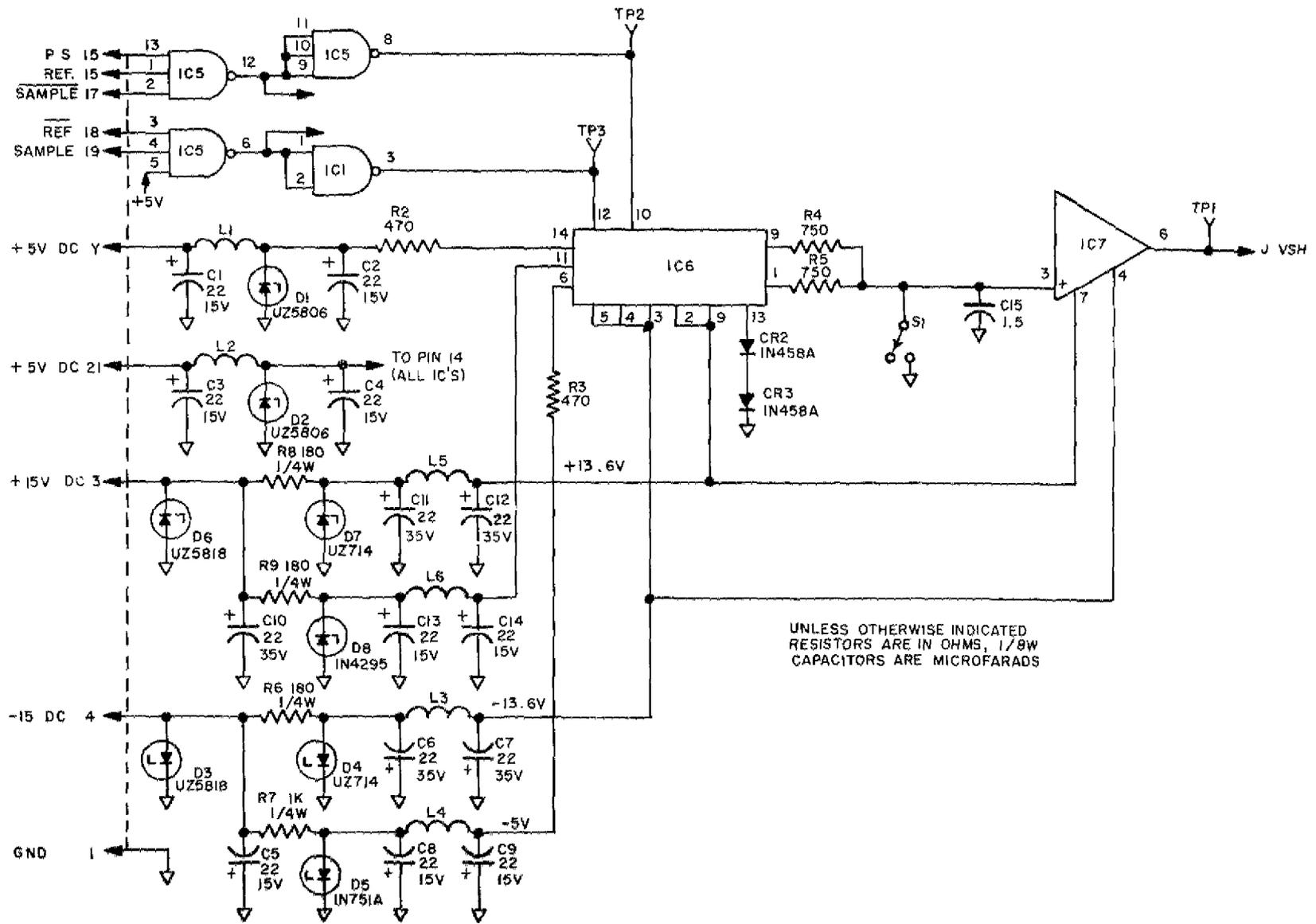
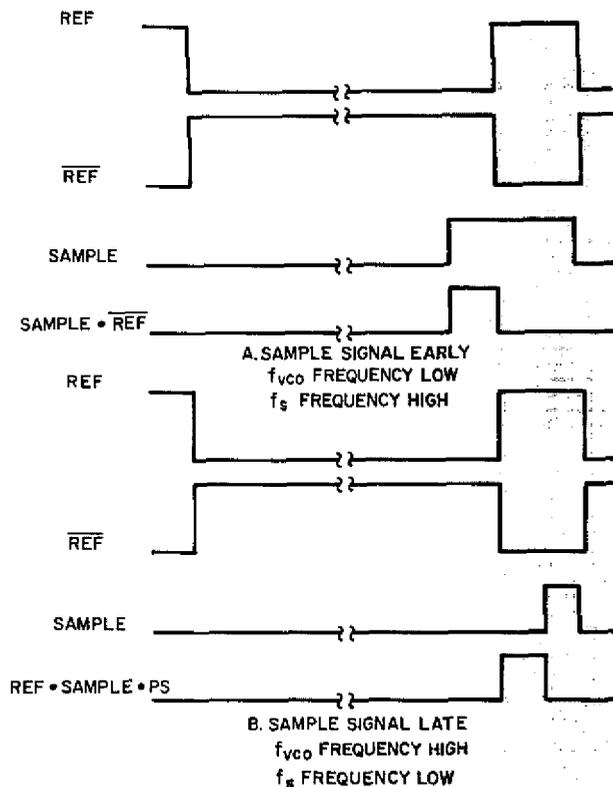


Fig. 22 - Sample-and-hold circuitry

Fig. 23 - Timing of signals in the generation of the error signal



Not all the bits from the BCD thumbwheel switches are used in the digital-to-analog converter. The first bit on the most significant decade, the first and second bits on the next most significant decade, and all four bits on the third most significant decade are the only bits used to feed the digital-to-analog converter. IC1 in Fig. 24 operates on the three most significant bits to provide two actual bits to the digital-to-analog converter.

Transistors Q_1 through Q_6 form the actual six-bit digital-to-analog ladder conversion network. These transistors are used as switches, normally open or not conducting. They are actuated by the positive-going signal on the base. This effectively places the collector resistor of the switching transistor in parallel with any other transistors in the ladder that are conducting and in series with R13 and R14. Thus the digital-to-analog ladder conversion network, equivalent circuitwise, is a variable voltage divider made up of R13 and R14 forming the fixed part and the ladder network forming the variable portion. So, as the thumbwheel switches are tuned from 136,000 MHz to 139,000 MHz, the resistance of the ladder network is continuously decreased, causing the voltage of TP1 to decrease in a continuous fashion.

IC1 in Fig. 24 insures that the three most significant bits from the thumbwheel switches also present a linearly changing (increase or decreasing) bit pattern to the ladder network. The output of the ladder network is fed to the dc amplifier through the buffering voltage follower IC2.

Figure 25 shows the dc-amplifier schematic. This amplifier provides the proper dc gain in the feedback loop from the error circuitry and digital-to-analog converter to the control voltage for the VCO. This circuit has two signal inputs: one from the digital-to-analog converter and V_{sh} from the sample-and-hold circuitry. R19 provides gain adjustment for the dc amplifier.

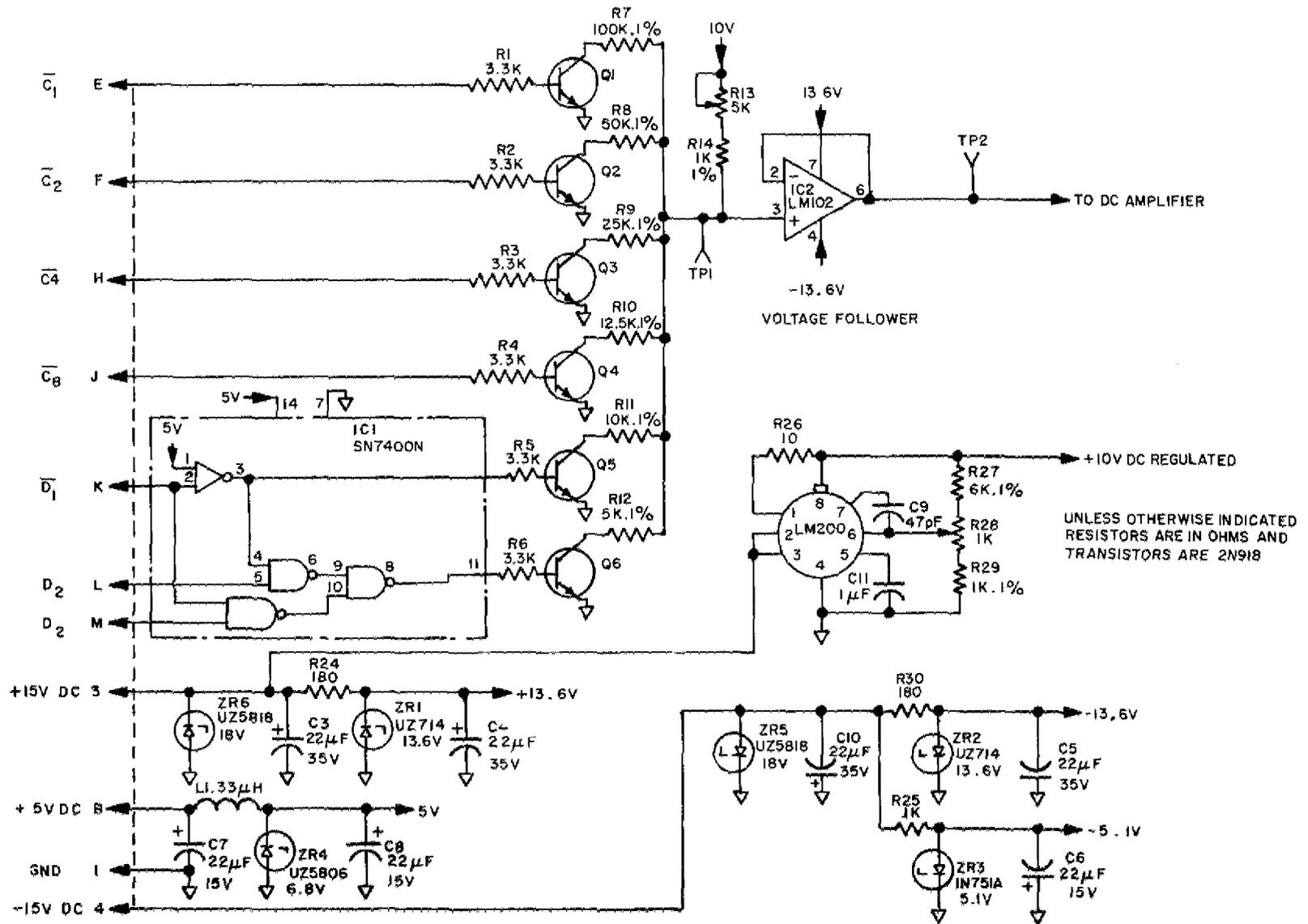


Fig. 24 - Digital-to-analog converter

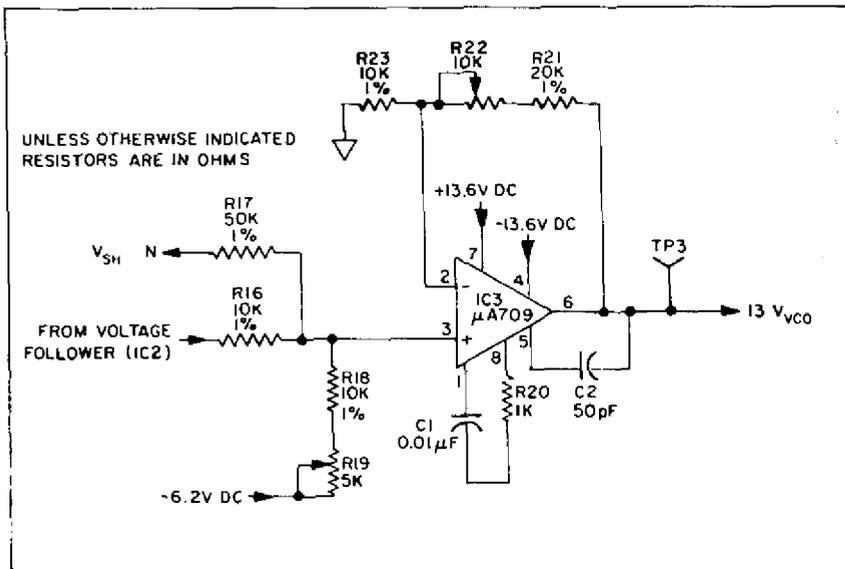


Fig. 25 - Dc amplifier

Figure 26 shows the unlock indicating circuitry. This circuitry performs two functions: it indicates whether the 10 kHz from the 1-MHz countdown reference generator is functioning, and it indicates whether the error signals that are being generated are being caused by frequency errors in excess of 1 kHz.

The 19-kHz or 1-MHz indicating circuitry receives a 10-kHz signal generated in the reference-interval generator by dividing the 1-MHz signal by 100. This signal is buffered by two inverters of IC-1 and then peak-detected by diode CR1, capacitor C4, and resistor R6. A dc level is generated at this point which, when compared to the reference signal on the other input to the voltage comparator (IC8's output) is held high, and the lamp driver Q3 is not turned on. If the 10-kHz or 1-MHz signal is removed, the voltage at the output of the peak detector drops and the output of the voltage comparator falls, causing Q3 to conduct and the unlock lamp to come on.

Transistor Q3 is driven by nor gate IC1 to allow two functions to activate the unlock lamp. The second function that can activate the unlock lamp is the error-detecting circuitry. This circuitry, also shown in Fig. 26, is basically a pulse-width discriminator and two decade counters. The two inputs to this circuit are the two error signals described earlier formed by $\overline{\text{REF}} \cdot \text{SAMPLE}$ and $\overline{\text{REF}} \cdot \text{SAMPLE} \cdot \text{PS}$. These signals are nor-gated together, and the output is sent to a pulse-width discriminator.

As stated earlier this circuitry is designed to detect frequency errors in the synthesizer of greater than 1 kHz; this corresponds to an error pulse width of approximately 330 msec from the error-detecting circuitry. Consequently when the input to the pulse-width discriminator is a pulse of width greater than 330 msec, the first decade counter IC5 is incremented. When this counter reaches the count of eight, two JK flip-flops of

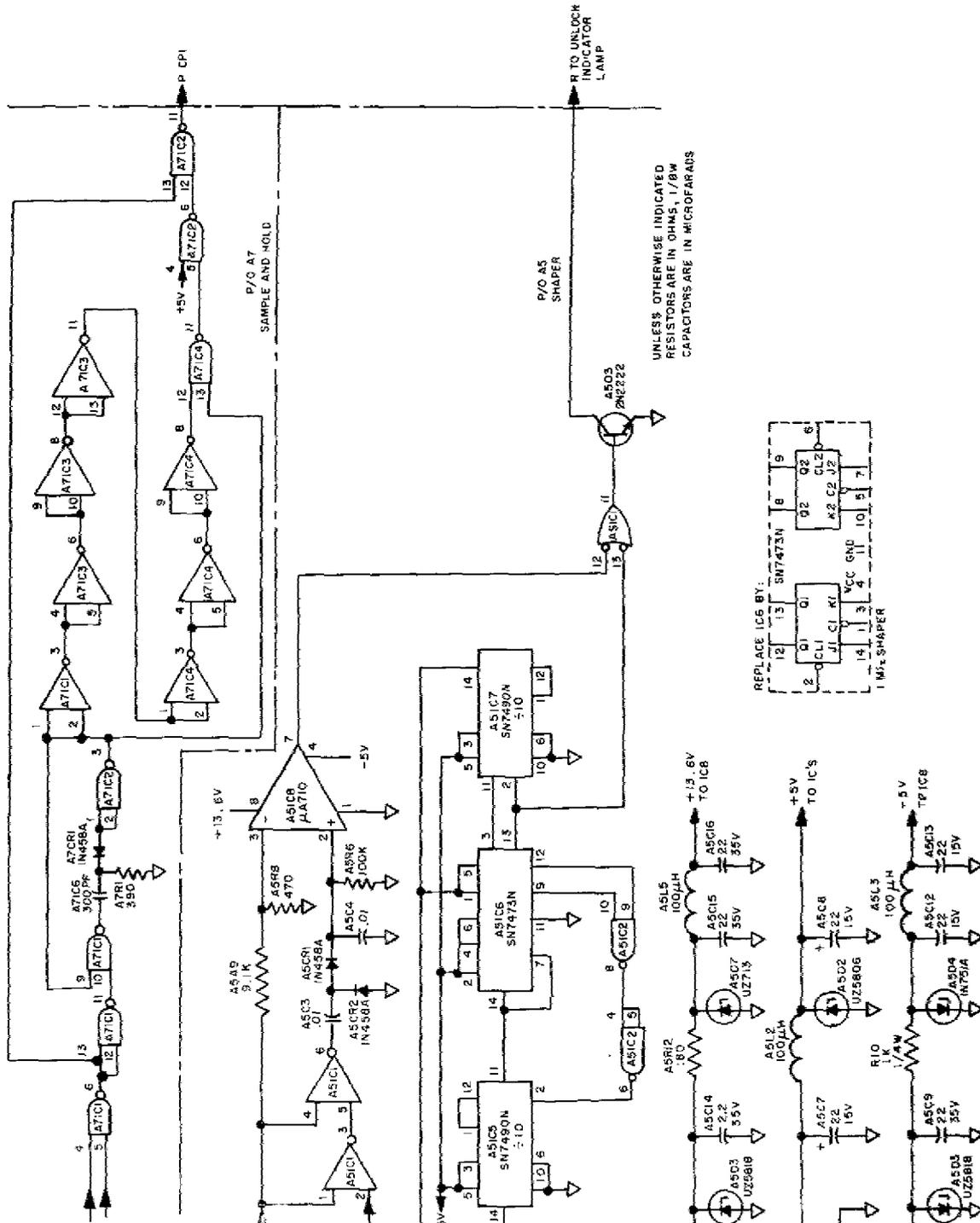


Fig. 26 - Unlock circuit

msec. So the unlock light will blink on and off at this rate. When the 1-MHz or 10-kHz signal is removed, the unlock light will be activated continuously.

DESIGN OF THE COMPARATOR CIRCUITRY

The comparator portion of the receiver must decide which of the incoming polarizations has the best S/N and switch the receiver output to look at the proper polarization or channel. In this receiver the decision is based on the agc voltages of the two channels. Figure 27 is a block diagram of the comparator circuit, Fig. 28 is a schematic diagram, and Fig. 29 is a photograph. The comparator is a separate module to facilitate maintenance.

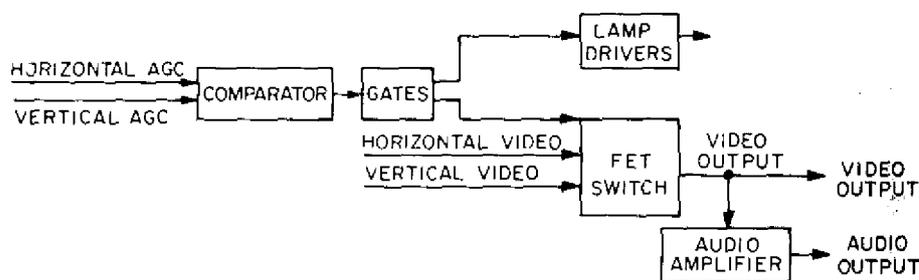


Fig. 27 - Comparator

With reference to Fig. 28 the agc voltages are decoupled by L1, C1, and C5 and L2, C2, and C6. This eliminates any ac that may have been picked up. The two agc voltages are compared by the UA710 comparator. The 180-kilohm or feedback resistor gives 2 dB of hysteresis to the comparator. The output of the comparator controls the DG144L metal-oxide-semiconductor FET switch. This IC acts as a SPDT switch, switching the output to the desired video input. The output of the comparator also controls light drivers which activate lights located on the front panel of the receiver. This allows an operator to visually check for correct operation. The video output of the switch goes to a driver which drives the output connector on the back panel and the single-ended push-pull audio amplifier. This video amplifier amplifies the audio signal, and the output is fed to a connector on the rear panel of the receiver.

ACKNOWLEDGMENTS

The authors are grateful to Lee Hammarstrom for reviewing the manuscript and making valuable suggestions and to Paul Oesterling and Vito Navarro for their help in constructing the prototype unit.

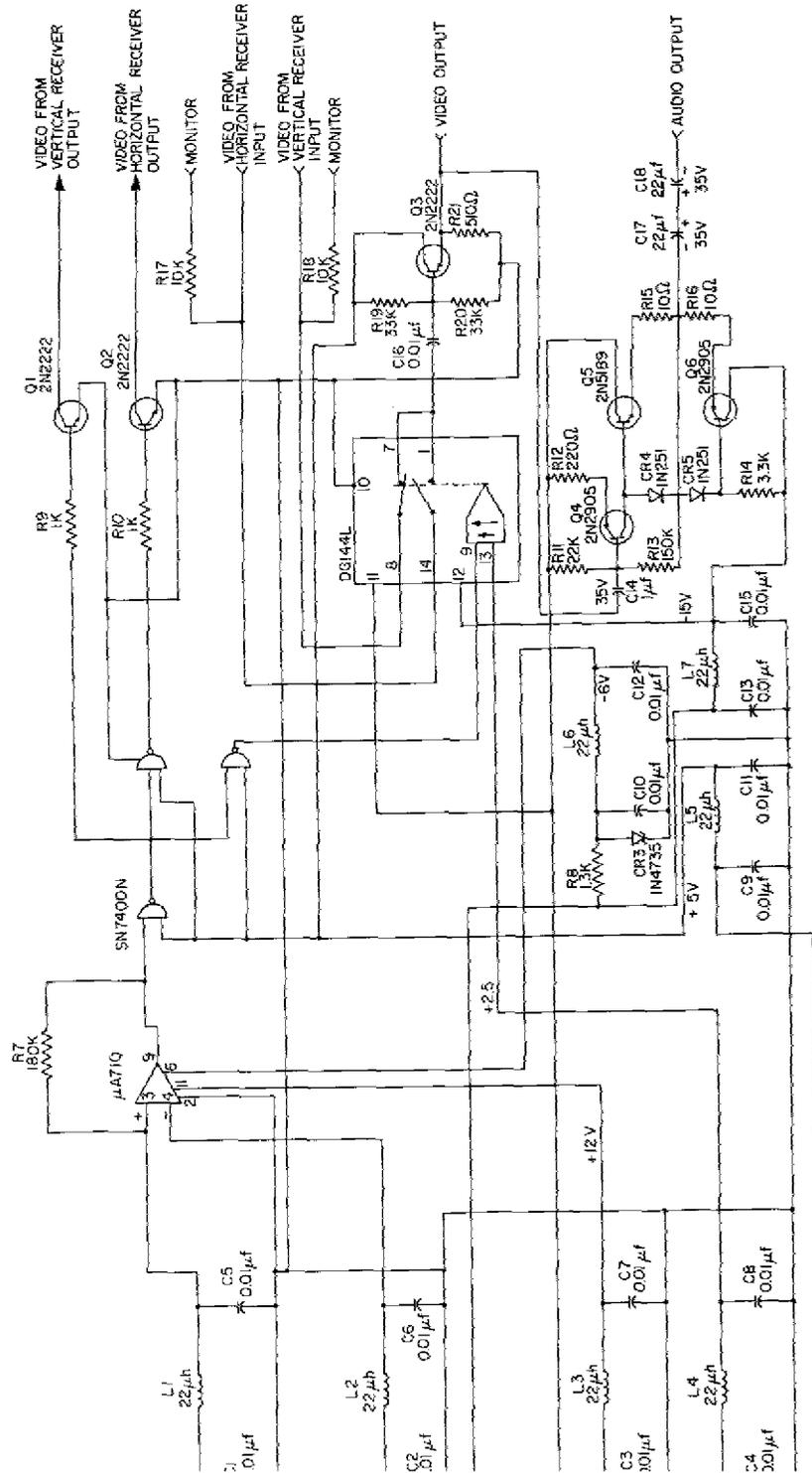


Fig. 28 - Comparator

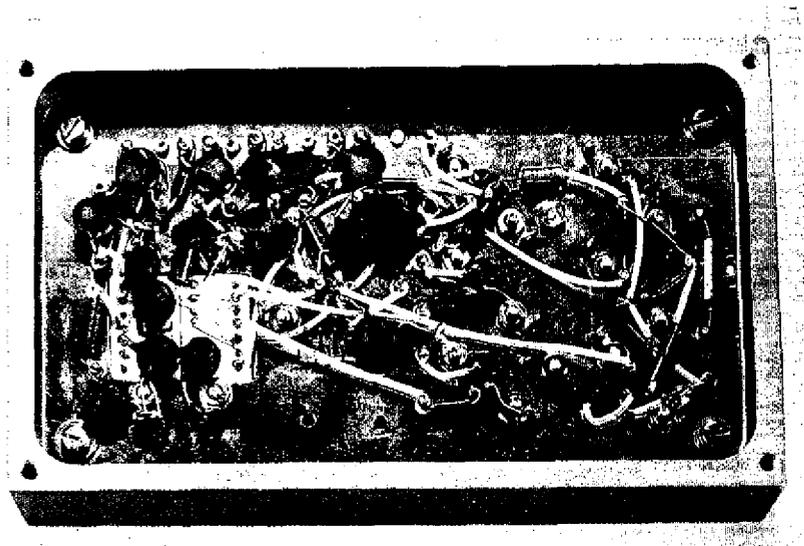


Fig. 29 - Comparator

BIBLIOGRAPHY

1. Schwartz, M., Bennett, W.R., and Stein, S., "Communication Systems and Techniques," New York:McGraw-Hill, 1966
2. Blair, W.L., and Ammerman, C.R., "Effect of Bandwidth on Receiver Sensitivity," HRB-Singer, Inc., Internal Report
3. Blake, L.V., "Antenna and Receiving-System Noise-Temperature Calculation," NRL Report 5668, Sept. 1961