

Microstrip Design Procedure for L-Band Transistor Power Amplifiers

G. T. O'REILLY, R. E. NEIDERT, AND H. E. HEDDINGS

*Microwave Techniques Branch
Electronics Division*

June 27, 1974



NAVAL RESEARCH LABORATORY
Washington, D.C.

Approved for public release; distribution unlimited.

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER NRL Report 7745	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) MICROSTRIP DESIGN PROCEDURE FOR L-BAND TRANSISTOR POWER AMPLIFIERS		5. TYPE OF REPORT & PERIOD COVERED An interim report on one phase of a problem.
		6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) G.T. O'Reilly, R.E. Neidert, H.E. Heddings		8. CONTRACT OR GRANT NUMBER(s)
9. PERFORMING ORGANIZATION NAME AND ADDRESS Naval Research Laboratory Washington, D.C. 20375		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS NRL Problem R02-46 WF 12 111 704
11. CONTROLLING OFFICE NAME AND ADDRESS Department of the Navy Naval Air Systems Command Washington, D.C. 20361		12. REPORT DATE June 27, 1974
		13. NUMBER OF PAGES 46
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		15. SECURITY CLASS. (of this report) Unclassified
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE
16. DISTRIBUTION STATEMENT (of this Report) Approved for public release; distribution unlimited.		
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)		
18. SUPPLEMENTARY NOTES		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) Microstrip matching circuits Microwave amplifiers Power amplifiers Transistor amplifiers		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) A procedure which uses microstrip matching circuits was formulated for designing L-band transistor power amplifiers. The procedure uses a precision measurement technique for transistor impedances and an optimization routine for realizing the required matching circuits in microstrip.		

20. Continued

A model for large step discontinuities in microstrip was developed and was included in a computer optimization program. Good agreement was obtained between measured and calculated microstrip circuit impedances.

The computer-aided procedure was used to develop L-band, class C, pulse-operated transistor power amplifiers. Significant improvement was obtained in power gain, bandwidth, and collector efficiency over amplifiers designed by more conventional methods.

CONTENTS

INTRODUCTION	1
Transistor Structures	1
Equivalent Circuits	5
Present Design Techniques	7
Purpose	7
EXPERIMENTAL TECHNIQUE	8
Circuit Analysis	8
Transistor Measurements	10
RESULTS	12
Step Junction Circuit Model	12
Matching Network Optimization	16
Transistor Measurement	17
Amplifier Design	17
Amplifier Performance	18
DISCUSSION	20
Junction Model	20
Transistor Impedances	20
Transistor Power Amplifiers	23
CONCLUSIONS	26
ACKNOWLEDGMENTS	28
REFERENCES	28
APPENDIX A — Program NACORZ	31
APPENDIX B — Program for Optimizing Impedance- Matching Circuits	35
APPENDIX C — Measured Transistor Circuit Impedances	42

MICROSTRIP DESIGN PROCEDURE FOR L-BAND TRANSISTOR POWER AMPLIFIERS

INTRODUCTION

In recent years, several manufacturers have been successful in the construction of transistors capable of output power on the order of tens of watts at frequencies up to 2 GHz [1-11]. This advance has been made possible through state-of-the-art improvements in manufacturing processes that permit reliable production of devices with the small active-area dimensions required for operation at microwave frequencies.

However, the design of networks associated with microwave power amplifiers has lagged significantly behind the already maturing device technology. The network design approach has been relatively unsophisticated, relying on trial and error experimental procedures. It was anticipated that significant improvement in amplifier performance could be achieved with the use of numerical computation techniques.

A computer-aided design method was developed during this work. It required the formulation of a junction model for large step discontinuities in microstrip circuits, the development of a precision measurement procedure, and an optimization routine for the realization of the required matching circuits.

Transistor Structures

An insight into some of the problems associated with the network design can be obtained from a review of transistor structures and the experimental design techniques.

A simplified picture of transistor manufacture commences with a *p*-type epitaxial layer deposited on a silicon substrate. An *n*-type base is diffused into the epitaxial layer through a window chemically etched into a previously deposited SiO₂ layer. Another SiO₂ layer is deposited, and a second, or emitter, window is etched. The *p*-type emitter is diffused into the base region, and a platinum silicide contact metal is deposited between the silicon and surface metal. Then a gold or aluminum film is deposited on each region. Base and emitter external connections are provided by thermal-compression bonding of small wires onto the respective regions.

Specific process controls, etching techniques, active region dimensions, and metalization processes and materials are closely guarded proprietary items; however, the basic structures are generally revealed.

The interdigitated emitter structures are depicted in Fig. 1. Devices can employ either discrete emitter "fingers" (Fig. 1a) or a continuous emitter comb (Fig. 1b). The metalization

Note: Manuscript submitted March 6, 1974.

pattern is the same for both structures. Figure 2 shows the most common modification of interdigit structure, the "fishbone" structure. The emitter tree is interdigitated in two dimensions with a base tree consisting of a highly doped p -type material diffused into the base region. The chief advantage of this modification is in increased emitter-periphery-to-base-area ratio, which increases the base injection current.

The overlay structure, Fig. 3, uses several discrete emitter sites diffused into the base region. A high-conductivity p^+ grid is used to conduct base current from the emitter to the base contacts. This structure permits wider and thicker metalization, thereby lowering the current density.

Finally, the mesh or inverse overlay structure is shown in Fig. 4. Here an emitter grid is diffused into the base region, forming a structure that is essentially the inverse of the overlay structure. This geometry further increases the emitter-periphery-to-base-area ratio.

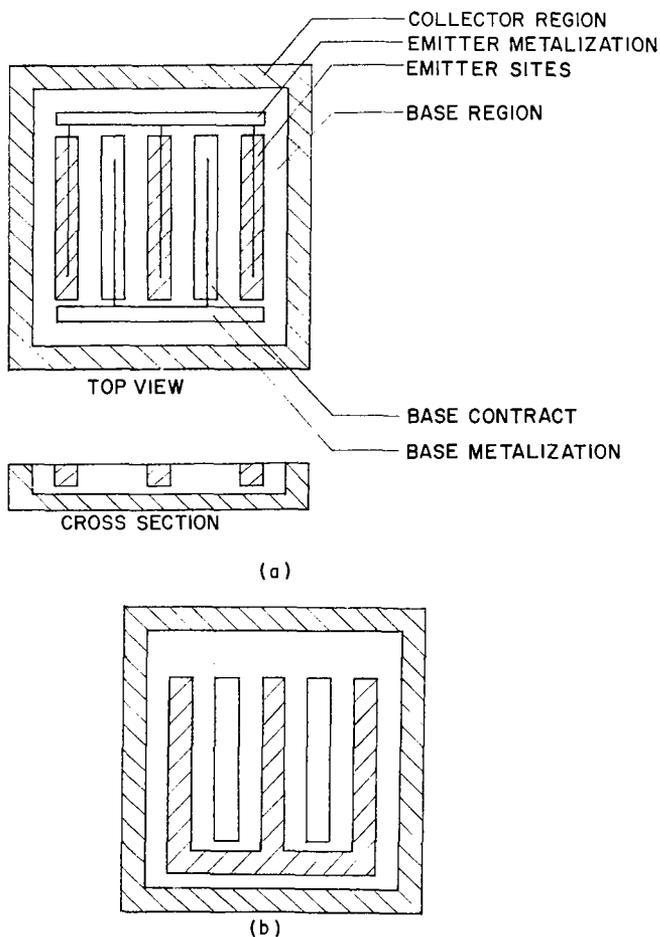


Fig. 1 — Interdigitated emitter structure. (a) Discrete emitter sites. (b) Continuous emitter comb.

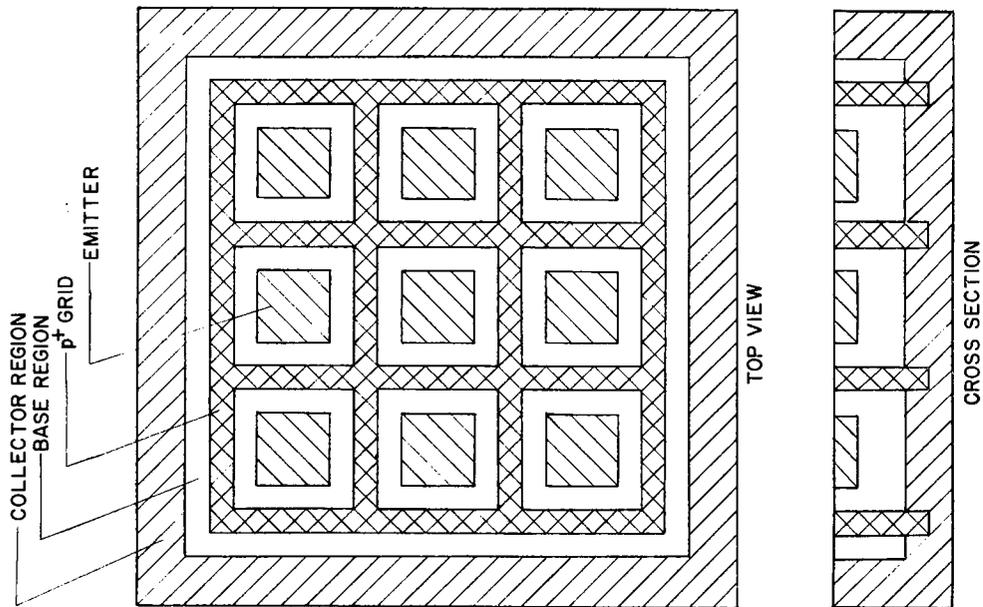


Fig. 3 — Overlay structure

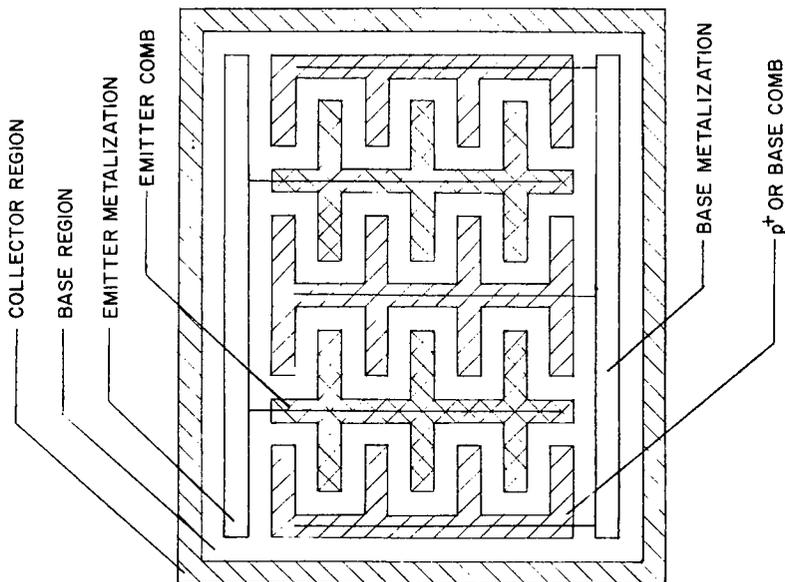


Fig. 2 — Fishbone structure

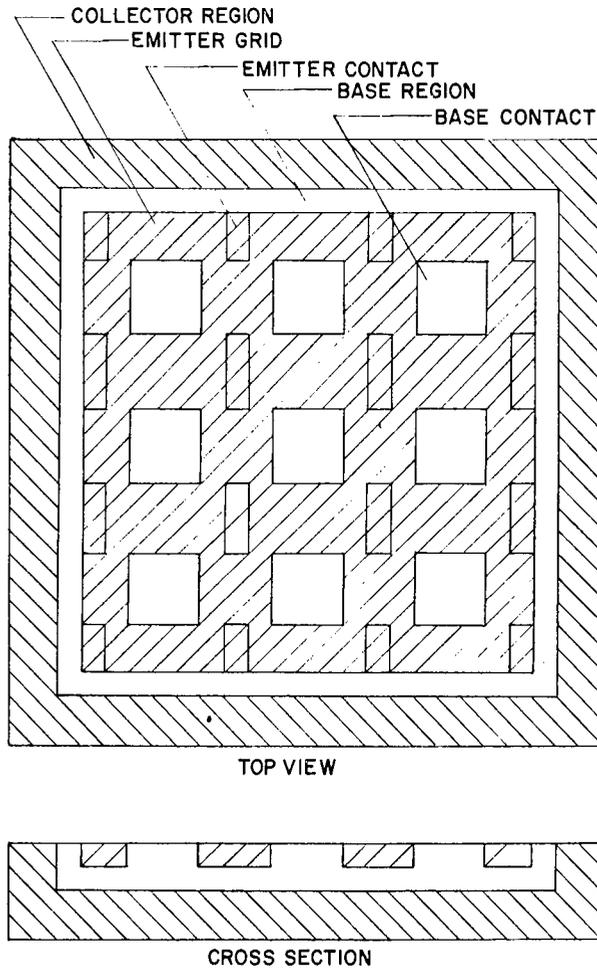


Fig. 4 — Mesh structure

Because the power-handling capabilities of each transistor cell are always limited by the device geometry, high-power transistors generally are composed of more than 1 cell and may have as many as 16 basic cells connected in parallel. As a result, the input impedance of a high-power transistor is generally very low, presenting a formidable impedance matching problem. An enlarged photograph of a multicell transistor is shown in Fig. 5.

Each of these transistor structures, or geometries, and the particular metalization used can be shown to have both relative advantages and disadvantages (12-14). The processing of the interdigitated structure is simpler than the processing of the overlay structure, and the fishbone modification has a high emitter-periphery-to-base-area ratio, which minimizes C_{ob} . Another advantage of this structure is its high current-handling capability per unit length of emitter periphery. This structure is subject to metal migration, has high finger current density, and has only fair ballasting resistor capability. The advantages of the overlay structure are that it has

the lowest finger current density; good ballast resistor capability; and the thickest metalization, which limits migration. The disadvantages of the overlay structure are its low emitter-periphery-to-base-area ratio and the debiasing of the central sections by a voltage drop in the p^+ grid. The advantages of the mesh structure, are its high emitter-periphery-to-base-area ratio and its process, which requires fewer steps than with the overlay structure. Its disadvantages are its poor ballast resistor capability and its thin metalization which is subject to metal migration.

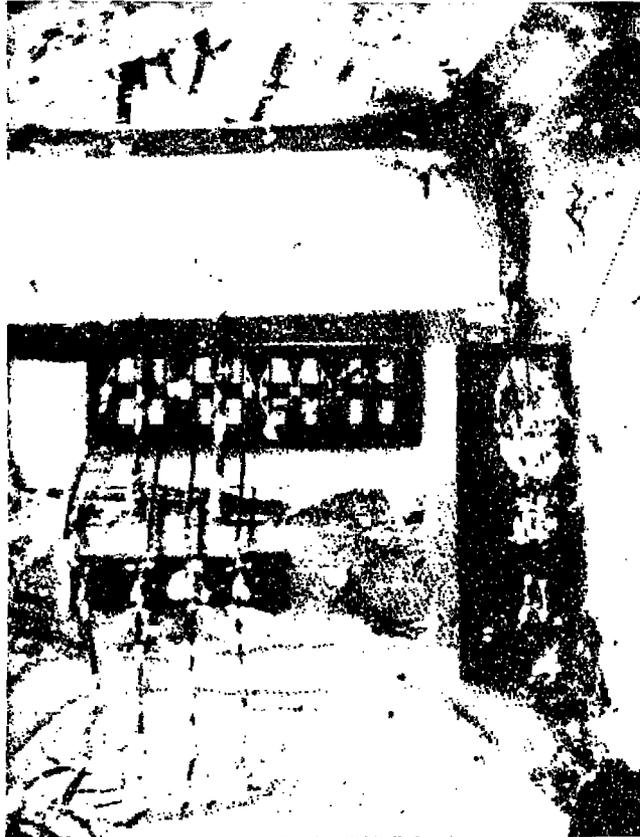


Fig. 5 — A multicell transistor

Until now there was little information available that would enable a microwave amplifier design engineer to select a transistor based on the performance of the transistor when incorporated into an integrated circuit amplifier. This research includes study of the properties of some of the three structural-type transistors in amplifier applications.

Equivalent Circuits

For low-frequency, small-signal, operation, the hybrid π circuit serves as an extremely adequate model for a bipolar transistor operated within the active region [15]. Dynamic

charge control models have been developed that describe transistors being operated outside the active region [16, 17]. Because many of the elements that become significant at microwave frequencies are not included in these models, their application is necessarily restricted as the operating frequency increases.

Small-signal equivalent networks for microwave transistors are derived from the scattering parameter measurements for the properly biased transistor [18-20]. Reasonable results have been presented for the comparison between the theoretical and experimental scattering parameters [18]. It has also been shown that low-noise amplifiers can be realized through use of these scattering parameters [21].

The scattering parameter measurement technique is applicable only to small-signal operation of transistors in their linear region. Because microwave power transistors are operated as class C common-base amplifiers, a nonlinear model must be used for this mode. The most significant attempt to model microwave power transistors was a time-variable extension of the Ebers-Moll model by Lange [22, 23]. The model, Fig. 6, has 35 elements for a single cell. The active inner base region was divided into three sections and the outer region into two sections with an auxiliary circuit for the three active sections similar to that of the Ebers-Moll model. The elements for the model are defined as follows:

C_c	= direct base-collector capacitor
C_o	= capacitor of the outer section of the base
$J_{B1, B2, B3}$	= base-collector current generators
$C_{1, 2, 3}$	= emitter capacitors
C_i	= capacitor of the inner section of the base
$J_{1, 2, 3}$	= current through the emitter diodes
R_o	= resistor of the outer section of the base
R_i	= resistor of the inner section of the base
R_A	= resistor of the auxiliary circuit
C_A	= capacitor of the auxiliary circuit.

Because the correlation between theoretical and experimental results is somewhat less than ideal, an application of this model, expanded for a multicell device, would lead to an unwieldy number of elements and to even more questionable results.

This limited success of modeling for transistors operated as class C amplifiers would indicate that its application to transistor amplifier design is not presently the optimal approach. A more practical approach would be to measure transistor impedances for single-frequency operation and to use these impedances to generate broadband matching circuits.

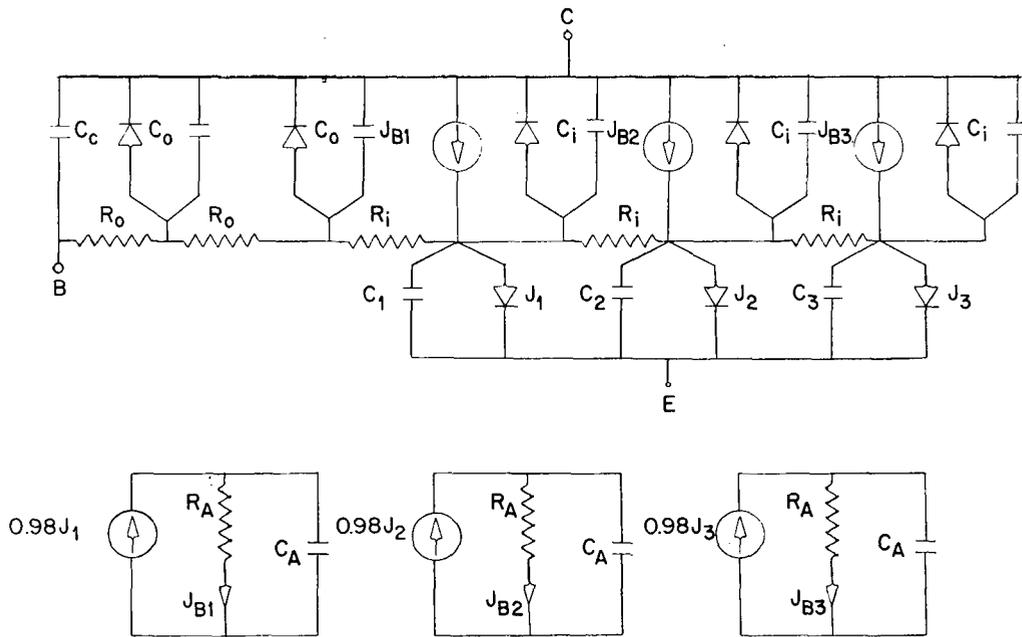


Fig. 6 — Lange transistor model

Present Design Techniques

The present approach to the design of large-signal microwave amplifiers is largely empirical, requiring several design iterations and giving only secondary consideration to the transistor and its pertinent characteristics. The transistor is generally placed between two tuners, which are then adjusted to give the best result over the desired bandwidth. The impedances from the transistor into the tuners are measured, and an approximate circuit is estimated from these measurements. Matching circuits are then constructed, usually in microstrip, and placed between the tuners and the transistor. Then a second iteration is begun. The process continues until an acceptable result is obtained. The tuners can be either stub tuners or, for more accurate measurement, microstrip lines overlaid with conducting tape.

Single-stage amplifiers have been constructed at the U.S. Naval Research Laboratory having a power output on the order of 40 W with a 10% 1-dB bandwidth with a procedure similar to that described [24]. Recently, Westinghouse Electric Corp. successfully achieved 1 kW at 1.25 GHz using the same procedure with twelve 100-W amplifiers having paralleled amplifier stages [25].

Purpose

The purpose of this research was to investigate the fundamental characteristics of microwave power transistors operated as class C power amplifiers and to use these

characteristics in a computer-aided design procedure. In particular, input and output impedance measurements were made for some transistors of the various structural types. Because these impedances can be on the order of 1Ω , an accurate method of measurement had to be developed. It was anticipated that a transistor selection for a particular application could be based on these impedance measurements.

The impedance-matching circuits were to be constructed using microstrip circuits on alumina substrates incorporating impedance transformation sections. This matching technique required an accurate model for step discontinuities in microstrip. This model was required for circuit generation with the use of a computer-aided design procedure.

The techniques developed were used to generate broadband transistor power amplifiers that did not require tuning for final operation.

EXPERIMENTAL TECHNIQUE

The development of computer-aided design of microwave power amplifiers encompassed three separate, but related, phases of research. First, an equivalent circuit for discontinuities in microstrip circuits was developed by empirical methods. The model was then incorporated into a computer program for the synthesis of microstrip impedance-matching circuits. Finally, an accurate measurement procedure was developed to evaluate the impedance characteristics of the various types of microwave power transistors. The computer optimization program was then used to generate the appropriate impedance-matching networks.

Circuit Analysis

Electromagnetic propagation in microstrip structures has been a subject of intense study during the past several years [26-31]. A microstrip transmission line is a parallel two-conductor line: one conductor is a small strip separated by a dielectric (for example, alumina) from the larger second conductor, which acts as a ground plane. Propagation can best be defined as a quasi-static, or approximate, transverse-electric-magnetic (TEM) mode [32, 33]. The approximation is very accurate at lower frequencies and for lines of sufficiently small dimensions. Equations are available for characteristic impedance, effective dielectric constant, wave velocity, and attenuation [34].

The empirical determination of an equivalent circuit for step discontinuities in microstrip began with the establishment of an extremely accurate impedance measurement technique. Several microstrip circuits similar to the one in Fig. 7 were fabricated with subminiature adapters (SMA) at both ends. One port was terminated by a $50\text{-}\Omega$ load, and the input impedance at the unterminated port was measured with a Hewlett-Packard Model 8410A Network Analyzer. The test setup is shown in Fig. 8. The errors inherent in the network analyzer were minimized in a manner similar to that presented by Hand [35]. An errorless network analyzer was assumed and was connected to an error network as shown in Fig. 9. The network analyzer was calibrated with an SMA-type short placed at

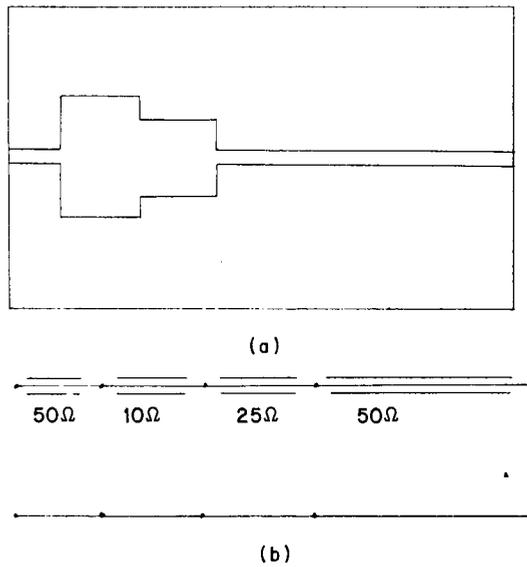


Fig. 7 — (a) Microstrip circuit. (b) Equivalent transmission line.

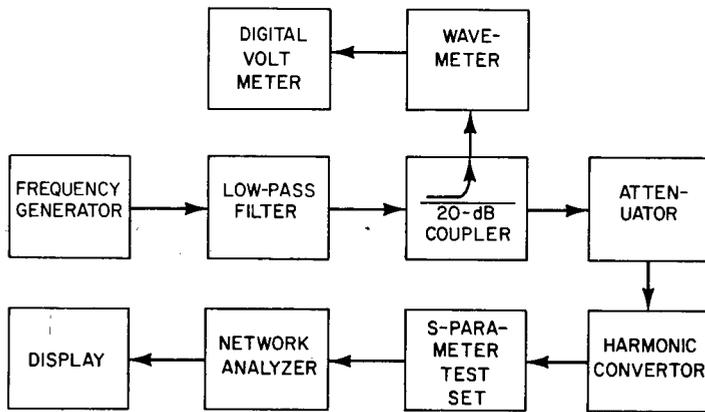


Fig. 8 — Impedance measurement test setup

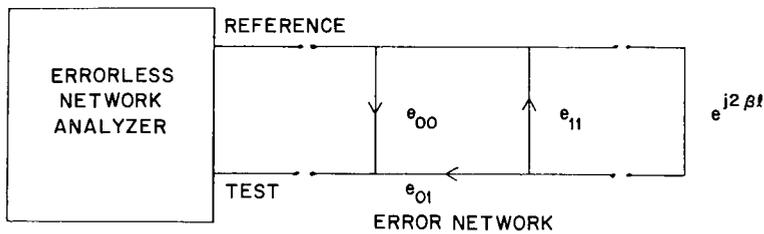


Fig. 9 — Signal flowgraph for network analyzer calibration

the face of the test port. Three offset shorts, of different lengths, were connected, and the values of the scattering parameter S_{11} were recorded. From basic theory, the measured value M_R of S_{11} is given by

$$M_R = e_{00} - \frac{e_{01} e^{-j2\beta l}}{1 + e_{11} e^{-j2\beta l}}. \quad (1)$$

The three error signals, e_{00} , e_{01} , and e_{11} , were determined at each frequency from the measured value M_R .

These values were used in the inverse equation

$$S_{11} = \frac{S_R - e_{00}}{S_R e_{11} + e_{01} - e_{00} e_{11}} \quad (2)$$

to correct the measured value S_R of the reflection coefficient for the circuits. A computer program, NACORZ, aided in calculating the input impedance from the corrected reflection coefficient S_{11} [36]. The impedance was rotated through the SMA connector. The program is included as Appendix A.

The effects of the step discontinuities were determined from the deviation between these measured values and those obtained from a transmission-line analysis.

Transistor Measurements

A three-section transistor test fixture, shown in Fig. 10, was fabricated to assist in transistor impedance measurements. The center section, on which the transistor was mounted, was placed between the two alumina substrates mounted on the outer sections. Each substrate had a single 50- Ω transmission line extending from the transistor tab to an SMA-type launcher at the outer edge. The collector supply voltage and ground return were incorporated through inductive coils.

The transistors were operated in the common-base configuration because of the packaging supplied by the manufacturers. The common-base configuration is usually used with microwave power transistors because the transistors can be operated at a higher gain and because stability is increased by a reduction in the common-lead inductance. At each frequency of interest, sections of indium foil were overlayed onto the 50- Ω line to approximate transmission-line matching sections until the desired operating characteristics were obtained. After the circuits had been optimized, the transistor test fixture was disassembled, and the impedances of the terminated microstrip circuits were measured. The measurements were made at the transistor side of the circuits by a Hewlett-Packard network analyzer with appropriate corrections. The process was repeated at several frequencies in the region of interest which provided a set of characterizing impedances. The test setup is shown in Fig. 11.

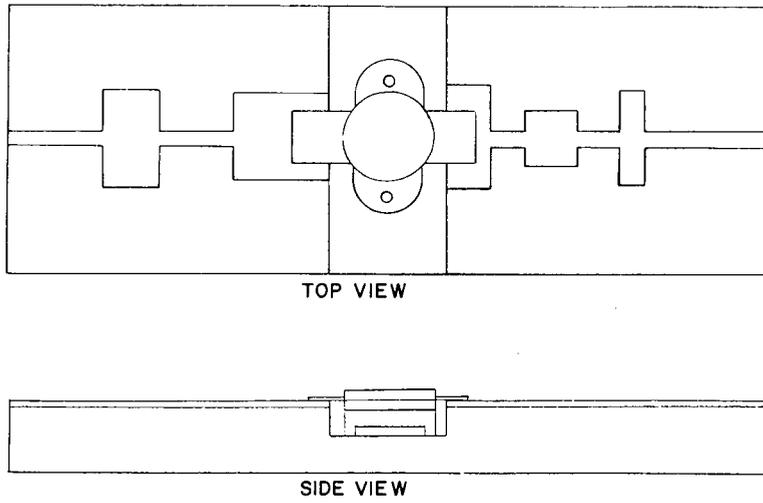


Fig. 10 - Transistor test fixture

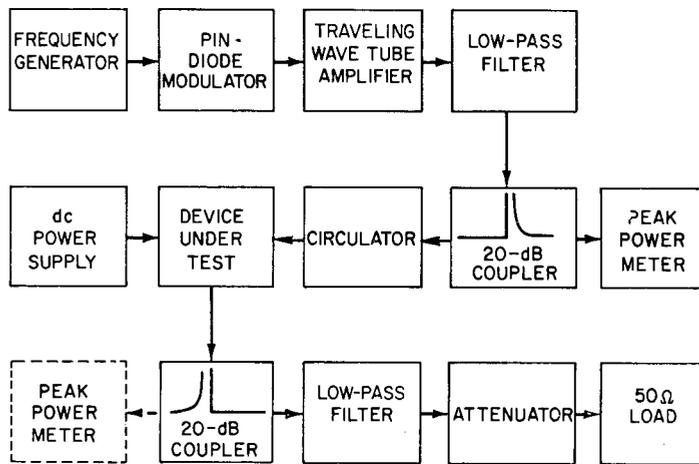


Fig. 11 - Transistor test setup

RESULTS

Step Junction Circuit Model

Discontinuities in microstrip circuits have been the subject of numerous papers in recent years [37-42]. Also, an earlier paper considered the problem of step discontinuities in balanced stripline circuits [43]. However, measurements of microstrip circuits indicated that the single-element equivalent circuits are not adequate to describe the effects of large step discontinuities. Calculated results using capacitive reactance or inductive reactance to describe the effects of the discontinuities did not agree with the measured results. In fact, the calculations indicated that no value of capacitance or inductance alone could adequately describe the junction effects in the 1- to 2-GHz region.

Both the capacitor and inductor equivalents did improve some of the calculated values, but each degraded other values. Empirical methods indicated that a combination of inductors and capacitors could improve many of the calculated values. The equivalent circuits considered are shown in Fig. 12. The values for the inductors and capacitors were initially based on those of the earlier papers and modified to obtain the best correlation with the measured values. Again, the best calculated results were still inadequate, indicating a need for a more complex model.

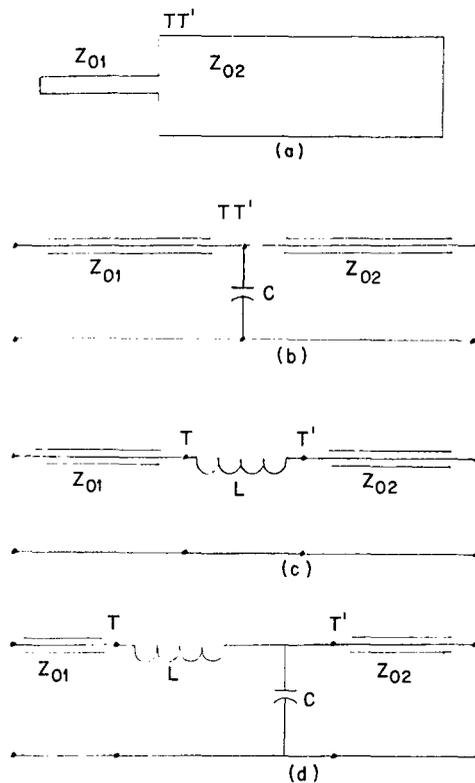


Fig. 12 —Junction models. (a) Step junction. (b) Shunt capacitance model. (c) Series inductor model. (d) *LC* model.

The addition of a series resistor significantly improved the impedance correlation. This resistor accounted for loss associated with the generation of higher order modes at the discontinuity. However, the data suggested that a distributed circuit model might be more appropriate for a computer programming application. A series of quarter-wave transformers was constructed with various line impedances. In all cases, the impedance steps were from 50Ω to a lower impedance and back to 50Ω . With a lossy section of transmission line used to represent the junction, the line lengths, characteristic impedance, and loss were varied until good correlation was obtained between measured values and calculated values. The results are shown in Figs. 13, 14, and 15. As would be expected, the impedance approached 50Ω and the line length approached zero as the step ratio approached unity. The final model is shown in Fig. 16.

Ideally, the process should have been repeated for various steps, but the microwave launchers were 50Ω , so it was not possible to isolate step discontinuities between two arbitrary impedances. In an attempt to account for these steps, it was anticipated that the characteristic impedance of the lossy section could be normalized to the higher impedance and the line length and loss could be maintained. A circuit with a series of arbitrary steps (Fig. 17) was constructed and measurements were taken. A comparison of these measurements with the calculated values for impedances with and without the junction model is shown in Fig. 18. The improvement indicated that the model was sufficiently accurate for inclusion in a computer-aided optimization routine.

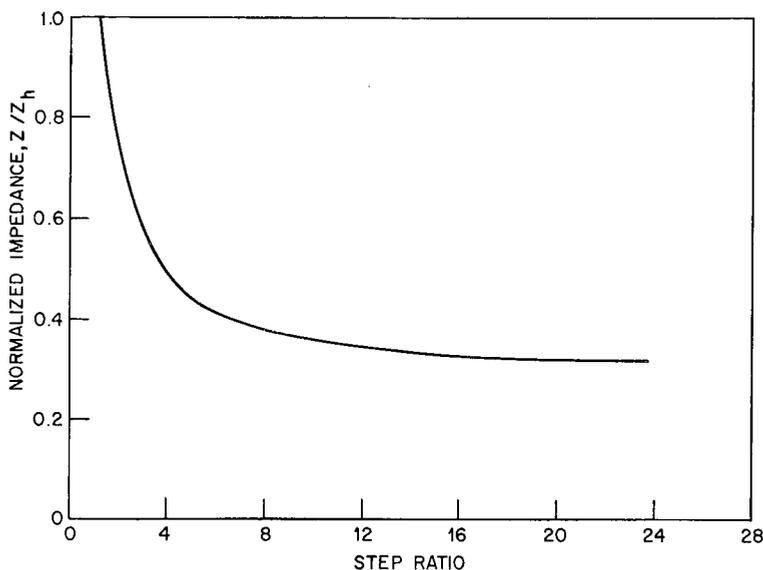


Fig. 13 — Junction model transmission line impedance

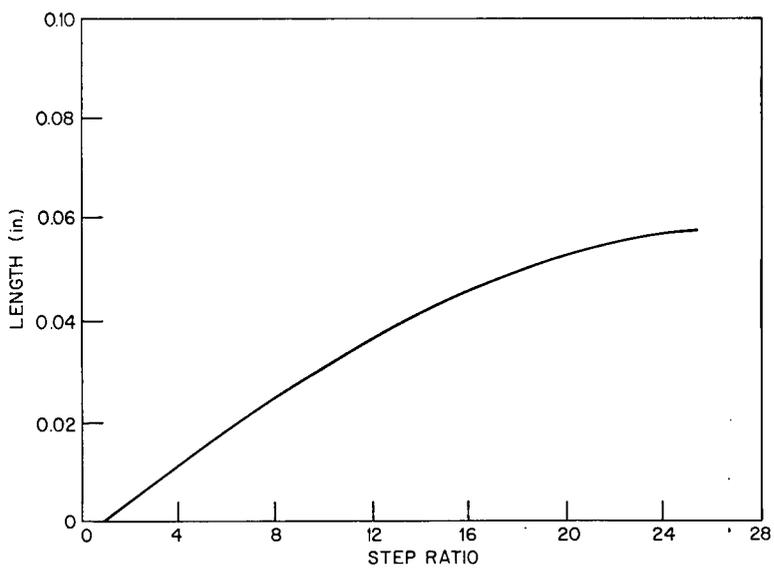


Fig. 14 — Junction model transmission line length

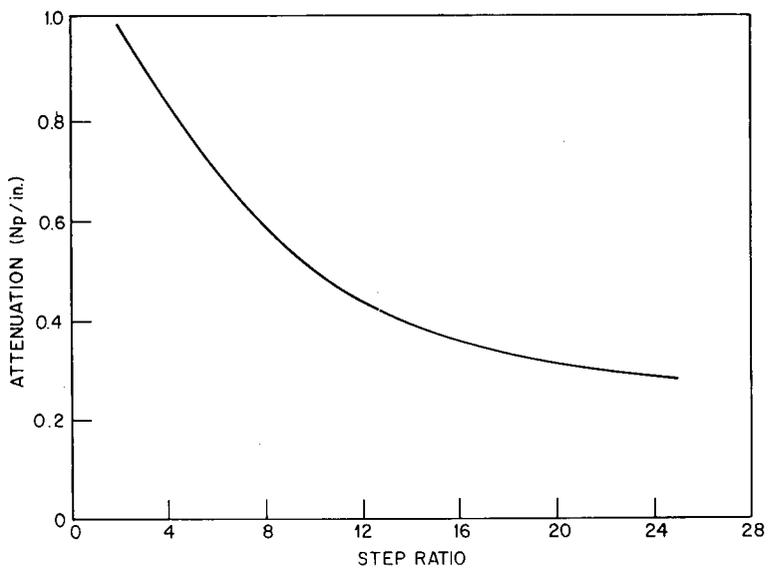


Fig. 15 — Junction model transmission line attenuation

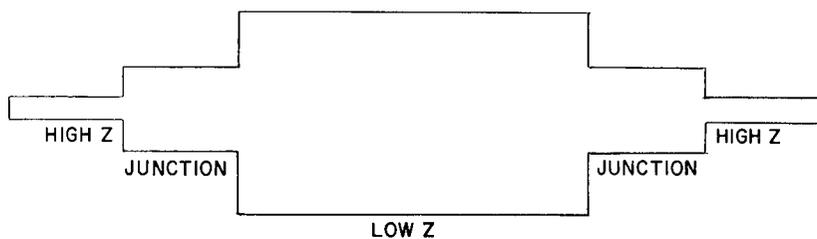


Fig. 16 — Transmission line junction model ($Z = \text{impedance}$)

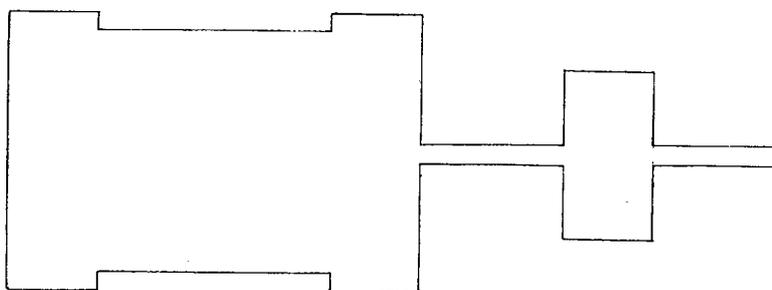


Fig. 17 — Junction model test circuit with arbitrary junctions

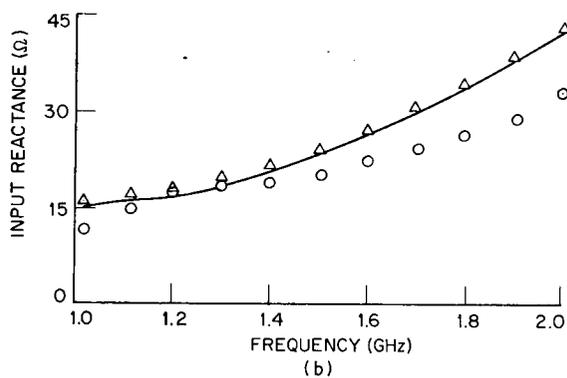
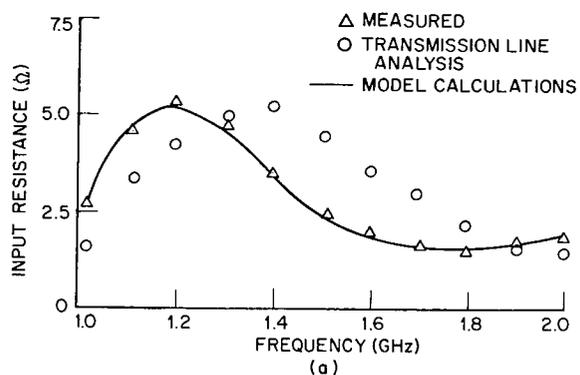


Fig. 18 — Impedance comparisons of test circuit

Matching Network Optimization

The computer-aided design of the matching networks was accomplished by an optimization procedure that minimized the function

$$\sum_{i=1}^n (R_{mi} - R_{ci})^2 + (X_{mi} - X_{ci})^2$$

for minimizing the absolute error, or by minimizing the function

$$\sum_{i=1}^n \left(\frac{R_{mi} - R_{ci}}{R_{mi}} \right)^2 + \left(\frac{X_{mi} - X_{ci}}{X_{mi}} \right)^2$$

for minimizing the percentage error. R_{mi} and X_{mi} are the measured impedances (resistance and reactance, respectively) and R_{ci} and X_{ci} are the calculated impedances. The function selected for any particular case is determined by the relative values of the real and imaginary parts of the set of measured impedances and the desired type of match.

This procedure is analogous to forming an N -dimensional surface and obtaining the minimum point of the surface in N -dimensional space. The program tests the sum of the squares of the difference between the measured and calculated impedances and exits when a set tolerance is accomplished. The fundamental limitation of any optimization routine is that the final answer is sorely dependent upon the initial values. Experience and care are required in the selection of the initial values to avoid both local minima and excess iterations.

The program is written in Fortran language, in a format usable with a timesharing terminal, and is entirely self contained. That is, it contains no library subroutines and is easily made adaptable to most timesharing systems.

Minimization is accomplished by a descending gradient technique, similar to the well-known "onion" method [44-46]. Because the spatial gradients are extremely large, it was determined that the most effective minimization technique is to optimize each variable independently. The program is written exclusively for microstrip matching networks, and therefore the only variables are line widths and line lengths. For every matching section, there are two variables in the surface function. The number of line sections is an input parameter selected by the operator. It is not necessary to have the same number of variables and measurements. The routine can be overdimensioned so that a relatively smooth fit may be obtained without an excessive number of matching sections. The optimum solution is based on a least-squares fit.

The input parameters are the maximum number of iterations, maximum tolerance desired, required impedances, measurement frequencies, number of measurements, number of line sections, substrate properties, and an estimated set of starting values for the variables.

Basically, the starting values and the number of sections required are determined from some of the well-known matching circuit properties [47].

The iteration is begun by evaluating a single-dimensional gradient and then descends along this gradient until a minimum is reached. The rate of descent depends on the gradient and decreases as the minimum is approached. The process continues for each variable until the entire set has been optimized. If the specified tolerance has not been achieved, the process is repeated. The program exits when the error is less than the set tolerance, or when the maximum number of iterations has been reached.

The program output consists of the line dimensions required for the desired set of impedances. In addition, the sum of the squares of the error is displayed so that the operator can determine the convergence. If an excessive error is obtained, the operator can select a larger number of iterations or additional line sections, or both.

The program and a block diagram are in Appendix B.

Transistor Measurement

The collector and emitter circuit impedances were measured for several transistors of each structural type under common-base class C amplifier operation. The amplifier was pulse operated with a 10- μ s pulse and a 1% duty cycle. The circuits were constructed by operating the transistor at a single frequency and empirically designing the collector and emitter circuits for maximum gain and minimum voltage standing-wave ratio (VSWR). The empirical design used indium tape overlays on 50- Ω lines to construct the matching circuits. The transistor test fixture was disassembled and the circuit impedances were measured. A listing of these results is given in Appendix C.

Amplifier Design

The Microwave Semiconductor Corp. (MSC) type 2010 transistor was selected as an appropriate unit for use in a computer-designed amplifier. A review of the data indicated that the collector circuit would be relatively easy to design but the emitter circuit would have severe limitations. An approximate equivalent circuit to represent the listed impedances, along with the work of Bode [48] and Fano [49], demonstrated that the theoretical limit on bandwidth, with a 1.1 VSWR mismatch at the collector, was on the order of 500 MHz. A similar analysis with the emitter data indicated that the same mismatch would yield only a 200-MHz bandwidth. The more significant limitation with the input circuit was observed from a plot of the emitter circuit impedances on the Smith chart. Because the reactive part became more negative with increasing frequency and because the resistive part was so small, these impedances could not be realized with distributed circuits. That is, an acceptable match did not appear possible over any significant bandwidth, a problem not occurring with the collector circuit.

During analysis of some of the measured collector and emitter circuit impedances, it was observed that the ratio of the emitter-to-collector circuit resistance varied inversely with

the collector circuit reactance. It was also felt that some reactance mismatch at the collector could be tolerated without a serious degradation of amplifier output power. Therefore, by increasing the collector circuit reactance, the real part of the input impedance was increased. This increase in input resistance resulted in a matching circuit that gave an improved match across a reasonable bandwidth.

A mismatched collector circuit was constructed, and additional measurements were made for an input-matching circuit. Table 1 lists the collector mismatch, the measured and predicted input resistance, and the measured output power. A new emitter circuit was constructed, with the computer-aided design, based on the measurements for the mismatch at the collector.

Table 1
Single-Frequency Performance of the Microwave Semiconductor Corp.
2010 Transistor With a Collector Circuit Mismatch

Frequency (GHz)	Transistor Output Impedance (Ω)	Measured Circuit Impedance (Ω)	Input Impedance (Real Part) Z_{in}		Power Output (W)
			Predicted	Measured	
1.0	$11.0 + j2.1$	—	1.05	1.44	17.0
1.1	$7.40 + j1.50$	$6.88 + j2.08$	1.45	1.31	21.0
1.2	$5.85 + j0.90$	$6.80 + j1.04$	1.47	1.32	20.0
1.3	$5.15 + j0.25$	$6.16 + j0.74$	1.38	1.42	17.5
1.4	$4.90 - j0.35$	$5.75 + j0.97$	1.37	1.54	12.5
1.5	$4.85 - j1.0$	$5.68 + j1.21$	1.48	1.80	9.5

Amplifier Performance

An emitter circuit was fabricated that would permit a mismatch VSWR of less than 2:1 over approximately a 15% band. A prediction of the amplifier performance was made based on the measured values for the emitter matching circuit. Table 2 shows a comparison of predicted and actual amplifier performance. A photograph of the final amplifier is shown in Fig. 19.

Table 2
 Calculated and Measured Amplifier Performance

Frequency (GHz)	Gain (dB)		Power Output (W)	Efficiency (%)
	Calculated	Measured		
1.05	—	5.65	9.2	44.4
1.10	8.84	8.80	19.0	54.7
1.15	—	9.30	20.0	52.9
1.20	9.10	8.17	16.4	50.4
1.25	—	5.93	9.8	41.7

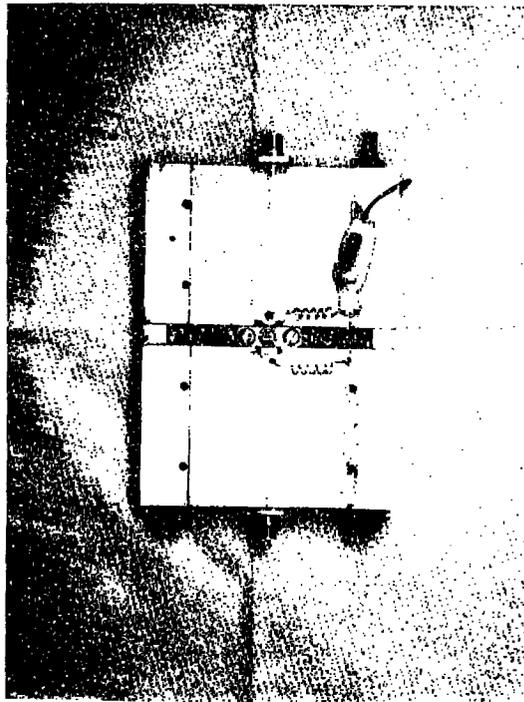


Fig. 19 — A computer-designed amplifier

DISCUSSION

Microwave power transistors appear to be an excellent replacement for thermionic devices in many applications. As the state of the art of device manufacture advances, more reliable and repeatable transistors will become available, thus requiring similar advances on the part of those associated with device application. It has been shown that considerable improvement in the performance of power amplifiers can be achieved through use of computer-aided design techniques. Several areas that require further study are discussed throughout the material that follows.

Junction Model

It was not the intent of this research to establish a rigorous theoretical derivation for the effects of step discontinuities in microstrip. It was, however, necessary to formulate a model that would adequately account for these discontinuities in the 1- to 2-GHz region. As earlier presented, the model was based on measurements for circuits with only two steps; from 50Ω to a smaller impedance (larger width) and back to 50Ω . The underlying assumption was that the steps were the same, independent of the direction of propagation, and that the equivalent circuit is symmetric at the two junctions. A set of curves for manual use and a set of approximating equations for computer application were presented. These equivalents adequately described the junction effects in the region of interest and were successfully applied during the amplifier realization.

Prior to extending the application of these models to higher frequencies it would be necessary first to verify its accuracy at those frequencies or to establish a more suitable model. Presently, transistors are available with significant output power for operation up to 4 GHz. A more extensive junction model, if necessary, could extend the computer-aided design procedure into this region.

The more significant sources of circuit measurement error, especially at higher frequencies, were the mismatch effects of the microwave launchers. These effects were almost negligible in the L-band region but would have to be included in higher frequency work. Connectors are available that are specified to have a maximum VSWR of 1.05 into the X-band region. Preliminary studies with these launchers indicate that they would be adequate for higher frequency work when properly installed.

Transistor Impedances

Several of the transistors (for example, PH 1006 and PH 1520) incorporate chip matching circuits determined by the manufacturer prior to shipment. The actual elements of the matching circuits are the bond wires, normally considered a package parasitic inductance, and metal-oxide semiconductor (MOS) capacitors. The most significant advantages of the chip matching scheme are that the effects of some of the package parasitics are minimized, and if properly designed, the harmonics are terminated at the transistor. An additional advantage may be that the matching impedances are those seen directly at the transistor chip prior to any rotation through a transmission line (the transistor lead). It may be

possible that the rotation is long enough to relieve some of the direction problems associated with the input impedance discussed earlier. Once again, the tuning associated with chip matching is accomplished by empirical methods, although the basic circuits are the same for a particular type of transistor.

The price that must be paid for chip matching is generally a reduction in the usable frequency range for the transistor because the matching circuits themselves are bandwidth limited. Transistors that incorporated chip matching were generally found to be easier to match for narrowband application but less suitable for broadband operation. This is one area in which further research is definitely needed.

Several transistors of each structural type were tested for impedance properties. Although the geometrical structures may differ, it would appear that this alone did not present any particular advantage or disadvantage. It is postulated that any effects from variations in geometric structure are completely masked by the effects of device packaging and fabrication.

In practice, it is not possible to match perfectly a set of transistor impedances across an entire band; therefore, some mismatch error must be accepted. The effects of this error can be seen in the comparison between the single-frequency performance and the broadband performance as outlined in Table 3. A fair estimate of these effects can be made using the equivalent circuit depicted in Fig. 20. For this circuit, it can be shown that an equivalent reflection coefficient can be expressed as

$$|\Gamma| = \left[1 - \frac{4R_L R_0}{(R_0 + R_L)^2 + (X_0 + X_L)^2} \right]^{1/2} \quad (3)$$

A prediction of amplifier performance with a mismatch at the collector when driven by an ideal source is shown in Table 4.

Table 3
Comparison of Single-Frequency and
Broadband Performance

Frequency (GHz)	Single-Frequency Power Output (W)	Broadband Power Output (W)
1.0	26.5	17.0
1.1	26.0	21.0
1.2	24.2	20.0
1.3	21.3	17.5
1.4	21.0	12.5
1.5	15.6	9.5

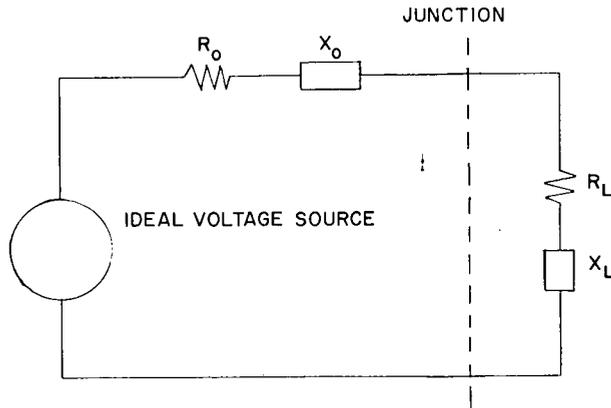


Fig. 20 — Circuit for calculating mismatch effects

Table 4
 Predicted and Measured Amplifier Performance
 When Driven by an Ideal Source

Frequency (GHz)	Gain (dB)	
	Calculated	Measured
1.0	9.58	8.87
1.1	10.15	9.73
1.2	9.65	9.11
1.3	9.10	8.36
1.4	9.10	7.34
1.5	7.41	6.25

The assumption that the transistor acts like a passive device can account for most of the errors. Other studies have shown that the output power is a function of both magnitude and phase of the reflection coefficient at the collector. The simplified equivalent circuit is a good indication of the best performance that can be expected for a collector mismatch VSWR. When the mismatch VSWR is less than 1.2, the predicted gain is within 0.5 dB of the measured gain.

The equivalent circuit is more adequate when used to predict the mismatch at the emitter. A comparison between calculated and measured values for input VSWR for the emitter circuit is given in Table 5. Again, because the transistor is an active device, some error is to be expected.

Table 5
Measured and Calculated Input VSWR
With the Designed Emitter Circuit

Frequency (GHz)	Input VSWR	
	Calculated	Measured
1.05	—	4.81
1.10	2.51	2.13
1.15	—	1.24
1.20	2.01	1.89
1.25	—	3.34
1.30	3.40	4.10

Transistor Power Amplifiers

The computer-aided design was based on a set of transistor impedances that yielded maximum amplifier power gain. Good correlation was obtained between the final calculated and measured values for both gain and input VSWR. Some error can also be expected because of the tolerances in the circuit fabrication, junction model, and measurement accuracy. The major source of error is the simplified equivalent used to predict the mismatch effects.

It should be noted that several other factors may be of significance in the design of a microwave power amplifier. The impedances used during this research were those associated with maximum output power. Factors such as efficiency, junction temperature, saturation, response flatness, and load variation effects were not considered and may lead to other sets of impedances. Matching circuits for these sets could be designed by the identical procedure used throughout this work.

Considerable variation was noted among transistors of the same type. This variation had been observed in earlier experiments in which the amplifiers had been empirically designed. If some variation between devices is inevitable, the most logical approach would be to select an optimum set of impedances for a series of transistors in which transistor interchangeability is a factor. However, achieving this interchangeability generally results in a degradation of amplifier performance.

Several empirically designed single-stage amplifiers have been combined using hybrid power combine and divide networks as shown in Fig. 21. The combine and divide networks are generally 3-dB hybrid couplers [50,51]. Signal phase becomes an important consideration when employing this combine and divide technique. As with any 90° hybrid, both magnitude and phase of the signals are underlying factors that affect the coupler performance. To combine two signals, the signals must be of equal magnitude and 90° out of phase. Any magnitude or phase deviation will result in a power loss. This leads to additional considerations

for the design of the matching networks. If the signal phase and gain of the transistors are identical, then the matching circuits for the two transistors must be of identical electrical length. However, if the transistors are not identical, that is, if there is a phase deviation between the two devices, then the matching circuits must cancel the phase difference. If this phase requirement is observed throughout the transistor impedance measurements, then the computer-aided design for each stage will result in proper phasing.

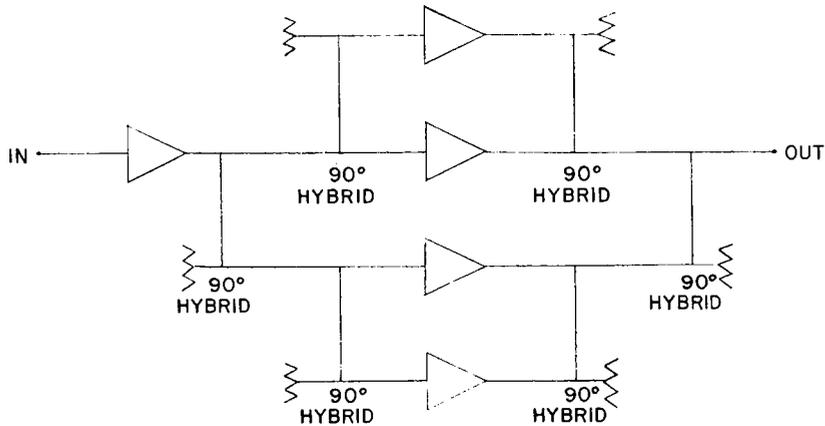


Fig. 21 — Multistage amplifier

The principal advantages of the computer-aided design can best be demonstrated by comparing amplifiers designed empirically with those designed with computer aid. The performance of an amplifier, empirically designed, incorporating an MSC 2010 transistor, is shown in Fig. 22. The amplifier, designed for maximum power output and bandwidth, is typical of the performance obtained with several similar transistors. The 7-dB gain and 10% bandwidth is generally the same as that achieved with most empirically designed amplifiers regardless of the transistor type. The input VSWR ranged from approximately 3 at the lower frequencies to 1.2 at the higher frequencies for this amplifier. Other amplifiers have been built with a 2:1 maximum VSWR.

A significant increase in both bandwidth and output power was achieved for the same transistor with the computer-aided technique as shown in Fig. 22. The input VSWR was also decreased across the 10% bandwidth. The chief limitation with bandwidth was the requirement to reduce the input VSWR. Small experimental adjustments on the computer-designed circuit resulted in a large increase in bandwidth. The input VSWR after these adjustments was as high as 3:1. The amplifier performance is shown in Fig. 23. The relative ease with which these adjustments were performed showed that the computer-designed circuit was a good starting circuit for construction of amplifiers with different performance characteristics. The time required for these minor experimental adjustments was significantly less than that required for a complete empirical design. The result was an amplifier with a much wider bandwidth and a higher output power than those developed by experimental design alone.

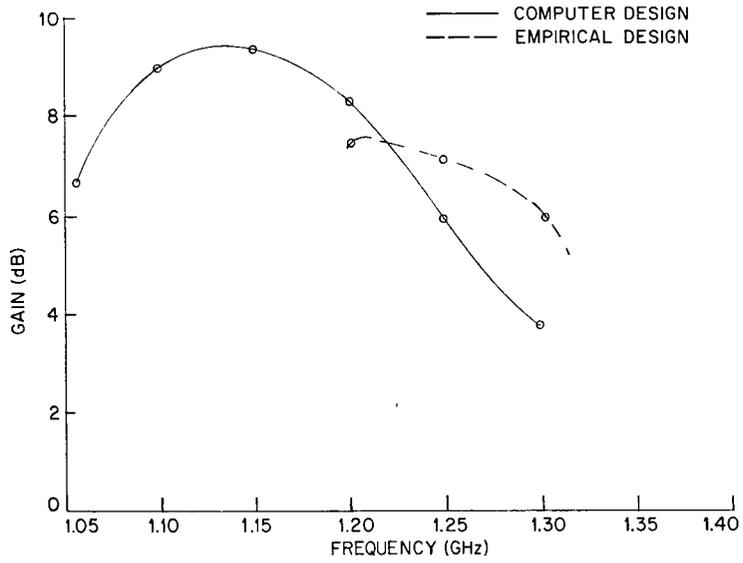


Fig. 22 - Comparison of computer-designed and empirically designed amplifiers

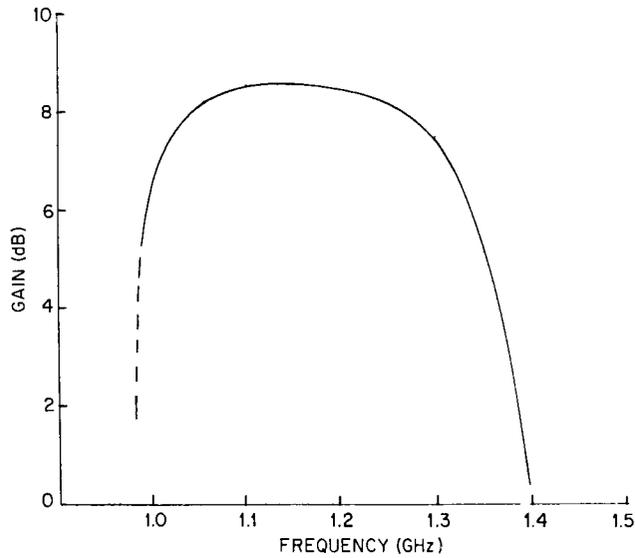


Fig. 23 - Broadband amplifier performance

Elevated collector voltages are often used when a transistor is operated as a class C, pulse-modulated amplifier. A significant increase in output power can be obtained if the duty cycle and pulse widths are small and when a sufficient heat sink is supplied. For example, the MCS 1330 transistor is specified to operate at 30 W and 28 V for continuous wave applications but can be operated at 35 V with as much as 70-W output power, providing the pulse width does not exceed 10 μ s and the duty cycle is less than 1%.

A performance comparison of the computer-designed amplifier and a similar amplifier empirically designed at Westinghouse Electric Corp. is shown in Fig. 24. The Westinghouse unit was operated with a 35-V collector supply and 5-W input. The computer-designed amplifier was operated with a 28-V collector supply and a 2.8-W input. The output power of both units is similar, but the Westinghouse unit has a lower power gain.

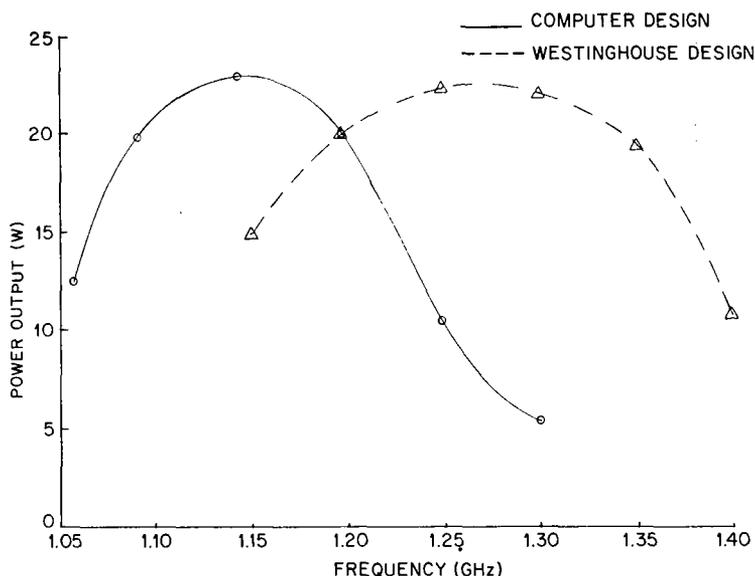


Fig. 24 — Comparison of computer-designed and Westinghouse Electric Corp. amplifier

CONCLUSIONS

Considerable performance improvement was achieved when transistor power amplifiers were designed with the aid of a computer optimization program. The required circuit impedances can be realized when accurate measurements are made and when provisions are made for the effects of the step discontinuities in microstrip circuits.

If the matching networks are accurately fabricated, and when all the measurements are precisely made, the need for tuning after fabrication becomes unnecessary. The need for design iterations is also eliminated, which saves both manufacturing time and material costs because as many as 10 or 12 iterations are generally required. The reason for the large number of iterations is the lack of repeatability between circuits with conducting tape overlays and those with chemically etched gold circuits.

It has also been demonstrated that the selection of a transistor for a particular application should include an analysis of the required circuit impedances because these impedances may lead to limitations on the amplifier performance. Although the realization of matching circuits is not the only consideration, it is one of the more important ones.

Several other solid-state devices, such as IMPATT and Gunn diodes, require matching circuits to obtain optimum performance. These matching circuits are generally experimentally designed for a particular device. Much of the work that has been presented here would find similar application for these other devices.

The most obvious extension of this research is the application of this design procedure at higher frequencies. This extension should include an analysis of step discontinuities in microstrip circuits. Perhaps a theoretical study of these discontinuities would lead to a junction model that would adequately describe the junction at all frequencies. Such a model would find application in many other areas in which microstrip circuits are used.

The chip matching technique that is currently used by some of the transistor manufacturers also requires further study. The measurements of the transistor input impedance show that a large increase in usable bandwidth might be possible if the matching circuits were more precisely designed. Also, the size reduction that would be obtained with chip matching would be very important when amplifier weight and size are design considerations. Ideally, the matching circuits would have both $50\text{-}\Omega$ input and output impedances for the amplifier.

Another area of interest would be a study of combining techniques that might lead to octave-type bandwidths. These would require the use of octave-band 3-dB couplers and a series of filters for subband amplification. A possible divide and combine technique is shown in Fig. 25.

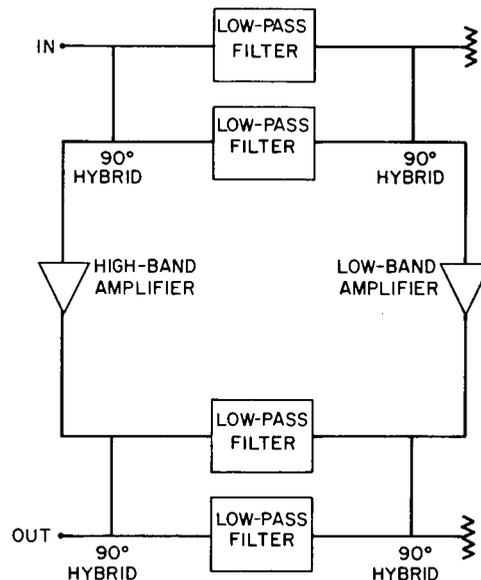


Fig. 25 — Circuit diagram for a broadband technique

ACKNOWLEDGEMENTS

The authors would like to express their appreciation to P. Silvester, McGill University, Montreal, Quebec, Canada; D. Leighton of Westinghouse Electric Corp., Baltimore, Md.; L. Whicker, Code 5250; and L. Young, Code 5203, Naval Research Laboratory, for their assistance and helpful suggestions. They would also like to express their appreciation to Mr. Paris Coleman, Code 5250, for his help with much of the computer programming.

REFERENCES

1. ———, *Microwaves* 6, No. 8, 56 (1967).
2. H. Sobol and F. Sterzer, *IEEE Spectrum* 9, No. 4, 20 (1972).
3. H.F. Cooke, *Proc. IEEE* 59, No. 8, 1163 (1971).
4. H. Sobol, *Proc. IEEE* 59, No. 8, 1200 (1971).
5. W.E. Poole and D. Renkowitz, *Microwave J.* 15, No. 10, 23 (1972).
6. ———, *Microwave J.* 5, No. 16, 12 (1972).
7. P.C. Parekh and J. Steenbergen, *Microwaves* 11, No. 8, 40 (1972).
8. J. Johnson and T. Moutoux, *Microwaves* 12, No. 18, 46 (1973).
9. ———, *Microwaves* 12, No. 7, 62 (1973).
10. H.A. Watson, *Microwave Semiconductor Devices and Their Circuit Applications*, Chap. 17, McGraw-Hill, New York 1969.
11. ———, *Microwaves* 11, No. 3, 60 (1972).
12. M. Flahie, *Microwaves* 11, No. 7, 36 (1972).
13. D.S. Jacobson, *Microwaves* 11, No. 7, 46 (1972).
14. V. Garboushian, *Microwaves* 11, No. 7, 54 (1972).
15. J. Millman and H. Taub, *Pulse, Digital, and Switching Waveforms*, McGraw-Hill, New York, 1965, p. 7.
16. P.E. Gray and C.L. Searle, *Electronic Principles, Physics, Models, and Circuits*, Chap. 21, John Wiley & Sons, Inc. New York, 1969.
17. H.K. Gummel and H.C. Poon, *Bell Syst. Tech. J.* 49, No. 5, 827 (1970).
18. K. Hartmann, W. Kotyczka, and M.J.O. Strutt, *IEEE Trans. MTT-20*, No. 2, 120 (1972).
19. K. Hartmann, W. Kotyczka, and M.J.O. Strutt, *Electron Lett.* 7, No. 18, 510 (1971).
20. M.H. White, "Characterization of Microwave Transistors," Ph.D. Dissertation, Ohio State University, 1969.

21. K. Kurokawa, Bell Syst. Tech. J. 44, No. 8, 1675 (1965).
22. J. Lange and W.N. Carr, IEEE J. Solid-State Circuits SC-7, No. 1, 71 (1972).
23. J. Lange, "An Application of Device Modeling to Microwave Power Transistors," Ph.D. Dissertation, Southern Methodist University, 1971.
24. R.E. Neidert and H. Heddings, NRL Report 7682, "1200- to 1300-MHz 100-Watt Transistor Power Amplifier," 1973.
25. E.T. Ebersol, Microwaves 11, No. 12, 9 (1972).
26. A. Presser, Microwaves 7, No. 8, 53 (1968).
27. G. Essayag and B. Sauve, Electron. Lett. 8, No. 23, 564 (1972).
28. A. Farrar and A.T. Adams, IEEE Trans. MTT-19, (1971).
29. W.J. Chudobiak, O.P. Jain, and V. Makios, IEEE Trans. MTT-19, No. 9, 783 (1971).
30. M.V. Schneider, Bell Syst. Tech. J. 48, No. 7, 2325 (1969).
31. A.F. Hinte, G.V. Kopcsay, and J.J. Taub, Microwaves 10, No. 12, 46 (1971).
32. C.P. Hartwig, D. Masse, and R.A. Pucel, "Frequency Dependent Behavior of Microstrip," presented at the IEEE G-MTT Int. Microwave Symposium in Detroit, Mich., 1968; *Digest of Technical Papers*, pp. 110-116.
33. G.I. Zysman and D. Varon, "Wave Propagation in Microstrip Transmission Lines," presented at the IEEE G-MTT Int. Microwave Symposium in Dallas, Tex., 1969; *Digest of Technical Papers*, pp. 3-9.
34. M.V. Schneider, Bell Syst. Tech. J. 48, No. 5, 1421 1969.
35. B.P. Hand, Hewlett-Packard J. 21, No. 6, 16 (1970).
36. G.T. O'Reilly and R.E. Neidert, "Computer Program for Increasing the Accuracy of Impedance Measurements Performed with a Hewlett Packard Manual Network Analyzer," NRL Memorandum Report 2676, 1973.
37. P.D. Patel, IEEE Trans. MTT-19, No. 11, 862 (1971).
38. A. Gopinath and P. Silvester, IEEE Trans. MTT-21, No. 6, 380 (1973).
39. P. Benedek and P. Silvester, IEEE Trans. MTT-20, No. 11, 729 (1972).
40. P. Benedek and P. Silvester, IEEE Trans. MTT-20, No. 8, 504 (1972).
41. P. Silvester and P. Benedek, IEEE Trans. MTT-20, No. 8, 511 (1972).
42. R. Horton, IEEE Trans. MTT-21, No. 8, 562. (1973).
43. A.A. Oliner, IRE Trans. MTT-3, No. 2, 134 (1955).
44. F.S. Acton, *Numerical Methods That Work*, Harper & Row, New York, 1970, p. 448.

45. K.S. Kunz, *Numerical Analysis*, McGraw-Hill, Co. New York, 1957, p. 244.
46. J.B. Dennis, *Mathematical Programming and Electrical Networks*, John Wiley & Sons, Inc., and the Technology Press of MIT, New York and Cambridge, 1959, p. 108.
47. G.L. Matthaei, L. Young, E.M.T. Jones, *Microwave Filters, Impedance-Matching Networks, and Coupling Structures*, McGraw-Hill, New York, 1964.
48. H.W. Bode, *Network Analysis and Feedback Amplifier Design*, Van Nostrand, Princeton, N.J., 1945, p. 360.
49. R.M. Fano, *J. Franklin Inst.* 249, No. 1, 57 (1950).
50. J. Lange, "Interdigitated Strip-Line Quadrature Hybrid," paper presented at the G-MTT Int. Microwave Symposium, 1969; *Digest of Technical Papers*, pp. 10-13.
51. L. Young, *Advances in Microwaves*, Vol. 1, Academic Press, New York, 1966, p. 115.

Appendix A

PROGRAM NACORZ

The computer program that follows (written in Fortran) is the one used for improving the accuracy of the Hewlett-Packard manual network analyzer.

O'REILLY, NEIDERT, AND HEDDINGS

```

00100 PROGRAM NACORZ (INPUT,OUTPUT)
00110 COMPLEX CJ,Y,ZL,E00,E01,E11,RM,S11,ZL2
00120 COMPLEX XY,AM,PI,BL,EL,YM
00130 COMMON EL,AM
00140 DIMENSION P(15,15),C(15,15),X(15),DB(3),ANG(3),RANG(3)
00150 DIMENSION DBL(3),GAM2(3),EL(6),GAMA(3),XX(3),Y(3),XY(3)
00160 DIMENSION AM(6),BL(3)
00170 EXTERNAL XCEKFN
00180 PRINT 40
00190 40FORMAT(*ENTER NO. OF FREQ.*,†)
00200 READ,KF
00210 PRINT 50
00220 50FORMAT(*ENTER NO.OF MEAS. AT EACH FREQ.*,†)
00230 READ,KM
00240 CJ=(0.,1.)
00250 DO 30 II=1,KF
00260 PRINT 112
00270 112FORMAT(*FREQ =*,†)
00280 READ,FREQ
00290 PRINT 120
00300 120 FORMAT(*ENTER OFFSET SHORT DATA*)
00310 CALL NETCOR(FREQ,E00,E01,E11)
00320 PRINT 121
00330 121 FORMAT(*ENTER MEASURED DATA*)
00340 DO 20 IJ=1,KM
00350 PRINT 110
00360 110 FORMAT(*S11 MAG=*,†)
00370 READ,RMAG1
00380 PRINT 111
00390 111FORMAT(*S11 ANG=*,†)
00400 READ,ANG1
00410 RANG1=ANG1/57.296
00420 DR1=-RMAG1/10.
00430 GAM1M=10.**DR1
00440 GAM2M=1.0/GAM1M
00450 GAMA1=SQRT(GAM2M)
00460 XM=GAMA1*COS(RANG1)
00470 YM=CJ*GAMA1*SIN(RANG1)
00480 RM=XM+YM
00490 S11=(E00-RM)/(E11*E00-E01-RM*E11)
00500 ZL=50.*(1.+S11)/(1.-S11)
00510 ALAM1=30./(FREQ*1.41421*2.54)
00520 A1=6.283186*.314/ALAM1
00530 B1=TAN(-A1)
00540 ZL2=50.*(ZL+CJ*50.*B1)/(50.+CJ*ZL*B1)
00550 PRINT1000,ZL2
00560 1000FORMAT(*Z=*,3X,2F10.5)
00570 PRINT60
00580 60FORMAT(/,*NEXT MEAS.*)

```

```

00590 20 CONTINUE
00600 PRINT70
00610 70 FORMAT(/,*NEXT FREQ.*)
00620 30 CONTINUE
00630 END
00640 SUBROUTINE NETCOR (FREQ,E00,E01,E11)
00650 DIMENSION P(15,15),C(15,15),X(15)
00660 DIMENSION DB(3),ANG(3),RANG(3),DBL(3),GAM2(3),EL(6)
00670 DIMENSION GAMA(3),XX(3),Y(3),XY(3),AM(6),BL(3)
00680 COMMON EL,AM
00690 COMPLEX CJ,XY,AM,PI,BL,EL,E00,E01,E11
00700 DO 10 I=1,3
00710 PRINT 11,I
00720 11 FORMAT(*MAG S11(*,I2,*)=*,†)
00730 READ,DB(I)
00740 PRINT 12,I
00750 12 FORMAT(*ANG S11(*,I2,*)=*,†)
00760 READ,ANG(I)
00770 10 CONTINUE
00780 CJ=(0.,1.)
00790 DO 14 J=1,3
00800 RANG(J)=ANG(J)/57.29577951
00810 DBL(J)=DB(J)/10.
00820 GAM2(J)=10.*DBL(J)
00830 GAMA(J)=SQRT(GAM2(J))
00840 XX(J)=GAMA(J)*COS(RANG(J))
00850 Y(J)=GAMA(J)*SIN(RANG(J))
00860 XY(J)=XX(J)+CJ*Y(J)
00870 14 CONTINUE
00880 K=-1
00890 DO 15 JJ=1,3
00900 K=K+2
00910 AM(K)=XY(JJ)
00920 AM(K+1)=XY(JJ)
00930 15CONTINUE
00940 X(1)=0.
00950 X(2)=0.
00960 X(3)=1.
00970 X(4)=0.
00980 X(5)=0.
00990 X(6)=0.
01000 PI=4.*CJ*3.141593*FREQ/30.
01010 BL(1)=-PI*2.5
01020 BL(2)=-PI*1.25
01030 BL(3)=-PI*.7352941178
01040 EL(1)=CEXP(BL(1))
01050 EL(2)=EL(1)
01060 EL(3)=CEXP(BL(2))
01070 EL(4)=EL(3)

```

```
01080 EL(5)=CEXP(BL(3))
01090 EL(6)=EL(5)
01100 CALL XCNLSB (6,15,60,.0001,IERR,X,P,C,XCEKFN)
01110 PRINT 16,IERR
01120 16FORMAT(*IERR=*,I2)
01130 E00=X(1)+CJ*X(2)
01140 E01=X(3)+CJ*X(4)
01150 E11=X(5)+CJ*X(6)
01160 RETURN
01170 END
01180 SUBROUTINE XCEKFN(X,F,K)
01190 DIMENSION X(6),EL(6),AM(6)
01200 COMPLEX CJ,E00,E01,E11,FF,AM,EL
01210 COMMON EL,AM
01220 CJ=(0.,1.)
01230 E00=X(1)+CJ*X(2)
01240 E01=X(3)+CJ*X(4)
01250 E11=X(5)+CJ*X(6)
01260 I=K
01270 FF=E00-EL(I)*E01/(1.+EL(I)*E11)-AM(I)
01280 A=K
01290 B=A/2.
01300 KK=K/2
01310 C=B-KK
01320 IF(C.GT.0.)GO TO 100
01330 F=AIMAG(FF)
01340 GO TO 110
01350 100F=REAL(FF)
01360 GO TO 110
01370 110RETURN
01380 END
```

Appendix B

PROGRAM FOR OPTIMIZING
IMPEDANCE-MATCHING CIRCUITS

The computer program used for optimizing the impedance-matching circuits is listed on the following pages. The program is written in Fortran computer language. A flow-chart is shown in Fig. B1.

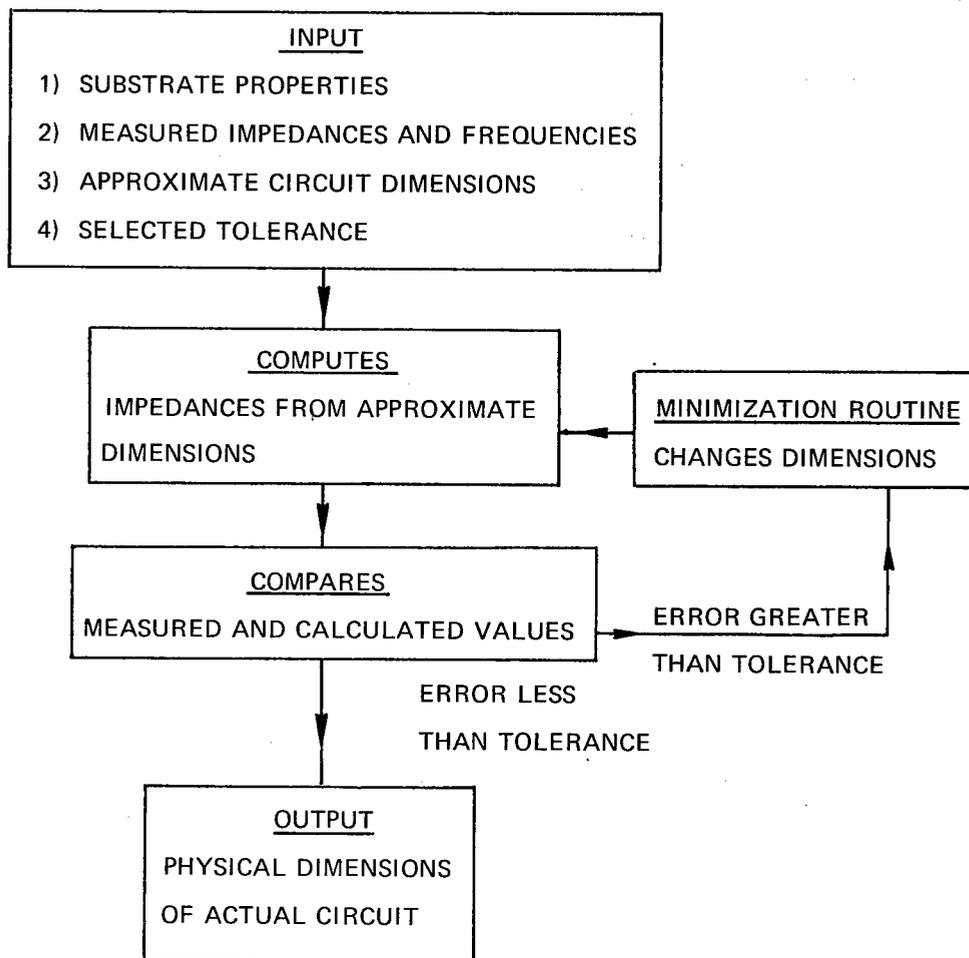


Fig. B1 — A computer program to optimize impedance-matching circuits

```

00100 PROGRAM OPTIM (INPUT,OUTPUT)
00110 DIMENSION X(30),WW(15),PLL(15),ZR(15),ZX(15),FR(15),F(15)
00120 COMMON ZX,ZR,FR,EPR,HI,KB,KE,KA,I4,CFS0,X
00130 COMMON KAA,KBB,KEE
00140*INPUTS NO. OF MEASURED Z
00150 PRINT 900
00160 900 FORMAT(*NO. OF MEASURED Z=*,†)
00170 READ,KA
00180 KB=KA+KA-1
00190 KE=KA+KA
00200 PRINT 910
00210 910FORMAT( )
00220 PRINT 901
00230 901FORMAT(*NO. OF LINE SECTIONS=*,†)
00240 READ,KAA
00250 KBB=KAA+KAA-1
00260 KEE=KAA+KAA
00270 PRINT 910
00280 1001FORMAT(F6.4)
00290*INPUTS MEASURED Z
00300 DO 1010 IA=1,KA
00310 PRINT 1020,IA
00320 1020FORMAT(*ZR(*,I2,*)=*,†)
00330 READ 1030,ZR(IA)
00340 1030 FORMAT(F6.3)
00350 PRINT 1040,IA
00360 1040 FORMAT(*ZX(*,I2,*)=*,†)
00370 READ 1030,ZX(IA)
00380 1010CONTINUE
00390 PRINT910
00400*INPUTS MEASURED FREQUENCY
00410 DO 1050 IB=1,KA
00420 PRINT 1060,IB
00430 1060FORMAT(*FREQ(*,I2,*)(GHZ.)=*,†)
00440 READ 1030,FR(IB)
00450 1050 CONTINUE
00460 PRINT910
00470*INPUTS ESTIMATED WIDTHS AND LENGTHS
00480 ID=-1
00490 DO 1070 IC=1,KAA
00500 ID=ID+2
00510 PRINT1080,IC
00520 1080FORMAT(*EST. W(*,I2,*)(IN.)=*,†)
00530 READ 1030,X(IC)
00540 PRINT 1090,IC
00550 1090FORMAT(*EST.L(*,I2,*)(IN.)=*,†)
00560 READ1030,PLI
00570 X(ID+1)=PLI

```

```

00580 1070 CONTINUE
00590 PRINT910
00600*INPUTS RELATIVE DIELECTRIC CONSTANT
00610 PRINT 1100
00620 1100FORMAT(*REL. DIEL. CONSTANT=*,†)
00630 READ 1030,EPR
00640 PRINT910
00650*INPUTS DIELECTRIC HEIGHT
00660 PRINT 1101
00670 1101FORMAT(*DIELECTRIC HEIGHT=*,†)
00680 READ1001,HI
00690 PRINT 910
00700 PRINT1111
00710 1111FORMAT(*ENTER MAX ITER*,†)
00720 READ,MAX
00730*CALCULATIONS
00740 DO 1 I2=1,MAX
00750 DO 2 I3=1,KEE
00760 I4=I3
00770 XS=X(I3)
00780 CALL ITER(XS)
00790 X(I3)=XS
00800 IF(CFSQ .LT. .1)GO TO 3
00810 2CONTINUE
00820 1CONTINUE
00830 GO TO 3
00840 3PRINT910
00850*PRINTS CALCULATED WIDTHS AND LENGTHS
00860 IG=0
00870 DO 1120 IE=1,KBB,2
00880 IG=IG+1
00890 PRINT 1130,IG,X(IE)
00900 1130FORMAT (*W(*,I2,*)=*,F6.3,*IN.*)
00910 XX=X(IE+1)
00920 PRINT1140,IG,XX
00930 1140 FORMAT(*L(*,I2,*)=*,F6.3,*IN.*)
00940 PRINT910
00950 1120 CONTINUE
00960 PRINT1180,CFSQ
00970 1180FORMAT(*SUM ERROR SQ.=*,F10.6)
00980 END
00990 SUBROUTINE CALCF (FSQ)
01000 DIMENSION X(30),WW(15),PLL(15),ZR(15),ZX(15),FR(15),F(15)
01010 COMMON ZX,ZR,FR,EPR,HI,KB,KE,KA,I4,CFSQ,X
01020 COMMON KAA,KBB,KEE
01030 COMPLEX FF,TA,TB,TC,TD,TAA,TBB,TCC,TDD
01040 COMPLEX AA,BB,CC,DD
01050 PHI=3.1415927

```

O'REILLY, NEIDERT, AND HEDDINGS

```

01060 DO 700 K=1,KB,2
01070 KD=(K+1)/2
01080 FREQ=FR(KD)
01090 J=0
01100 DO 10 I=1,KBB,2
01110 J=J+1
01120 WW(J)=X(I)
01130 PLL(J)=X(I+1)
01140 10 CONTINUE
01150 TA=(1.0,0.)
01160 TB=(0.,0.)
01170 TC=(0.,0.)
01180 TD=(1.0,0.)
01190 DO 20 JJ=1,CAA
01200 W=WW(JJ)
01210 PL=PLL(JJ)
01220 CALL TLABCD(W,HI,PHI,PL,FREQ,EPR,AA,BB,CC,DD)
01230 TAA=TA*AA+TB*CC
01240 TBB=TA*BB+TB*DD
01250 TCC =TC*AA+TD*CC
01260 TDD=TC*BB+TD*DD
01270 TA=TAA
01280 TB=TBB
01290 TC=TCC
01300 TD=TDD
01310 IF(JJ .EQ. CAA)GO TO 20
01320 STEP=WW(JJ)/WW(JJ+1)
01330 IF (STEP .GT. 1.0)GO TO 30
01340 STEP=1./STEP
01350 WH=WW(JJ)
01360 GO TO 40
01370 30WH=WW(JJ+1)
01380 GO TO 40
01390 40WBAR=.1479*STEP+.8511
01400 WDEL=ABS(WW(JJ)-WW(JJ+1))
01410 W=WH+WDEL/WBAR
01420 CALL ZZERO(W,HI,PHI,EPR,ZO)
01430 CALL LAM(W,HI,EPR,FREQ,ALAMD)
01440 IF(STEP .GT.10.)GO TO 42
01450 PL=.00319*STEP+.00319
01460 AL=-.056*STEP+1.056
01470 GO TO 43
01480 42PL=.002*STEP+.0087
01490 AL=-.0153*STEP+.649
01500 GO TO 43
01510 43EL=2.*3.14159265*PL/ALAMD
01520 CALL DLABCD(ZO,AL,PL,EL,AA,BB,CC,DD)
01530 TAA=TA*AA+TB*CC
01540 TBB=TA*BB+TB*DD
01550 TCC=TC*AA+TD*CC

```

```

01560 TDD=TC*BB+TD*DD
01570 TA=TAA
01580 TB=TBB
01590 TC=TCC
01600 TD=TDD
01620 20 CONTINUE
01630 FF=(50.*TA+TB)/(50.*TC+TD)
01640 F(K)=REAL(FF)-ZR(KD)
01650 F(K+1)=AIMAG(FF)-ZX(KD)
01660 700CONTINUE
01670 V=0.
01680 DO 101 LA=1,KE
01690 V=V+F(LA)*F(LA)
01700 101 CONTINUE
01710 FSQ=V
01720 RETURN
01730 END
01740 SUBROUTINE TLABCD(W,HI,PHI,PL,FREQ,EPR,AA,BB,CC,DD)
01750 COMPLEX CJ,AA,BB,CC,DD
01760 CJ=(0.,1.)
01770 CALL ZZERO (W,HI,PHI,EPR,ZO)
01780 CALL LAM(W,HI,EPR,FREQ,ALAMD)
01790 EL=2.*PHI*PL/ALAMD
01800 CJ=(0.,1.)
01810 AA=COS(EL)
01820 BB=CJ*ZO*SIN(EL)
01830 CC=CJ*SIN(EL)/ZO
01840 DD=COS(EL)
01850 RETURN
01860 END
01870 SUBROUTINE ZZERO (W,HI,PHI,EPR,ZO)
01880 RATIO=W/HI
01890 SQ=(1.+10.*HI/W)**(.5)
01900 EPEF=(EPR+1.)/2.+(EPR-1.)/(2.*SQ)
01910 SREPE=SQRT(EPEF)
01920 IF (RATIO .LE.1.0)GO TO 101
01930 ZI=W/HI+2.42-.44*HI/W+(1.-HI/W)**6.
01940 ZO=120.*PHI/(ZI*SREPE)
01950 GO TO 201
01960 101 ZO=60.*ALOG(8.*HI/W+W/(4.*HI))/SREPE
01970 GO TO 201
01980 201 RETURN
01990 END
02000 SUBROUTINE LAM(W,HI,EPR,FREQ,ALAMD)
02010 SQ=(1.+10.*HI/W)**(.5)
02020 EPEF=(EPR+1.)/2.+(EPR-1.)/(2.*SQ)
02030 SREPE=SQRT(EPEF)
02040 ALAMD=30./(FREQ*SREPE*2.54)
02050 RETURN
02060 END

```

O'REILLY, NEIDERT, AND HEDDINGS

```

02070 SUBROUTINE XCCOMG (XS,G)
02080 DIMENSION X(30),WW(15),PLL(15),ZR(15),ZX(15),FR(15),F(15)
02090 COMMON ZX,ZR,FR,EPR,HI,KB,KE,KA,I4,CFSQ,X
02100 COMMON KAA,KBB,KEE
02110 COMPLEX FF,TA,TB,TC,TD,TAA,TBB,TCC,TDD
02120 COMPLEX AA,BB,CC,DD
02130 X(I4)=XS
02140 CX=X(I4)
02150 HX=X(I4)/500.
02160 X(I4)=X(I4)-HX
02170 CALL CALCF (FSQ)
02180 FS1=FSQ
02190 X(I4)=X(I4)+2.*HX
02200 CALL CALCF (FSQ)
02210 FS2=FSQ
02220 G=(FS2-FS1)/(2.*HX)
02230 X(I4)=CX
02240 RETURN
02250 END
02260 SUBROUTINE XCCOMF(XS,FSQ)
02270 DIMENSION X(30),WW(15),PLL(15),ZR(15),ZX(15),FR(15),F(15)
02280 COMMON ZX,ZR,FR,EPR,HI,KB,KE,KA,I4,CFSQ,X
02290 COMMON KAA,KBB,KEE
02300 X(I4)=XS
02310 CALL CALCF (FSQ)
02320 CFSQ=FSQ
02330 RETURN
02340 END
02350 SUBROUTINE ITER (XS)
02360 ADX=.1*XS
02370 GM3=0.
02380 CALL XCCOMG (XS,G)
02390 GM=ABS(G)
02400 IF(GM .GT. 1000.)GO TO 22
02410 IF(GM .GT. 100.)GO TO 21
02420 IF(GM .LE. 100.)GO TO 20
02430 20 ADX=ADX/4.
02440 GO TO 22
02450 21 ADX=ADX/2.
02460 GO TO 22
02470 22 DO 14 I=1,25
02480 CALL XCCOMF (XS,FSQ)
02490 IF (FSQ .LT. .1)GO TO 15
02500 CALL XCCOMG (XS,G)
02510 GM=ABS(G)
02520 GM2=G/GM
02530 GM4=GM3+GM2
02540 IF(GM4 .EQ.0.0)ADX=ADX/3.
02550 GM3=GM2

```

```
02560 IF (GM .LT. .01)GO TO 15
02570 IF (G .LE.0.) GO TO 11
02580 GO TO 12
02590 11DX=1.
02600 GO TO 13
02610 12DX=-1.
02620 GO TO 13
02630 13XS=XS+ADX*DX
02640 14CONTINUE
02650 GO TO 15
02660 15RETURN
02670 END
02680 SUBROUTINE DLABCD(ZO,AL,PL,EL,AA,BB,CC,DD)
02690 COMPLEX CJ,EZ,EP,EN,HSIN,HCOS,AA,BB,CC,DD
02700 CJ=(0.,1.)
02710 EZ=AL*PL+CJ*EL
02720 EP=CEXP(EZ)
02730 EN=CEXP(-EZ)
02740 HSIN=.5*(EP-EN)
02750 HCOS=.5*(EP+EN)
02760 AA=HCOS
02770 BB=ZO*HSIN
02780 CC=HSIN/ZO
02790 DD=HCOS
02800 RETURN
02810 END
```

Appendix C

MEASURED TRANSISTOR CIRCUIT IMPEDANCES

The measured transistor circuit impedances are listed on the following page. The impedances are those measured for maximum power output and minimum reflected power. All data are for transistors operated as class C amplifiers with a 10- μ s pulse and a 1% duty cycle.

Transistor Type	Test No.	Power Input (W)	Frequency (GHz)	Impedances (Ω)				
				Emitter Circuit	Collector Circuit			
PH 1006	1	0.8	1.0	5.39 - j1.24	22.09 + j0.30			
			1.1	7.69 - j31.79	10.46 + j4.72			
			1.2	20.74 - j32.88	6.52 + j5.05			
			1.3	48.59 - j4.96	4.47 + j2.71			
			1.4	36.40 - j14.66	3.28 + j0.8			
	2	0.8	1.5	10.46 - j15.23	2.22 + j1.40			
			1.1	6.54 - j27.94	10.42 + j5.59			
			1.2	24.69 - j28.80	5.17 + j5.28			
			1.3	43.49 - j14.33	3.66 + j2.92			
			1.4	30.88 - j15.45	3.26 + j1.62			
			1.5	13.73 - j16.98	2.38 + j0.17			
			PH 1510	1	2.5	1.0	2.98 - j10.67	8.43 + j11.39
						1.1	3.84 - j14.49	10.28 + j5.86
						1.2	6.50 - j23.65	10.14 + j0.75
				2	2.5	1.3	46.02 - j36.59	7.75 + j1.38
1.4	17.27 - j21.56	6.68 + j1.03						
1.5	3.88 + j7.71	4.31 + j1.28						
PH 1012	1*	2.5	1.2	7.19 - j18.56	15.07 + j2.40			
			1.3	12.67 - j0.25	20.54 + j20.03			
			1.4	23.45 - j12.02	9.34 + j5.47			
			1.5	8.32 - j7.79	5.49 + j4.61			
			1.15	4.5 - j19.95	7.1 - j1.0			
	2†	3.0	1.20	6.0 - j19.0	5.85 - j2.5			
			1.25	5.0 - j23.0	5.5 - j4.5			
			1.30	10.5 - j22.8	4.5 - j3.0			
			1.35	26.5 - j15	2.9 - j4.0			
			1.15	3.75 - j19.0	5.25 - j4.75			
			1.20	4.5 - j18.95	4.55 - j3.5			
			1.25	4.0 - j20.75	3.95 - j4.05			
MSC 2010	1	2.5	1.30	5.0 - j26.5	2.75 - j5.25			
			1.35	14.5 - j36.5	3.75 - j4.25			
			1.0	1.5 - j3.2	11.0 + j2.1			
			1.1	1.08 - j3.1	7.4 + j1.5			
			1.2	.91 + j3.4	5.85 + j0.90			
			1.3	.84 + j4.1	5.15 + j0.25			
			1.4	.84 + j5.0	4.90 - j0.35			
			1.5	.88 + j5.95	4.85 - j1.0			

*Tested with 14.5-W output.

†Tested with 23.0-W output.