

# Simulation of AADC Simplex and Multiprocessor Operation

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## ABSTRACT

Simulation of a proposed naval Advanced Avionic Digital Computer (AADC) has been underway to arrive at architectures which efficiently meet the needs of expected program workloads. Models of avionic program workloads have been derived from various sources and used to drive these simulations. These models consist of sets of nearly independent program modules which effect periodic, known demands on system resources.

Simplex and multiprocessor configurations of the AADC have been modeled, and certain features of proposed AADC executive operation have been incorporated into these models. Guided by previous simulation work, both nonpaged and paged operating systems with multiprogrammed memories have been simulated.

The simplex processor achieves the highest percentage of processor utilization and, with multiprogramming, the lowest level of program transfer overhead. The effectiveness of multiprogramming in the multiprocessor configurations does not match that experienced with the simplex processor, but this effectiveness might be boosted by compartmenting program workloads into separate families under different processing elements.

Under full processor utilization, background executive activities such as system timing account for less overhead than direct executive functions controlling program execution. Sharing of the processing element by executive and program workload thus appears an effective strategy for a simplex system. Multiprocessor demands on the executive indicate that a dedicated executive processor is reasonable for multiprocessor configurations under full workloads.

Sharing of busing resources by both data and program transfers appears to offer an acceptable cost-efficiency tradeoff in dual and triple processor operation, but a triple processor would profit more, if cost reduction is paramount, by maintaining separate busing and relinquishing possible hardware executive features for a dedicated software executive.

## PROBLEM STATUS

This is an interim report; work on this problem is continuing.

## AUTHORIZATION

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## SIMULATION OF AADC SIMPLEX AND MULTIPROCESSOR OPERATION

### INTRODUCTION

An Advanced Airborne Digital Computer (AADC) is being developed to provide a standard solution to future, growing demands of naval avionics missions (1). AADC design studies have considered various implementations of simplex and multiprocessor systems. All implementations have in common a fast-access block-oriented memory which feeds programs to small high-speed random-access task memories from which processing takes place (2). The suitability of various architectures for processing avionics program workloads is of prime concern, and work has been aimed at tailoring system design to the inherent characteristics of expected workload requirements.

Modeling and simulation of the AADC has been in progress in pursuit of optimized system designs (3,4). Simulation study to date has been aimed at gauging the effect on system overhead of various schemes for memory resource allocation. Results using models of the E-2B program workload indicate that paging and multiprogramming of AADC task memory can provide efficient system operation with modest requirements on task memory size.

Further simulation work—the subject of this report—has been directed toward evaluating computer performance under a broader range of workloads and under the influence of an executive system (5) intended for the AADC. One-, two-, and three-processor systems with selected resource allocation schemes have been included in these simulations and their performance analyzed in an effort to reveal relative effects of different operating schemes.

Workload models for these simulation studies were derived from three sources: an analysis of the E-2B program workload (6); the F-111B program manual (7); and a study by the General Electric Company of AADC future mission requirements (8). These workloads represent processor loads ranging between  $10^5$  and  $10^6$  instructions per second and tactical and nontactical environments.

The method of reducing workloads to a form suitable for AADC system simulation has been discussed in Refs. 3 and 4. Essentially, a program workload is composed of separate program modules or tasks which are processed periodically by the computer. Each task constitutes a demand on the computer system's resources (memory, processors, buses) at each task iteration. Depending on the detail of available workload program descriptions, a given task can be modeled as a chain of subprogram modules or segments, each segment requiring a specifiable amount of program storage, instruction executions, and data transfers. The resulting task models are then depicted as directed graphs much akin to flow charts for normal programs except that nodes define predetermined data on system resource demand rather than steps of algorithmic procedures.

Following the results of previous AADC simulation work, the paged architecture has been extended into these simulations. Consequently all program modules are partitioned into 256 word blocks or pages in the workload models.

Detailed descriptions of the workload models are presented in Appendix A. Summary characteristics of the workloads are shown in Table 1.

Table 1  
Gross Characteristics of the AADC Workload Models

Source of the Workload Model	Program Size (words)	Number of Program Modules	Processing Load (instructions/sec)
E-2B workload study	18,432	12	$2 \times 10^5$
F-111 program manual	8,192	11	$2 \times 10^5$
AADC future requirements study by GE	25,600	20	$1 \times 10^6$

## THE AADC SYSTEM

The salient feature of the AADC systems is a two-level memory hierarchy incorporating a fast-access block-oriented random-access memory (BORAM) and a fast random-access memory of small size (1024 to 4096 words) called a task memory (TM). Programs reside in BORAM, and, when called upon by the executive, a program module can be transferred into TM, where it is processed by the arithmetic and control unit (A&C). A third or random-access main memory (RAMM) is provided to store variable data which may be transferred to and from TM as program processing demands. Communications among these memories is via a system of buses, which may be independent or shared depending on cost effectiveness in each case.

AADC processing power is indicated by the better-than-2-million-instruction-per-second A&C used in the simplex multiprocessor configurations.

Figure 1 is the block diagram of the generalized AADC configurations. With some exceptions the AADC model used in these simulations is the same as that used in the AADC simulation with an E-2B workload (3). For convenience some of the description of the system model given in Ref. 3 will be repeated here.

The system hardware units are the following:

- BORAM—A read-only store for the entire program workload. It is accessible in blocks of 256 words.
- TM—A random access store into which program instructions and data are brought for processing.

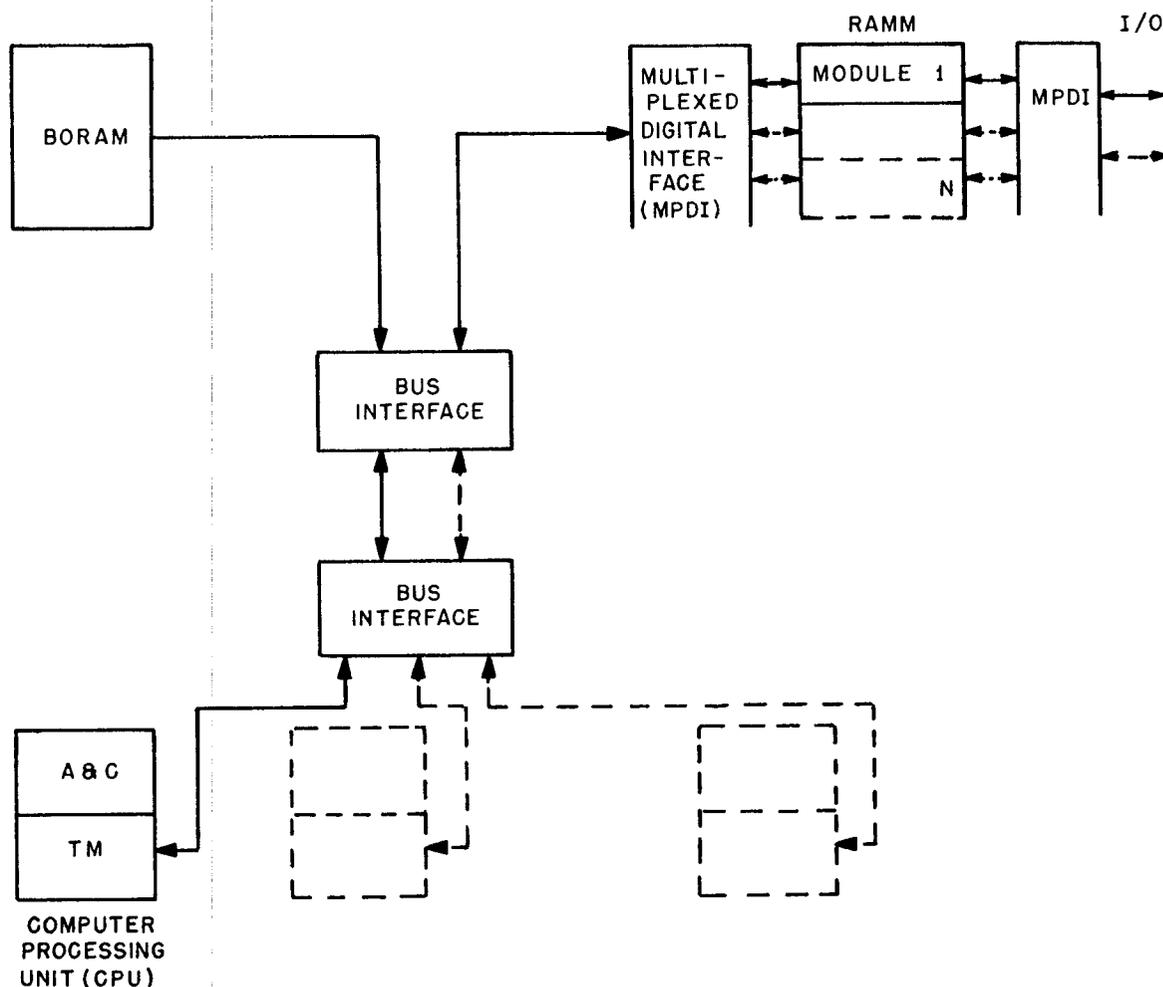


Fig. 1—AADC model

- RAMM—A random access store for program and system data. The RAMM is modular, consisting of one or more independent units.
- A&C—An arithmetic and control unit coupled to a TM, from which memory it fetches instructions and data for processing.
- Buses—Communication paths for program instructions and data among the system memories. The bus from BORAM to TM provides for transfer of program instructions into TM when needed there for processing. The bus between RAMM and TM provides data communications between these memories according to program demands. It is assumed that a multiplexed structure in this bus allows concurrent communication between one or more RAMM and TM pairs.

Transfers between RAMM and I/O flow over a multiplexed bus system allowing simultaneous communication between external devices and RAMM modules. I/O takes priority over internal communication between RAMM and TM and, as such, delays the

movement of internal data according to the relative amount of external data-transfer activity.

The system operates as follows:

- The system is multiprogrammed, with each CPU (computer processing unit) processing one task at a time.
- Tasks are scheduled by the system executive according to specified processing iteration rates and deadlines.
- In-process tasks may not be interrupted unless program and executive-routine processing must share a single CPU.
- Program processing and storage can be implemented in a paged format.
- Program pages are loaded into TM on a demand basis (when referenced and not before).
- Deallocation of space on a program page in TM is governed by a "least recently used" criterion.
- Processing takes place from TM only.
- There is no program or data exchange between CPUs in the multiprocessor system.
- Requests for data transfers between RAMM and TM are made under program control. A program making a data request ceases processing until the transfer is complete.
- Space for storage of transient data in TM is set aside as a collective area of word locations in each TM.
- The system can be run with TM containing program instructions from only the task in process (monoprogrammed TM) or from the task in process and from previously run tasks as well to the extent that space limitations and the in-process task allow (multiprogrammed TM).

#### MASTER EXECUTIVE CONTROL

System monitoring and resource allocation are handled in the AADC by the master executive control (MEC). Timing, task scheduling, communications, testing, and failure response are responsibilities of the MEC. The executive functions in AADC will be implemented by either AADC-instruction programs processing from a TM (software MEC) or by a special processor-associative memory unit capable of executing executive functions at high throughput rates (hardware MEC). a thorough description of the AADC MEC can be found in Ref. 5.

Those executive routines required for normal task processing have been explicitly incorporated into the simulation model. These routines perform the following functions:

- Interrupt recognition and processing,
- Real time clock update,
- PM Reinitialization,
- PM assignment,
- External PM enable,
- PM completion,
- Data/program transfer,
- Dedicated-channel selection,
- Page fault.

These functions are implemented in the simulated AADC MEC by separate program routines to which control passes through a system of event-generated interrupts. The duties of these routines are described briefly.

- Interrupt recognition and processing is activated by the appearance of an interrupt sent to the executive by a system unit requesting executive attention. This routine recognizes the interrupt and places the appropriate MEC routine on a list of jobs to be done by the executive. The stack of jobs is then attended to on a priority basis until all jobs have been completed or another interrupt is generated.

- The real-time-clock routine is listed for processing by an interrupt generated every  $t$  milliseconds, where  $t$  is the system-clock update interval. This routine counts down processing deadlines of active PMs and checks for the occurrence of any deadline intervals reaching zero. In the event of a zero deadline, this routine puts the PM-reinitialization routine on the executive job list.

- PM reinitialization checks those PMs which have reached the end of their allowed processing interval. If they have indeed been completed in that time, their processing deadlines are reset for the start of their next processing interval or iteration. The execution status of a PM is recorded as "ready for processing" in its new iteration interval except for PMs activated by the external interrupt rather than internal scheduling. A PM reaching its zero deadline and not having reached completion is noted as being overdue and is not reinitialized at that time. PMs reinitialized by this routine are ready for processing and, as such, the PM-assignment routine is put on the list of assigned executive tasks.

- PM assignment checks active PMs in the system for those eligible to commence processing. A PM is eligible if it has been initialized for processing, has not yet been processed within its current iteration interval, and is not awaiting the completion of other PMs which must precede it in order of execution. That eligible PM with the shortest deadline is then assigned to a CPU for processing. If no CPU is free, no PM can be assigned at that time. If a PM can be assigned to a CPU, the program-transfer routine is put on the executive job list in order to initiate the transfer of program instructions from BORAM to TM. Also, if the PM requires it, the dedicated-channel-selection routine can be put on the list to dedicate a channel between TM and I/O for use by the CPU processing that PM.

- External PM enable initializes, for processing, those PMs activated by externally generated interrupts rather than these PMs iteratively run under control of the real-time clock. As such, this routine is put on the list of executive jobs to be processed by an external PM enable interrupt.

- PM completion is put on the executive job list by an interrupt generated at the completion of a PM's processing. This routine releases the CPU which was assigned the completed PM and records that PM as having completed execution.

- The routines for data or program transfer control are put on the list depending on the condition requiring that service of the executive. A request or interrupt for a program load from BORAM to TM causes the listed routine to initiate the transfer on an available bus. The routine puts itself back on the list if the bus is not available at that time. An interrupt requesting a data transfer between RAMM and TM causes similar action. At the completion of a transfer, an interrupt is generated, causing the executive routine to release the bus for other requests.

- The dedicated-channel selection routine is responsible for seizing and releasing a bus dedicated to a channel between TM and I/O for PMs identified as requiring such a channel for processing. This routine is put on the list of executive jobs at PM assignment and completion times.

- The page fault routine is included in the simulated AADC system to account for executive interaction in paging. An interrupt generated at a page fault causes this routine to be listed. This routine serves to put the program transfer routine on the list, which then initiates the page load into TM.

Figure 2 shows the functional relationships of the executive routines to each other and the rest of the system. Appendix B contains flowcharts of the MEC routines.

## THE SYSTEM SIMULATION

The operations of the AADC system are simulated on a computer using the Simscript programming language. The behavior of the system units and executive control are encoded as a collection of discrete-time-and-event operations. The flow of activity from one event to the next is subject to the specific sequence of operations designed into the

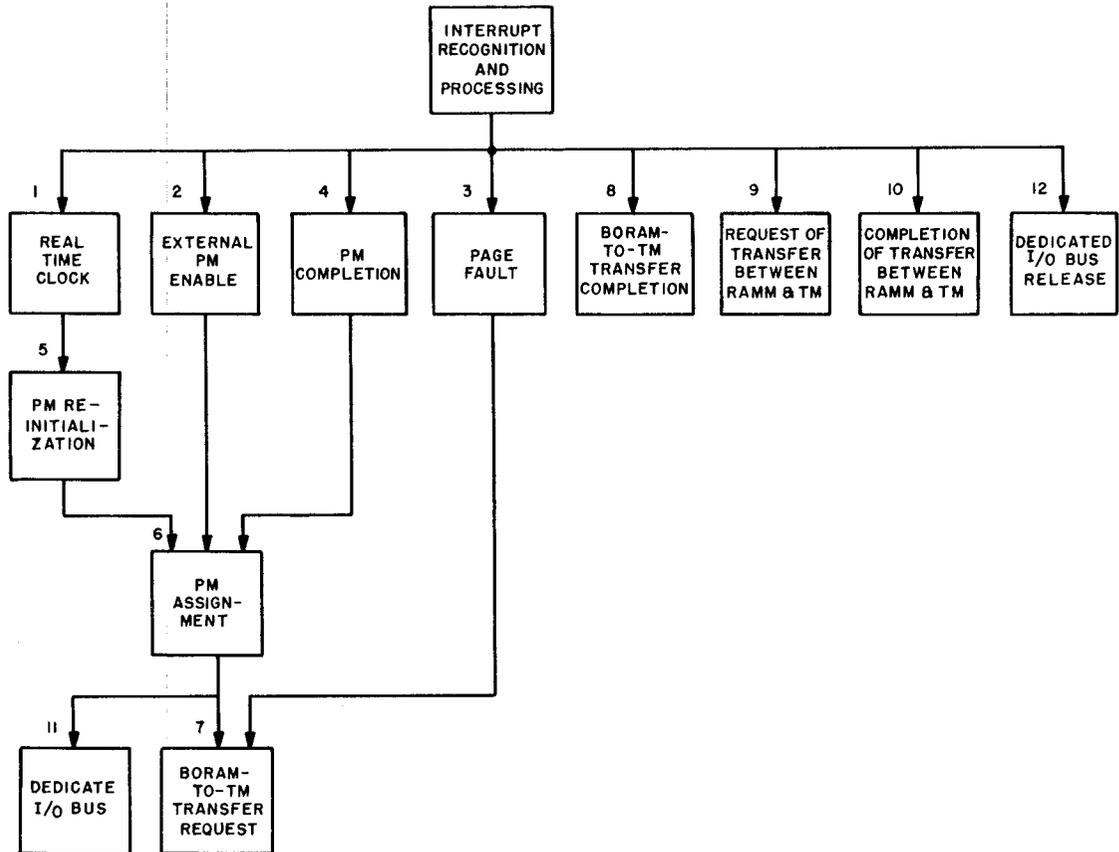


Fig. 2—Functional relationships of the simulated AADC executive routines

simulated system and the constraints of time passage decreed between the occurrence of events of processes. Figure 3 is a block diagram of the system simulation depicting the process events and the functional flow of control from one to the other. Each block represents a Simscript routine which implements required functions of system processes. The diagram shows the generation of interrupts by events in the simulated process and the passage of control, by these interrupts, to the subroutine blocks emulating the MEC interrupt-recognition-and-processing operations. Completion of the interrupt processing routine transfers control back to the start of that routine, from where control can be passed to the start MEC routine block initiating processing of the highest priority MEC routine on the list of waiting executive tasks. The functions of the executive routine in process are scheduled to be complete at a system time determined by the specified routine processing time. From here, control is passed back to the executive or on to the appropriate simulated computer operation. More detailed description of the simulation can be found in Appendix C.

## SIMULATION STRATEGY

Simulated AADC computer runs were made using the system and workload models described in this report. Information about the system throughput and overhead are of

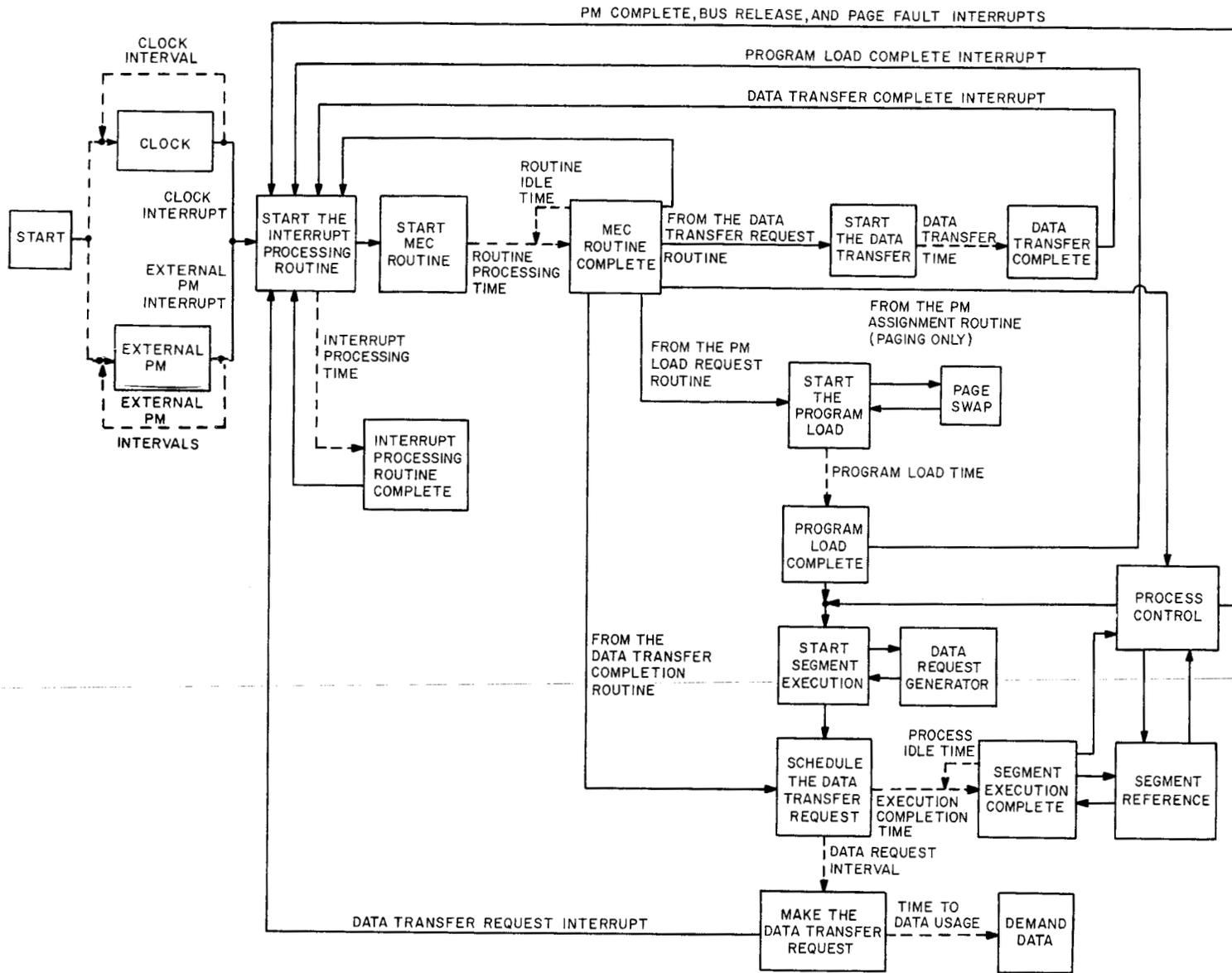


Fig. 3—AADC simulation

interest for various configurations of AADC architecture. Specifically these configurations include simplex, dual, or triple processors, executive processing by dedicated or shared processing units, and paged or nonpaged operation. AADC performance can be gauged for various configurations, by comparing the relative contributions to operating overhead made by the different components of the simulated system.

The design goal of the AADC is the processing of workload tasks via instructions contained in the stored program modules. Time consumed in executive functions, bringing program instructions into TM and moving data in and out of RAMM constitutes a resource not applied directly to this processing goal. For a given amount of instruction processing time, establishment of overheads for the various systems allows a comparative view of the efficiency of architectural variations. Accordingly, the statistics gathered by a simulation program during a run are chosen so as to establish such overheads.

Figure 4 reproduces the results printout of a sample simulation run. Most of the data shown are self-explained by the associated labeling. The results at the top in Fig. 4 provide information about program activity and how well the set of active PMs are meeting their assigned processing deadlines.

Figure 4 includes statistics relating to MEC activity. The performance of the Executive can be examined by waiting and processing-time statistics given for the various routines and interrupts. The numbers 1 through 12 labeling the interrupt and routine columns refer to MEC functions as follows:

1. Real time clock,
2. External PM enable,
3. Page fault,
4. PM completion,
5. PM reinitialization,
6. PM assignment,
7. Initiation of BORAM-to-TM loading,
8. Completion of BORAM-to-TM loading,
9. Initiation of a transfer between RAMM and TM,
10. Completion of a transfer between RAMM and TM,
11. Selection of a dedicated I/O channel,
12. Release of a dedicated I/O channel.

```

ELAPSED TIME = 10000000. USECS

TOTAL PMS ASSIGNED = 1394

PM      1   2   3   4   5   6   7   8   9  10  11
NUMBER OF ITERATIONS OF EACH PM
NUM 1250 40   5  20 49   5   5   5   5   5   5
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
NUM      0   0   0   0   0   0   0   0   0   0   0
AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC      7 249 1818 48  18 1833 1836 1838 1828 1820 1819
SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC      2 246 1809 44  15 1830 1834 1835 1827 1818 1810

      INTERRUPT DATA
INT      1   2   3   4   5   6   7   8   9  10  11  12
NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
NUM 10000 68 1331 1549 0 0 0 1331 3130 3130 0 0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - 0.1 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - 12. USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - 147773. USECS

      MEC ROUTINE DATA
PM      1   2   3   4   5   6   7   8   9  10  11  12
NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
NUM 10000 68 1331 1549 1279 2914 1331 1331 3130 3130 0 0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC      0   3   3   0   0   2   0   3   2   0   0   0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC     118 76 104 95 21 385 40 82 113 112 0 0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
MSC     400.0 4.1 6.7 23.2 65.2 329.3 21.3 21.3 50.1 50.1 0.0 0.0
AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC      0.1 1.3 0.0 0.0 0.1 0.4 0.1 0.0 0.0 0.1 0.0 0.0
LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC      7 7 7 7 7 14 7 14 7 7 0 0

      CPU DATA
CPU      1
TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
USC     1722399.
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - 1075488. USECS

TOTAL TIME MEC WAS BUSY - 111507%. USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC =
110308. USEC

NUMBER OF RORAM TO TASK MEMORY LOADS - 1331
TOTAL TIME SPENT LOADING TASK MEMORY - 50578. USECS

NUMBER OF DATA REQUESTS - 3130
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY - 253016. USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED - 409328. USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES - 82003. USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 266. USECS

NUMBER OF SEGMENT REFERENCES - 8831
NUMBER OF PAGE FAULTS - 1331
NUMBER OF PAGE JUMPS - 7477

```

Fig. 4—A sample printout giving the results of a simulated run

Figure 4 next contains results showing overall CPU and MEC utilization, data and program bus usage, and paging activity. Total CPU utilization is defined by summation of all time intervals between assignment of PMs and their completion. This encompasses, of course, the indicated instruction processing time plus nonprocessing overhead time.

When executive routines and workload programs are sharing the same processing unit, direct interruption of PM processing activity will occur, and this accumulated delay is given in the results. Delay from the initiation of data requests through the executive response time to the availability of the requested RAMM modules is also accumulated and given in the results.

Reproduced printouts from the simulation runs discussed in this report appear in Appendix D. (Figure 4 is the same as Fig. D16.)

## SIMULATION RESULTS

### Simplex Processor

The simplex processor is the fundamental AADC configuration. With a processing element capable of at least  $2 \times 10^6$  instruction executions per second, the simplex version can service any of the three workloads modeled in this study. Hence it was considered useful to run all of these workloads in the simplex model; furthermore a broader range of inputs adds more confidence to the simulation results.

The simplex AADC is planned to operate with a software executive rather than the hardware type due to cost considerations. The software executive can be run in its own dedicated processing element or as a floating executive sharing the processor with the program workload. Simulation runs were made under the following conditions:

- Paged and nonpaged operations;
- Monoprogrammed and multiprogrammed TM;
- One CPU (simplex AADC);
- One RAMM module,
- Processor speed of 2 instructions/ $\mu$ sec;
- BORAM speed of 7 words/ $\mu$ sec;
- BORAM block access time of 2  $\mu$ sec;
- RAMM speed of 3 words/ $\mu$ sec;
- Program page size of 256 words;

- TM size of 1024 to 4096 words;
- Dedicated or floating (shared) software MEC;
- Executive clock interrupt interval of 1 msec;
- MEC routine processing times as follows:
  - Interrupt processing, 7  $\mu$ sec,
  - Real time clock, 10  $\mu$ sec,
  - PM reinitialization, 51  $\mu$ sec,
  - PM assignment, 113  $\mu$ sec,
  - External PM enable, 61  $\mu$ sec,
  - PM complete, 15  $\mu$ sec,
  - Data/program transfer, 16  $\mu$ sec,
  - Dedicated channel selection, 9  $\mu$ sec,
  - Page fault, 5  $\mu$ sec.

Figure 5 displays the overall performance of various AADC configurations for the three workloads processed in 10-second simulated run times. The bars indicate the components of cumulative CPU time attributable to different system activities. The sections of each bar represent computer processes as follows.

The bottom section corresponds to the accumulated time that the A&C was busy executing instructions. On top of that is added the time used to transfer data between RAMM and TM. Next, program transfers from BORAM to TM consumed time indicated by the third section. To this point, we have accounted for processor and bus utilization.

The upper two sections represent MEC activity. They show the additional CPU times given to waiting on executive activity. The section representing dedicated-MEC activity shows that, even if executive processing does not take the CPU away from workload processing, certain CPU functions must still await the supervision of the executive. The top section (floating MEC) shows additional CPU time (over that for the dedicated MEC) consumed by the requirement that the CPU process executive as well as workload programs. Executive routines not involved in the chain of PM processing activities (such as the real time clock routine) account for this extra time.

In these runs of the simplex AADC the workload processing requirements were completely satisfied with the CPU active from about 25% to 85% of run time, depending on the workload and the system configuration. For a given workload the instruction execution



and data transfer times represent program characteristics which remain independent of the system configuration in which they are being processed. Among the different workloads represented, the time consumed, relative to instruction processing time, varies in the overhead activities. The difference in mean PM sizes, instruction counts, data requirements, and referencing patterns account for this.

PM transfer time varies with different paging configurations for a given workload. Generally this overhead was greatest in the nonpaged systems. As shown in the previous AADC simulation work (4), program transfer activity decreases as paging and paging with multiprogrammed TM are employed. The relative decrease depends on the page referencing characteristics of the workload in question and, for the GE workload in a 1024-word paged monoprogrammed TM, actually increases slightly. This happens because, in the GE workload model, PMs are not paged strategically and each new page reference causes a page fault and subsequent page load.

The extent to which executive overhead varies with system configuration depends also on the specific system activity affected. This AADC simulation assumes executive interaction in program paging and loading. Thus that portion of MEC overhead concerned with PM transfers will diminish with the decrease in paging which occurs in multiprogrammed systems. Specific figures are available in Appendix D in the results printouts.

Some additional runs were made with each workload to observe the effect on executive overhead of directly reducing the activity of specific MEC routines. The simulations were being run with an executive clock update interval of 1 millisecond. The feeling that this might be generating excessive overhead motivated runs with this clock interval lengthened several times. Relative reduction in MEC overhead did occur according to the percentage of the executive accounted for by the clock routine. Relative improvement is less with heavier workloads, because the clock interval is not affected by task processing rates. The 1-millisecond clock interval does not appear to tax executive processing.

Another executive routine, PM assignment, is the costliest, because of required processing time. The frequency with which it is listed for processing depends on the conditions for listing it. As was shown in Fig. 2, PM assignment is listed for processing by PM reinitialization, PM completion, and external PM enable. This can result in many tries at PM assignment when there is either no PM ready to run or no CPU available. Restriction of the PM assignment listing to cases of CPU availability in simulation runs is indicated (Figs. D10, D20, and D30) by "reduced PM assignment activity." Again, some slight reduction in executive overhead is noticeable.

In either of the above cases the relative reduction in executive time yields much less relative improvement in overall system efficiency, as can be noted by the relative contribution of the executive to CPU time.

More simulation results are shown in Fig. 6. These runs were made to present the appearance of relatively heavy workloads simply by restricting the length of simulation runs to that point at which all PMs in a workload had been processed at least once. Since the executive schedules PMs for execution as soon in their iteration interval as there is processing available to them, the CPU is busy almost full time up to that point. There is

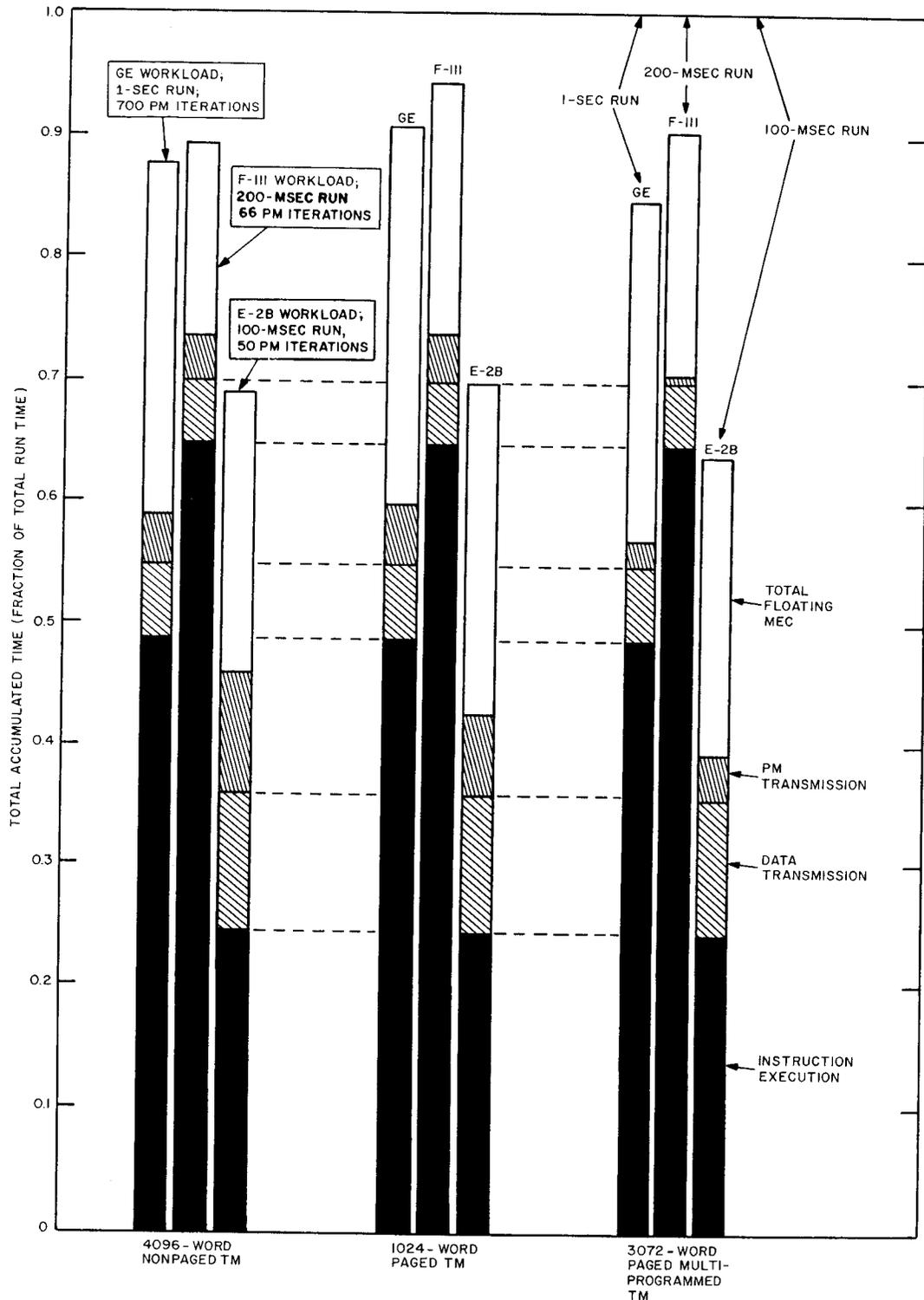


Fig. 6—Simplex processor CPU utilizations over simulated runs representing “heavy” workloads

some change in the workload statistics effected by this strategy due to greater proportion of high-iteration-rate PMs processing over the shorter interval. Executive overhead in these runs with pseudo-heavy workloads compares closely to the normal runs in Fig. 5.

### Dual Processor

The AADC is intended to be expandable in both memory and processing capability to service workloads presented by more complex future avionics missions. The simulation model is likewise expandable in this regard, and simulations were run to reveal the effect of adding more CPUs to the basic simplex system.

Normally the multiprocessor AADC would not be used unless it is warranted by the workload requirements. None of the three workloads used in the simplex runs warrant a multiprocessor. Accordingly a heavier workload was created from the GE programs by raising the iteration rates of selected PMs. By expanding a given workload in this manner, an almost arbitrarily high processing load can be presented to the AADC model.

The power of a multiprocessor computing system is more fully used by not requiring the workload to share any of that processing power with executive routines. The executive, then, runs in its own dedicated processing element similar to, but independent of, the workload processors.

It would be economical to provide only a single bus system which multiple CPUs can share for program instruction and data transfers rather than having a bus between RAMM and TM for data and a BORAM-to-TM bus for program instructions. In the simplex system, data and program transfers are naturally disjoint, but in a multiprocessor, competition for a single bus will increase system overhead as a portion of data and program transfer requests try and retry for bus service. Accordingly, simulation runs for dual and triple processors were made with both separate-bus and shared-bus configurations to allow assessment of their comparative efficiencies.

The same system parameters were used in the multiprocessor runs as in the simplex runs except, of course, for the number of processors. The workload, as mentioned, was derived by expanding the GE program model. Also incorporated is the slight improvement in executive efficiency obtained by limiting listing of the PM assignment routine to verified cases of available CPUs.

Figure 7 shows results of the dual-processor simulations. The bar graphs again show time consumed by different system activities. These times, for the multiprocessor simulations, are the totals for each activity in all CPUs in the system. For example, the instruction execution time shown is the total time in both processors of the dual processor. The overheads in the various system configurations are again shown with instruction execution times normalized (same for all systems) to allow direct comparisons.

Figure 7 displays the dual-processor utilization of CPU time with separate and shared buses for program-instruction and data transfers. Nonpaged, paged, and multiprogrammed

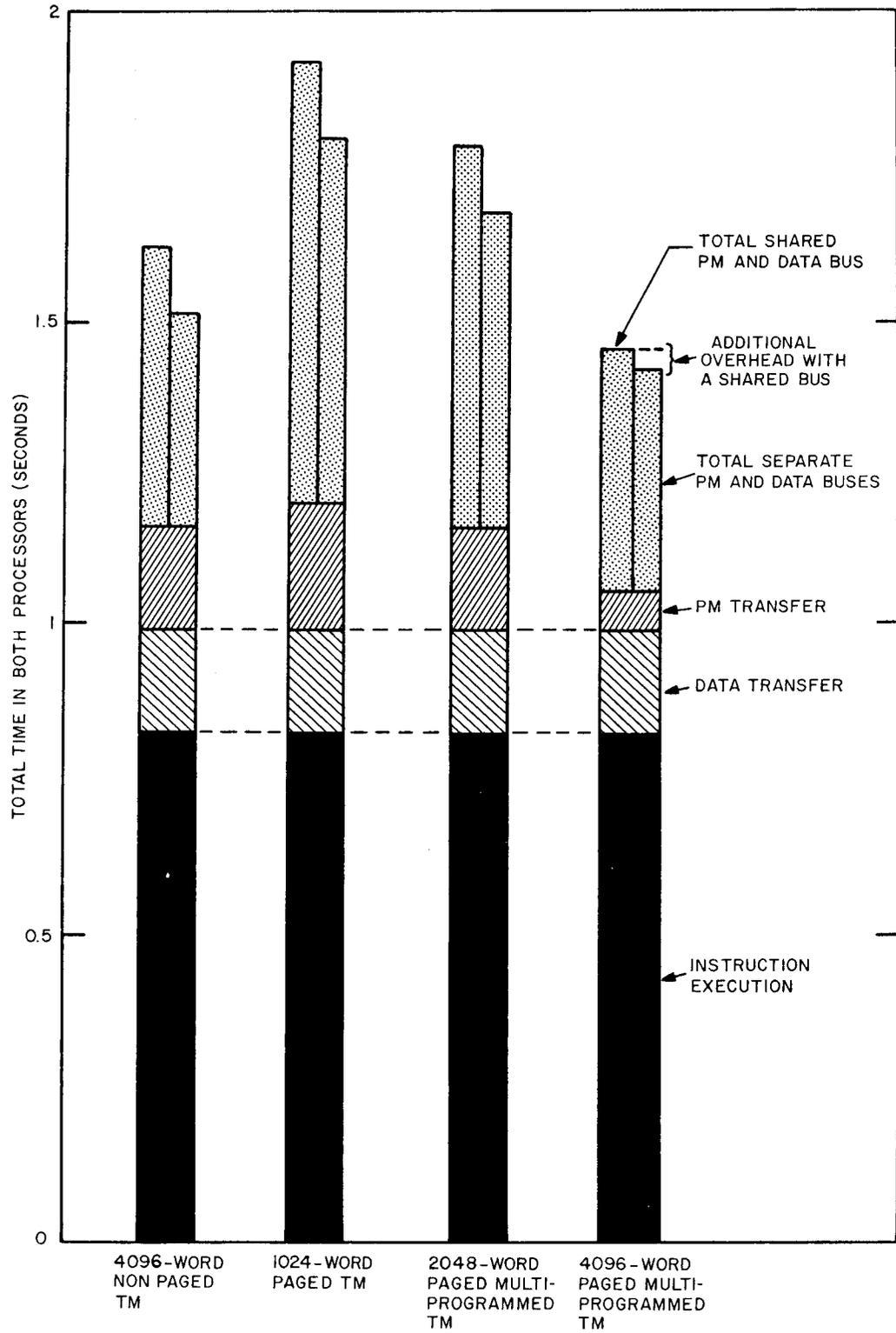


Fig. 7--Dual processor CPU utilizations over a 1-second simulated run and 1074 PM iterations

simulations were run for these cases. CPU utilization is not given for floating-executive operation, since only dedicated software and hardware MECs were considered for the multiprocessor simulations.

The results indicate that the relative benefits of multiprogramming TMs in a multiprocessor do not match those in the simplex system, because, without specific strategy governing assignment of PMs to multiple CPUs, PMs suffer lower probabilities of finding needed pages resident in TM from previous iterations. Therefore, higher rates of page faulting occur.

The performance of multiprogramming in multiprocessors (with arbitrary PM assignment to CPUs) can be commented on as follows. Assume a program workload which can be divided into  $N$  separate and independent, but similar, groups of PMs, where  $N$  is the number of CPUs in a multiprocessor which is to service that workload. Consider two CPUs such that the first of these is a CPU in the  $N$ -CPU multiprogrammed multiprocessor which is to process our assumed workload and the other CPU is an independent unit dedicated to process *one* of the  $N$  subgroups of PMs created by partitioning the assumed workload. Each of these two CPUs is processing an equal workload in terms of numbers of PM iterations, instruction executions, page references, etc., by our assumption that the  $N$  subworkloads have properties similar to each other and to the complete workload. The difference is that the first CPU can be assigned to process any PM in the entire workload whereas the other is subject to a range of PMs only  $1/N$  as large as the first. Although both CPUs would generate page references at the same rate, the CPU in the multiprocessor generates its references over a range of program  $N$  times as great as the independent CPU. Then, for both CPUs to demonstrate the same paging performance in terms of page faulting rate, one would expect the CPU in the multiprocessor to have to have a local (task) memory  $N$  times as large as that of the individual CPU dedicated to  $1/N$  of the workload.

Figure 7 shows CPU utilizations for program-instruction and data transfers using separate buses and sharing the same bus. The results show greater overhead with a shared bus (about 8% more CPU time in the nonpaged system) compared to the same system with separate program and data buses. This additional overhead is composed of transfer waiting time and extra executive activity.

Analysis of the results in Appendix D shows that average program-instruction and data transfer overheads were increased by about 25% by the additional waits suffered in attaining the services of the shared bus. The effect of this on total system operating efficiency depends on the relative amount of system time constituted by transfer overhead to begin with. The dual processor under the expanded GE workload shows less than 10% additional total time traded for use of the shared bus in any of the system configurations.

### Triple Processor

Triple processor simulations of the AADC were run under similar conditions as the dual processor except for two changes. First, the GE workload was expanded somewhat further in accordance with the extra processing capability. Second, the executive parameters included those values specified for the hardware MEC. Executive activity increases

almost linearly with task processing rates, and the higher throughput of the hardware MEC allows more room for meeting expanded executive processing requirements.

The hardware executive routine run times were as follows:

Interrupt processing,	3.6 $\mu$ sec,
Real time clock,	26 $\mu$ sec,
PM reinitialization,	36 $\mu$ sec,
PM assignment,	24 $\mu$ sec,
External PM enable,	30 $\mu$ sec,
PM completion,	10 $\mu$ sec,
Data/program transfer,	15 $\mu$ sec,
Dedicated channel selection,	3 $\mu$ sec,
Page fault,	5 $\mu$ sec.

Figure 8 shows CPU utilization in the triple processor. The additional percentage overhead contributed by use of the shared bus for transfer of program instructions and transfer of data is about double that experienced in the dual processor. This is in spite of the added efficiency of the hardware MEC in the triple processor. In fact the free run times of the executive transfer-request routines are given as 14.5 and 16 microseconds respectively (5) for the hardware and software executives. This suggests that, other than for faster interrupt recognition, the hardware MEC cannot provide any special relief from overhead due to program-instruction and data transfers.

As a point of comparison, a run of the nonpaged triple processor was made with the executive parameters set for a dedicated, software MEC. The result is included as the left-most bar in Fig. 8. It shows that, for the nonpaged system with separate program and data buses and a hardware MEC, (the right-hand split portion of the second bar from the left), the additional overhead born by going from a hardware to software MEC is less than that born by going from separate to shared program and data buses. The capacity of the system for meeting transfer requirements with a single bus is being pushed closer to its limit of performance by the extra workload activity in the triple processor than it is being pushed to meet the supervisory requirements with the slower MEC.

Executive activity in the multiprogrammed system with 4096 words of TM for program residence is only modestly increased by shared-bus overhead. If the program-transfer or data-transfer activity is low to begin with, the penalty for requiring them to share a single bus is relatively small. So it is here, where multiprogramming has reduced PM transfers.

## CONCLUSIONS

### System Operation

Simulations of the AADC simplex, dual, and triple processor configurations were run to examine the effects of various system parameters on CPU utilization. Those hardware and executive functions consistently required for the processing of active workload tasks

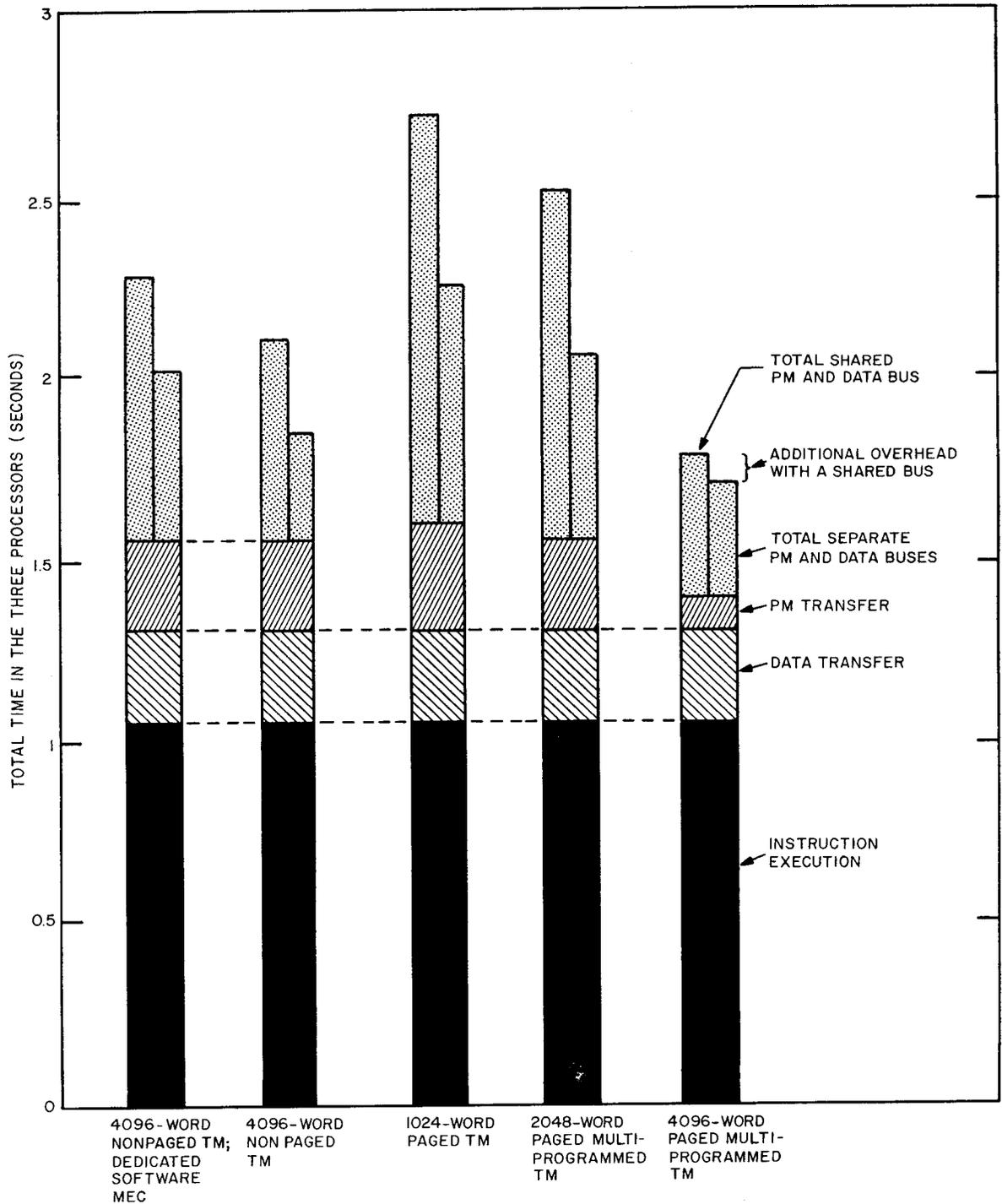


Fig. 8—Triple-processor CPU utilizations over a 1-second simulated run and 1320 PM iterations

were incorporated into the simulation design. Although the results are not independent of the particular workload models used to drive the simulation, certain trends and averages in the results allow reasonable conclusions as to the course of effective AADC system designs.

The bar graphs of CPU utilization indicate that a level of 50% of system time spent in instruction processing is easily attainable and a minimum goal for system effectiveness in simplex or multiprocessor realizations. Overall effectiveness does depend strongly on the workload in terms of average task processing times per iteration. The system overhead involved in getting a PM through assignment, transfers, and completion is relatively constant (about 1/2 millisecond) for a given system configuration, and workloads with long running PMs will allow greater system effectiveness in proportion to their instruction processing times.

The system configuration displaying most efficient use of processing resources in the simplex processor with paging and multiprogrammed TM. CPU utilization of up to 70% with a floating MEC and 80% with a dedicated MEC is indicated. Multiprogramming reduces not only PM transfer overhead but also the executive overhead associated with these transfers.

The results show that multiprogramming the multiprocessor does not provide the same increase in performance when workload PMs can arbitrarily seize the services of the first available CPU in the system. Under certain conditions a multiprocessor with  $N$  CPUs would have to have TMs  $N$  times as large as that of a simplex processor to achieve the same multiprogramming performance. Thus the recommendation is that, to best multiprogram TMs in an AADC multiprocessor, the workload should be divided among the CPUs in the system on a dedicated basis. A PM dedicated to a particular CPU would be assigned only if that CPU is available. Consequently the multiprocessor appears very much like two or more simplex processor, each with its own smaller workload, except that they are under control of the same executive and share common communication and storage facilities. The multiprogramming effectiveness of the simplex processor would tend to be passed on to the multiprocessor. This would mean, of course, that the executive would have to rededicate some PMs, in the event of a CPU failure, to the remaining operable CPUs.

There is another benefit from partitioning a workload among different CPUs in a multiprocessor. Workloads studied have contained tasks conflicting in the processing time of one with the iteration interval of another. If such a conflict is to be avoided, means must be provided either for the high-repetition-rate task to break into the long processing time of the other or for conflicting tasks to be assigned to run in different CPUs of a multiprocessor. Thus, if PMs were partitioned into families under different CPUs, tasks with conflicting timing would be put into different families.

### Executive

The executive overhead is a function of the type of MEC used (dedicated or floating software or dedicated hardware) and the system configuration it must supervise. In the

simplex system the added CPU time usurped by floating executive routines is over half the overhead caused by the dedicated MEC. This additional overhead is due to those executive routines not involved in direct control of processing activities and due to which routines there is no task processing delay under normal circumstances. These routines are real time clock, PM reinitialization, transfer completion, and those PM assignments which make no assignment because of unavailable CPUs or lack of PMs ready for execution.

The floating executive simulation does not account for CPU time which might be consumed in transferring executive routines into TM for processing. The requirement that a large block of executive program be brought into TM each time a certain routine is required could raise total system overhead by a significant amount, considering that nominal PM processing times are only 1 or 2 milliseconds. That subset of floating executive routines routinely needed to supervise the execution of workload tasks should reside permanently in TM on the basis that each one of those routines is required to execute at least once for each PM iteration.

PM assignment consumes the greatest amount of time in the software executive because of its long nominal execution time (113 microseconds). Therefore its activity should be limited by judiciously listing it for processing only when PMs are ready for execution and CPUs are available to service them.

Real time clock is the next-highest time consumer in these simulations due to the high clock update rate (1 millisecond). As with PM assignment, it would appear desirable to limit real-time-clock activity to bare essentials in the floating executive, where all unnecessary activity directly delays workload processing. Limiting these two executive functions, as discussed in the simplex processor simulation results, did indeed reduce CPU overhead but not by an amount which would indicate that the overhead was out of line to start with. That is, a 1-millisecond clock does not appear to be compromising executive performance.

Allowing executive functions the use of a dedicated processor appears appropriate in the multiprocessor AADC. The software executive in the dual processor with a shared bus for program instructions and data would keep a CPU active more than 50% of the time, assuming a full program workload. Also, sharing an executive processor with workload PMs could cost undesirable delays in PMs assigned to that processor.

The hardware MEC in the nonpaged triple processor configuration was also active about 50% of the time with separate program-instruction and data buses in the system. A dedicated software executive in the same system stayed active about 80% of the time based on a full workload. The hardware executive appears not unwarranted in the triple processor, judging from its 50% or higher usage rate. However, a dedicated software executive would not, it seems, be overburdened, at least not if separate program-instruction and data buses are maintained. The difference in total CPU utilization between the hardware and software executive is about 10% in the unpagged triple processor. In short, the software executive seems to be about as capable of managing three CPUs as two, on the basis of per-CPU utilization. The use of the hardware executive provides an added bonus largely because of the greatly shortened time to execute PM assignments. If means could

be found to significantly reduce the time required by the software executive to assign PMs, it would be the recommended choice for managing three as well as two CPUs.

### Busing

The toll on CPU utilization exacted by forcing program-instruction and data transfers to share the same bus depends, of course, on the amount of traffic trying to use that bus. The increase in the CPU overhead for a dual processor (with software executive) ranges from 8% in the monoprogrammed configuration to less than 2% with 4096 words of multiprogrammed memory. Multiprogramming reduces program-instruction transfer activity and the corresponding conflict time for bus usage. The triple processor (with hardware executive) under the same conditions suffers additional overhead ranging from about 20% to 5%. The hardware MEC has not saved the three-CPU system from experiencing the expected effects of 50% more data and program-instruction activity competing for a bus, as compared with the dual processor. The almost equal processing time for bus-transfer routines in both executives does not provide for significant difference in system overhead insofar as transfers are concerned.

Use of a single shared bus for program instructions and data is apparently a good tradeoff in the dual processing system. A maximum 10% loss in CPU utilization is expected with 5% or less being a more nominal figure. The triple processor stands to lose significantly more of its CPU resources if a shared bus is used. If the goal is a reduction in system hardware complexity, it would appear more fruitful to maintain separate buses and to use a dedicated-software executive. More overhead is charged to the nonpaged, triple processor by going to a shared-bus system than by going to a software MEC. Moreover, if high performance requirements dictate the use of a hardware executive, it would not make sense to compromise most of the gain by using the shared bus system.

In either a dual or triple processor the overhead from shared busing would be significantly reduced if executive interaction in data and program-instruction transfers is eliminated. In fact any configuration of simplex or multiprocessor would experience an increase in CPU utilization with that aspect of executive overhead removed.

### Remarks

The results contained herein depend to some degree on the workload models chosen for the simulations and on assumptions made about the characteristics of AADC designs. Analysis of these results and conclusions about them have been made accordingly, and caution should be exercised in applying them beyond the scope of this work. Characteristics of the simulation models have generally been chosen conservatively; certain system hardware parameters of projected AADC designs now surpass those used in this work and would result in better performance than estimated here.

As a result of this and previous work, some of the system concepts explored in this report have already been made part of the projected AADC designs. Paging and multiprogramming of task memory are such concepts and are being actively studied for their

effect on related system components. Also, elimination of MEC intervention in memory transfers has been proposed and would markedly reduce system overhead from floating or dedicated executives.

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## APPENDIX A

### CHARACTERISTICS OF THE SIMULATED WORKLOADS

Each program workload to run in the AADC is partitioned into a set of individually managed subprograms or program modules (PMs). Each PM would normally implement some independent task or portion thereof such as navigation, antenna steering, or track correlation. The AADC executive manages the scheduling and execution of all tasks in the workload according to the requirements of the mission being carried out. A PM, according to real-time requirements, may be required to perform its task at a given fixed rate or perhaps only when specifically requested by some device external to the AADC.

Figures A1 through A3 display representations of the program modules of the simulated workloads, stating the workload functions which the PMs implement and giving the processing parameters. For each PM nominal values are given for the number of program memory locations, instruction executions, and data word transfers required at each execution of that PM. The arrows and associated time values show the scheduling requirements of each PM in terms of the length of time interval in which each processing iteration must occur. Those PMs marked "Clocked" must execute at a fixed iteration rate specified by the iteration interval shown and are scheduled under control of the internal system clock. Those PMs marked "External Enable" are activated by receipt of an interrupt from an external device, which interrupt is generated in the simulations according to Poisson arrival statistics with a mean rate as specified by the time interval shown. Some PMs depend on others for data and, as such, can execute only after them. As displayed in the figures, such PMs form chains of predecessor-successor tasks which must be processed in the order shown.

The number of instruction executions required by some PMs is so great as to extend their processing time well beyond the allowed iteration interval of another PM in the same workload. For example, in the F-111 workload, PM 9 requires 80,000 instruction executions for a processing time of greater than 40 milliseconds, whereas PM1 must execute once every 8 milliseconds. The simulation does not allow for faster PMs interrupting slow ones. Rather, a long PM such as PM 9 was considered to be executable in a chain of separate processing iterations (say 10,000 instruction executions each) that are short enough to allow the interjection of faster PMs such as PM 1 in the pauses or breaks between.

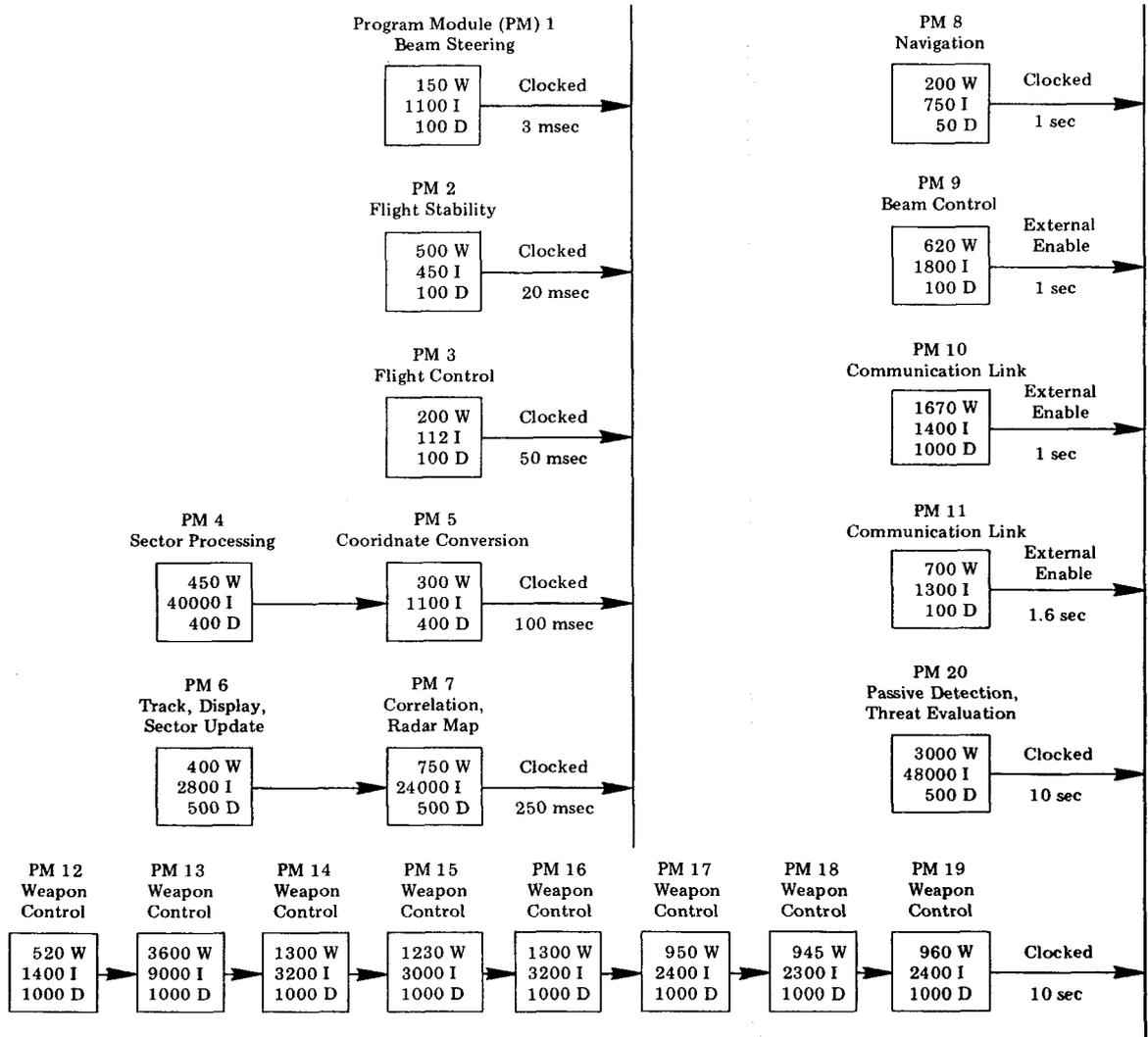


Fig. A1—Program module configuration derived from the workload for a General Electric mission study. For each PM nominal figures are shown for the number of program memory locations (W), instruction executions (I), and data word transfers (D) required at each execution of that PM.

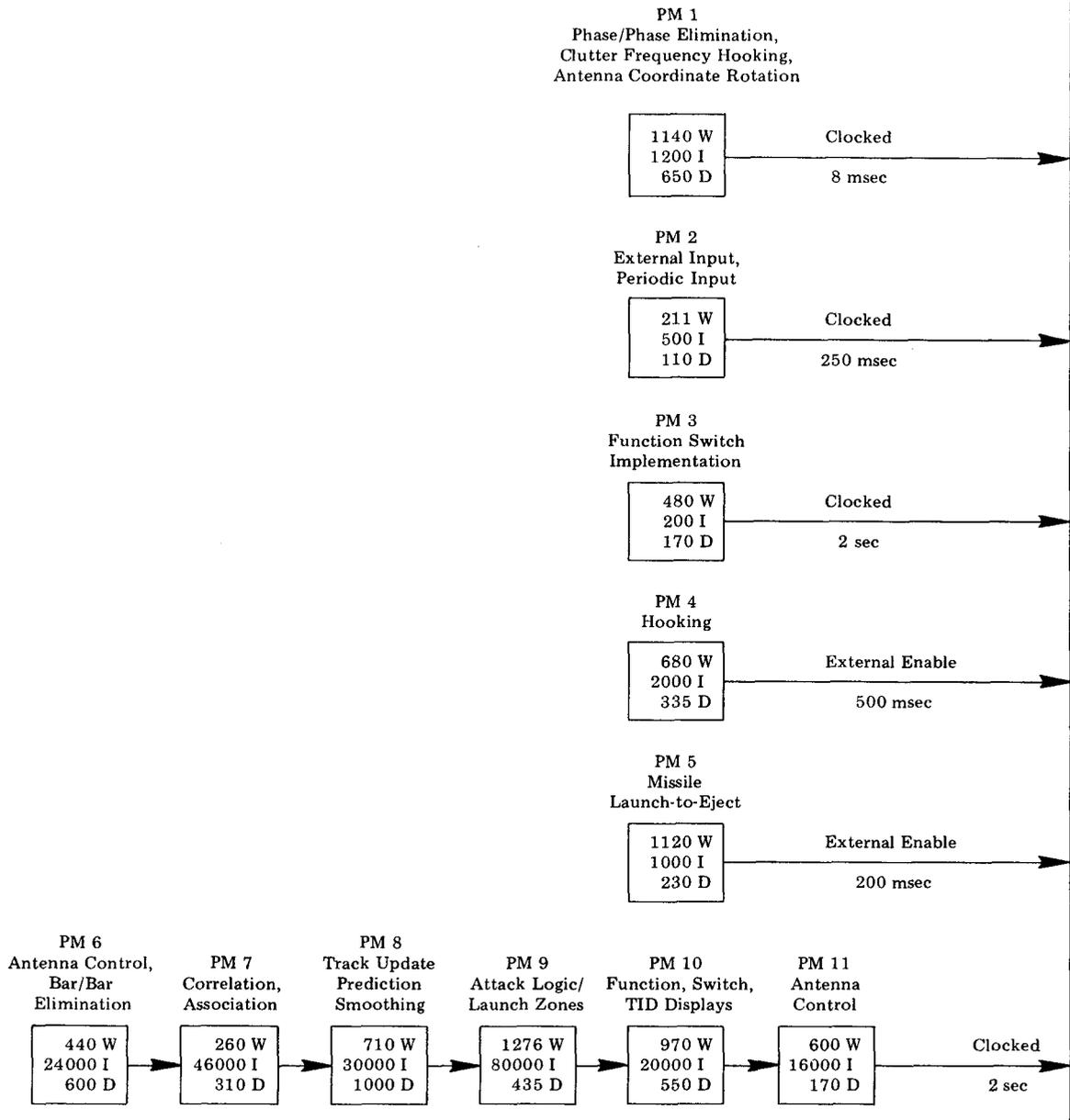


Fig. A2—Program module configuration derived from a workload for the F-111 aircraft

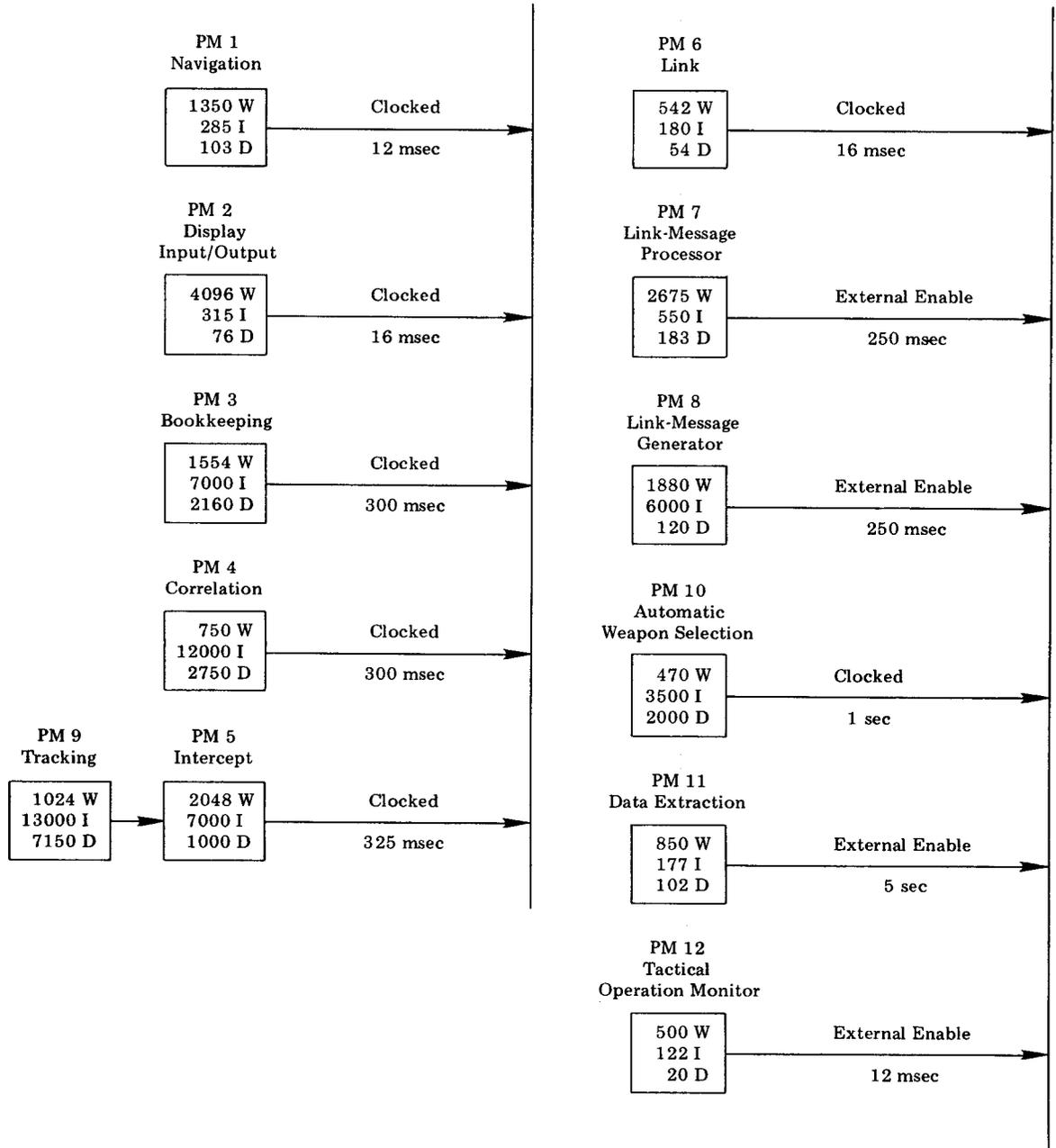


Fig. A3—Program module configuration derived from a workload for the E-2B aircraft

## APPENDIX B

### SIMULATED MEC ROUTINES

The simulated MEC routines are incorporated into the simulation to implement certain functions of the AADC executive system. They are activated through a system of interrupts generated in the AADC. Each interrupt generated in the simulated system is placed on a list and taken from it on a first-come-first-served basis for processing. One routine, interrupt processing and recognition, serves to take the interrupt from the list, recognize it, and then list for processing the appropriate MEC routine for carrying out the executive functions requested by the interrupt. The list of MEC routines to be processed is served on a highest-priority-first basis.

The simulated MEC functions, their processing times by software and hardware executives, and their relative priorities are given in table B1. Figures B1 through B13 show flow charts of these routines.

Table B1  
MEC Function Run Times and Priorities

MEC Function	Software MEC Processing Time ( $\mu$ sec)	Hardware MEC Processing Time ( $\mu$ sec)	Relative Priority
Interrupt recognition and processing	7	3.6	
Real time clock update	40	26	8
PM reinitialization	51	36	2
PM assignment	113	24	1
External PM enable	61	30	9
PM completion	15	10	10
Data transfer request	16	15	3
Data transfer completion	16	15	4
Program transfer request	16	15	3
Program transfer completion	16	15	4
Dedicated bus selection	9	3	6
Dedicated bus release	9	3	7
Page fault	5	5	5

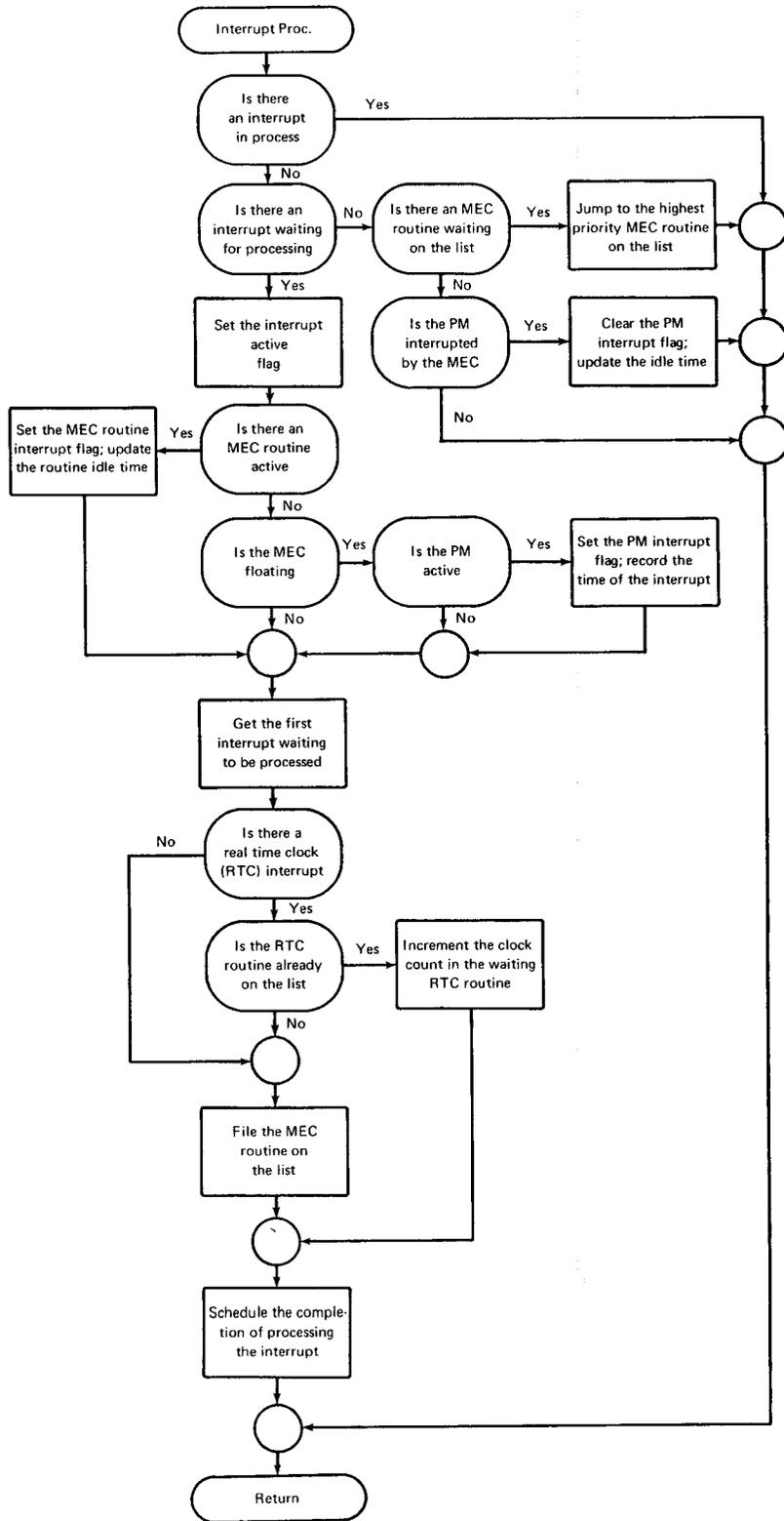


Fig. B1—Interrupt recognition and processing

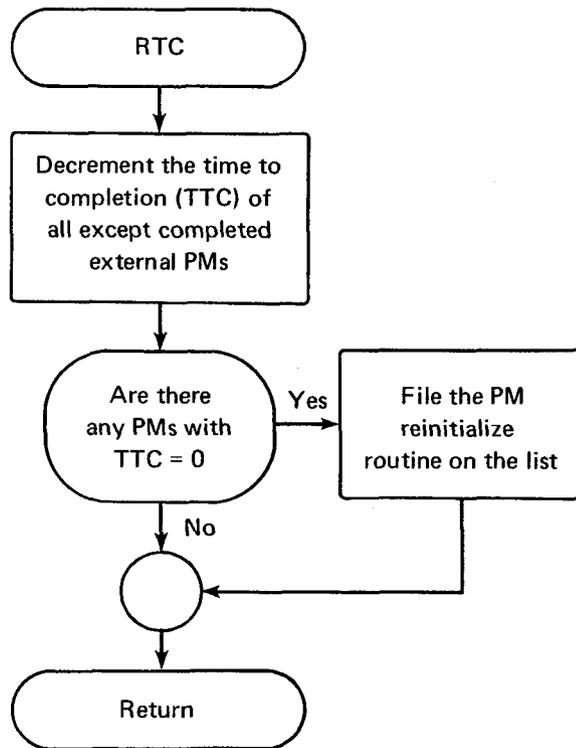


Fig. B2—Real time clock update

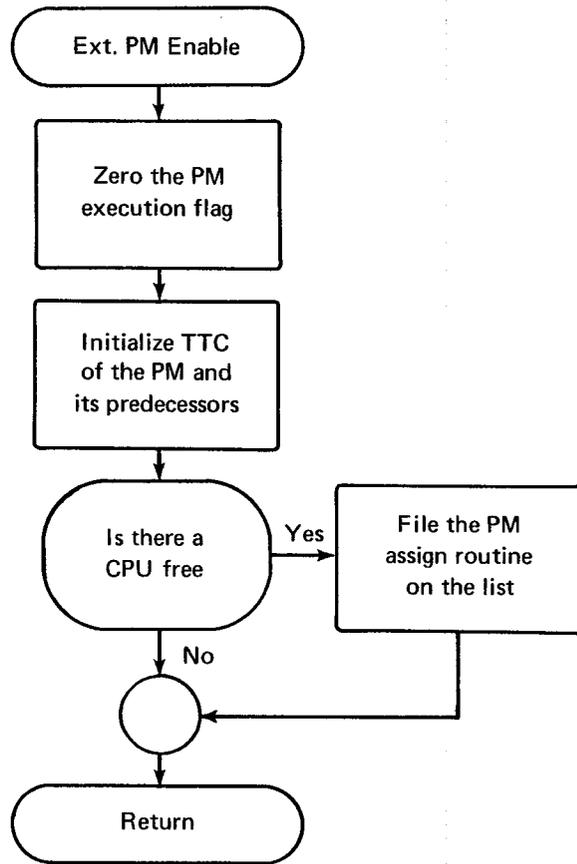


Fig. B3—External PM enable

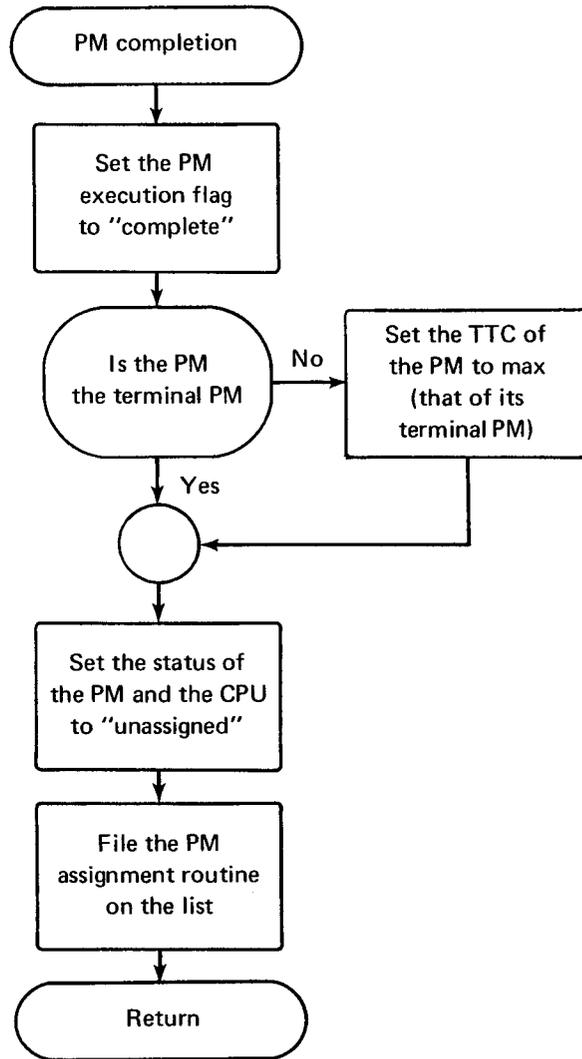


Fig. B4—PM completion

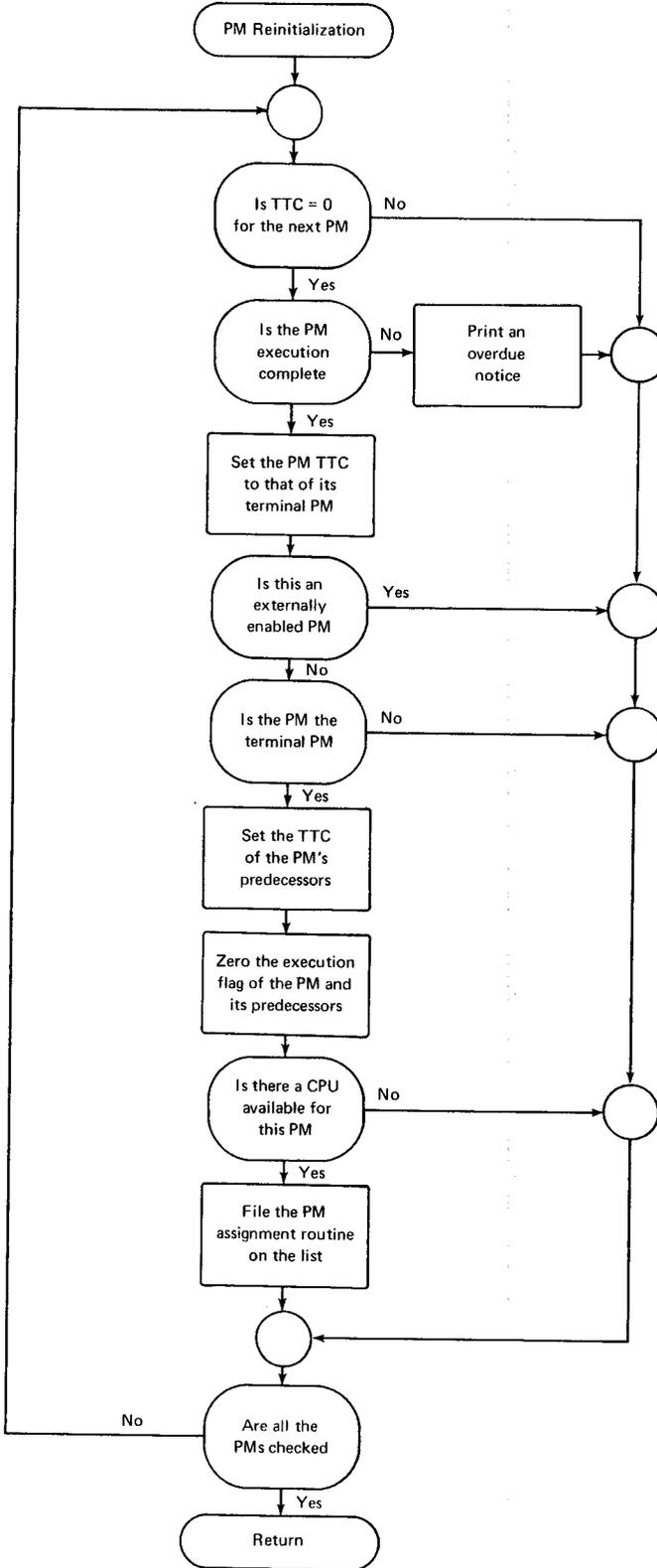


Fig. B5—PM reinitialization

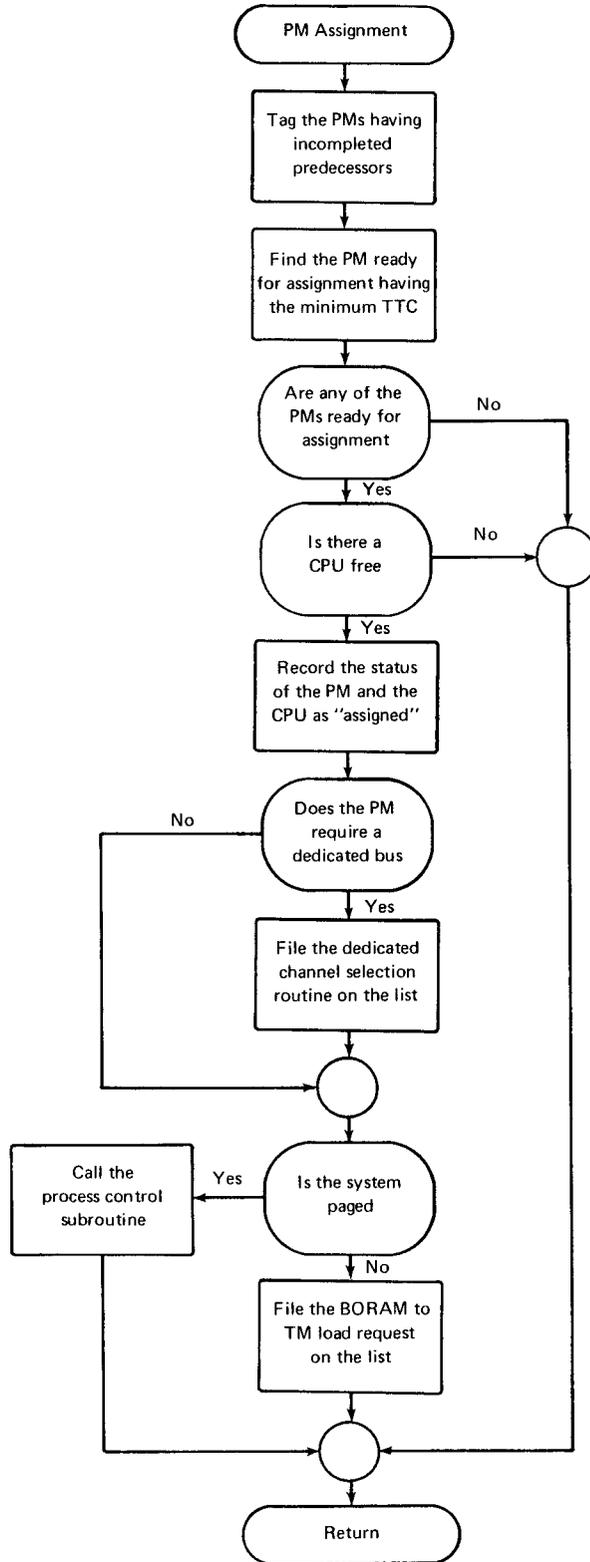


Fig. B6—PM assignment

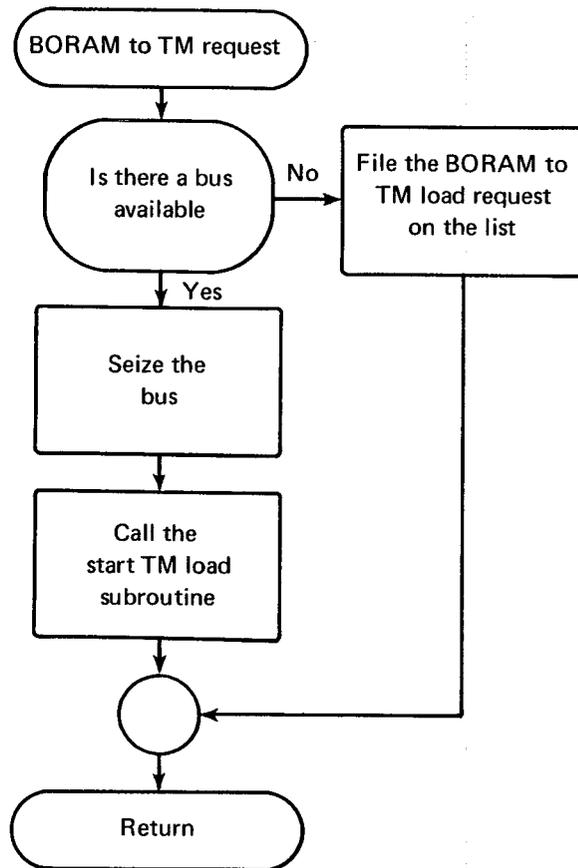


Fig. B7—BORAM-to-TM (Program) transfer request

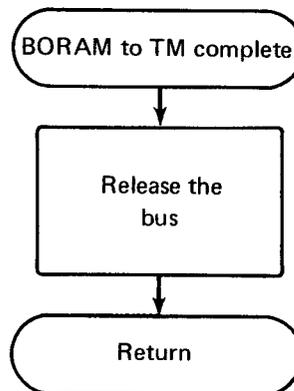


Fig. B8—Completion of the BORAM-to-TM transfer

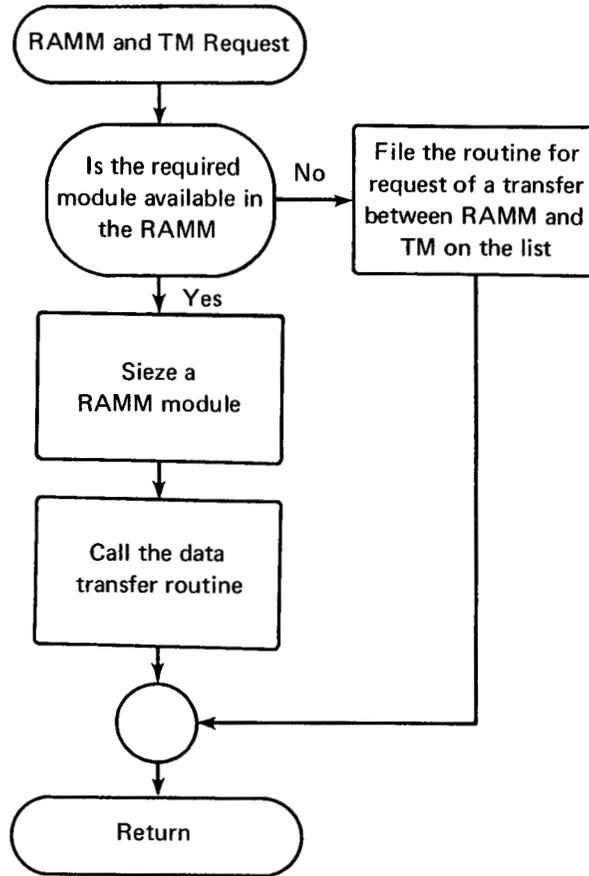


Fig. B9—Request for a transfer between RAMM and TM (data transfer)

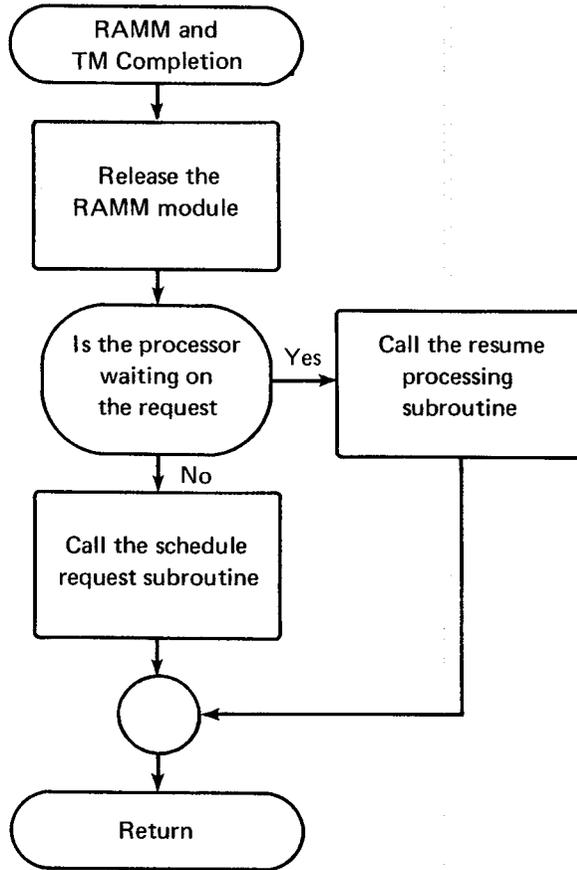


Fig. B10—Completion of a transfer between RAMM and TM

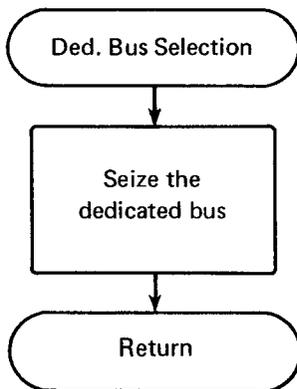


Fig. B11—Dedicated bus selection

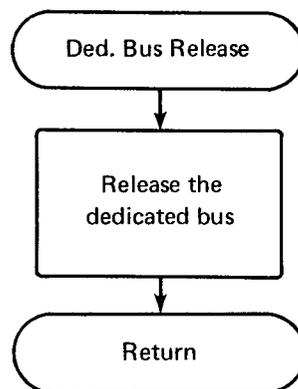


Fig. B12—Dedicated bus release

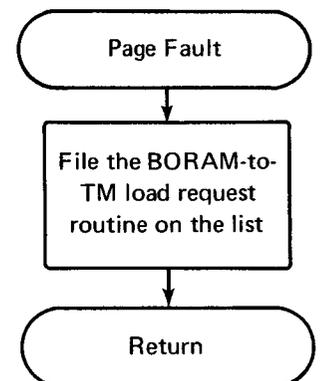


Fig. B13—Page fault

APPENDIX C  
SIMULATION ROUTINES

The simulation system is composed of Simscript routines which implement the functions of the AADC system model. These routines are of two types: event routines activated at scheduled times by the Simscript system scheduler and normal subroutines activated by direct jumps within the system. Flow charts of these routines are shown in Figs. C1 through C20, and the functions of the routines are briefly described in the figure titles.

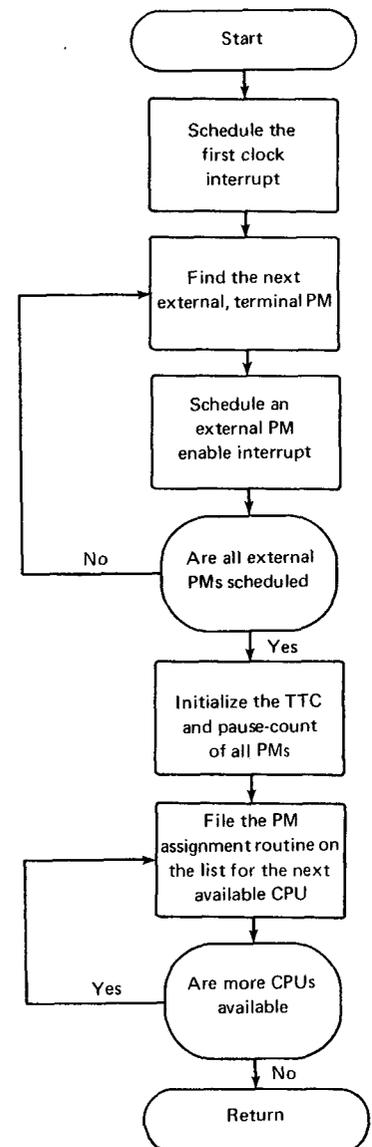


Fig. C1—Start. This is an event which occurs just once at the very beginning of a simulation to start the system running. It schedules the immediate occurrence of the first real time clock and external PM enable interrupts. Then all PMs are initialized with respect to their iteration intervals, and the MEC PM assignment routine is listed for execution.

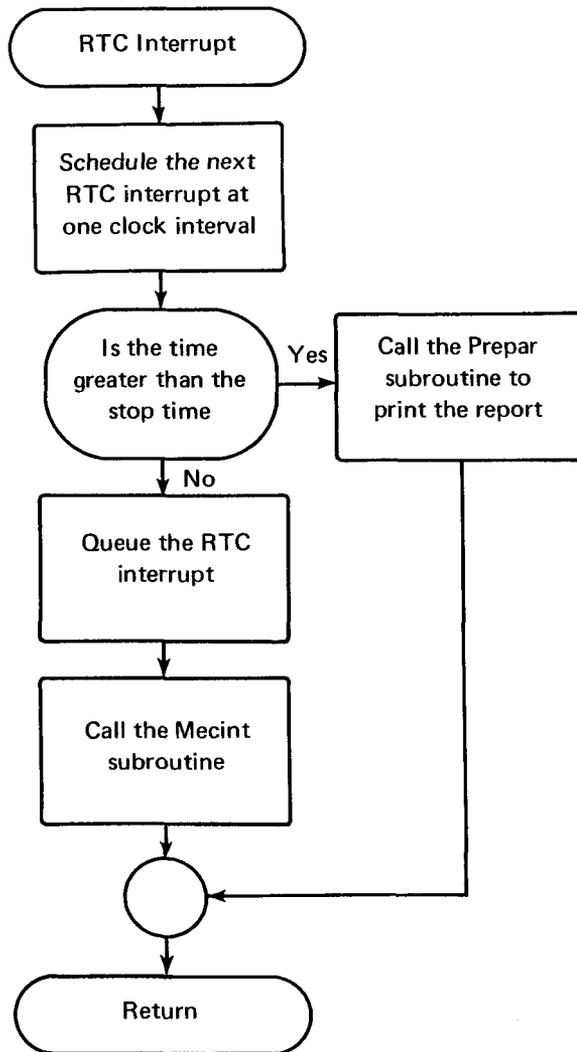


Fig. C2—Real time clock. This is an event routine which first schedules its own reoccurrence at one clock interval in the future. Next it checks whether the simulated time has exceeded the specified simulation run time and, if so, calls a subroutine to prepare the printout of the simulation results. If the run is not ended, the RTC (real-time clock) interrupt is queued and the Mecint subroutine is called to commence the interrupt processing.

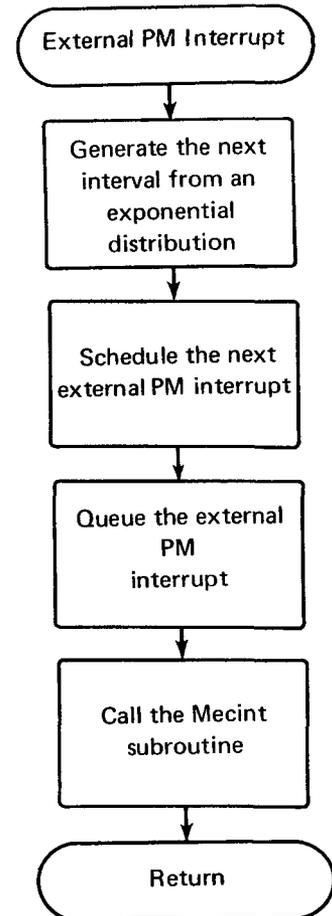


Fig. C3—External PM interrupt. This is an event routine which first schedules its reoccurrence according to the mean execution rate of the PM and an exponential probability distribution. It queues the external PM enable interruption and jumps to subroutine Mecint to commence interrupt processing.

Fig. C4—Mecrou. This is a subroutine which initiates MEC routine processing. A flag is set indicating that the executive routine is active, and the variable used to store accumulated time that a routine is idled by interrupt processing is zeroed. The event Mecom is then scheduled to occur at a time given by the processing time of the executive routine being started.

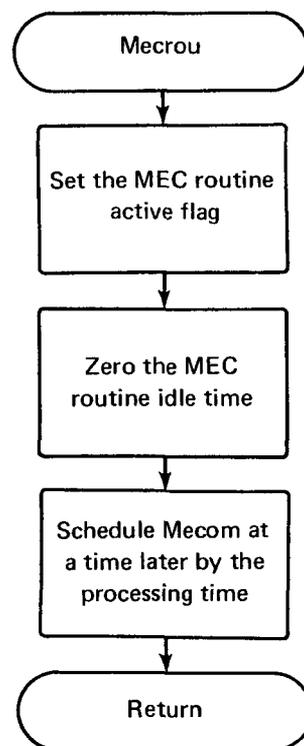
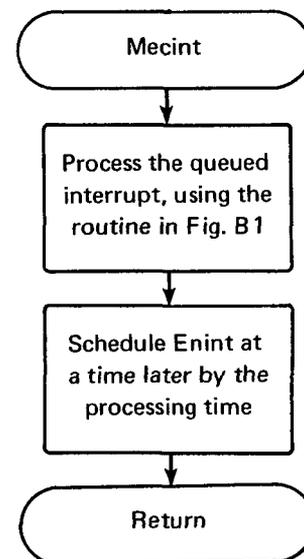


Fig. C5—Mecint. This is a subroutine which performs the function of recognizing and processing interrupts as described in the main body of this report. It then schedules the event Enint, which marks the completion of the interrupt processing interval later by the time specified for execution of the interrupt processing routine.



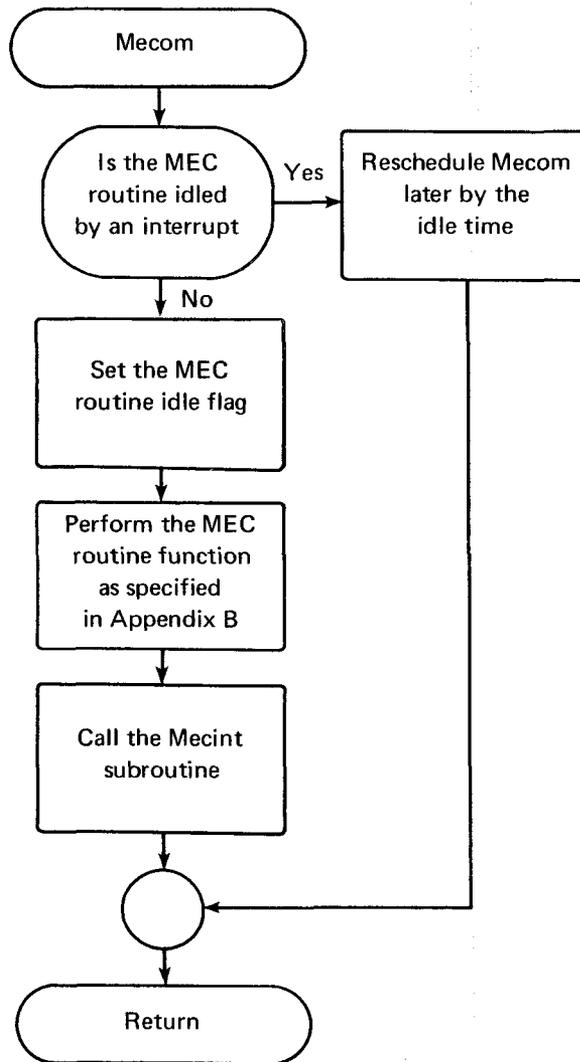


Fig. C6—Mecom. This is an event which marks the completion of an executive routine processing interval. First, if any idle time has accumulated during the interval, Mecom is immediately rescheduled for the time later by the idle time and an exit is made. If no idle time has accumulated, the routine flag is set to active and the appropriate executive functions are performed as described in the report. The Mecint subroutine is then called to initiate processing of other routines which might be waiting on the executive job list.

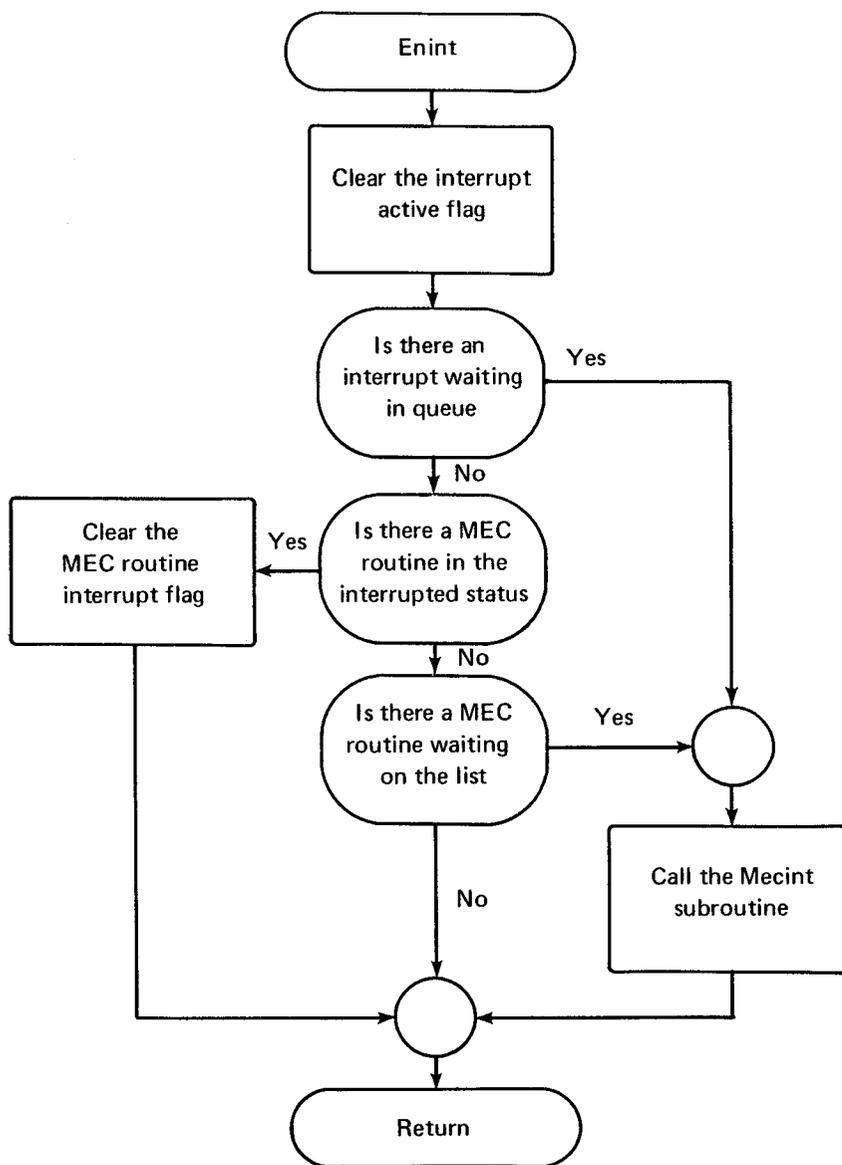


Fig. C7—Enint. This is an event which marks the completion of the interrupt processing routine. The interrupt-processing-active flag is first cleared. If other interrupts are waiting in queue for processing, the Mecint subroutine is called and an exit made. If no interrupts are waiting, a check is made to determine whether an active executive routine was interrupted by the interrupt processing, and, if so, the routine interrupt flag is cleared and an exit made. If no active executive routine was interrupted, a check is made to determine if any executive routines are waiting for processing, and, if so, the Mecint subroutine is called to initiate the highest priority routine on the list.

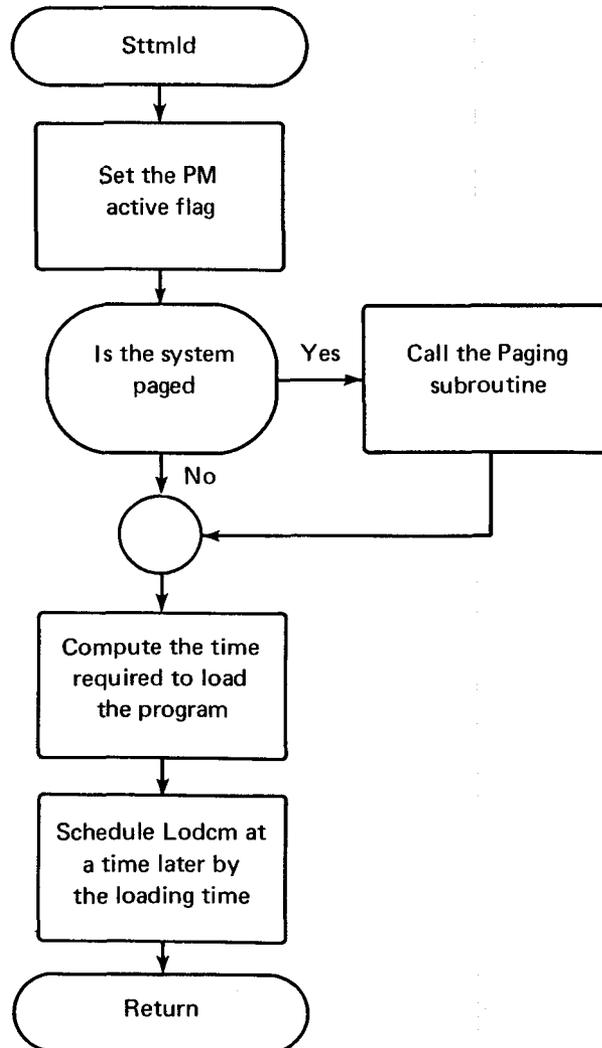


Fig. C8—Sttmld. This is a subroutine which initiates BORAM-to-TM loading (starts TM loading). A flag is set to denote CPU activity, and, if the system is paged, subroutine paging is called to update the TM page contents. The time required to transfer the PM or page is computed, and the Lodcm event is scheduled at the proper time to mark completion of the transfer.

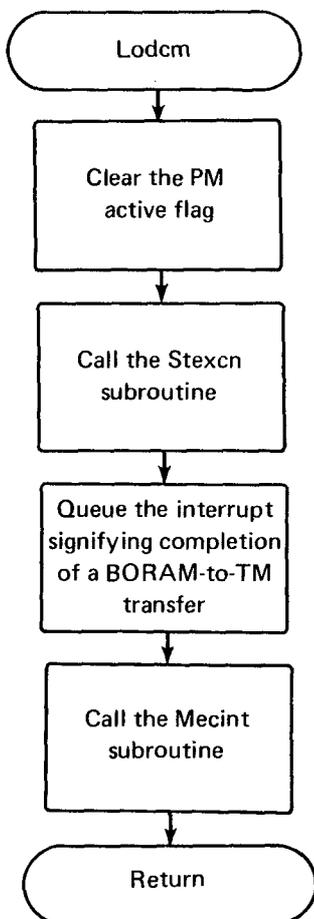


Fig. C9—Lodcm. This is an event which marks completion of the program transfer. The active flag is cleared, and the Stexcn subroutine is called to initiate processing of the next program segment. An interrupt signifying the completion of the program transfer is listed, and the Mecint subroutine is called to process it.

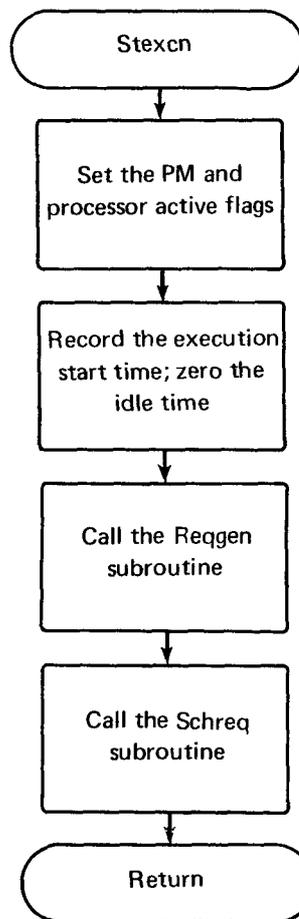


Fig. C10—Stexcn. This is a subroutine which initiates processing of a program segment (starts execution). Activity flags are set and execution start and idle times are initialized. Next, the Reqgen subroutine is called to generate and file the segment's data requests. Finally, the Schreq subroutine is called to initiate activities of these requests.

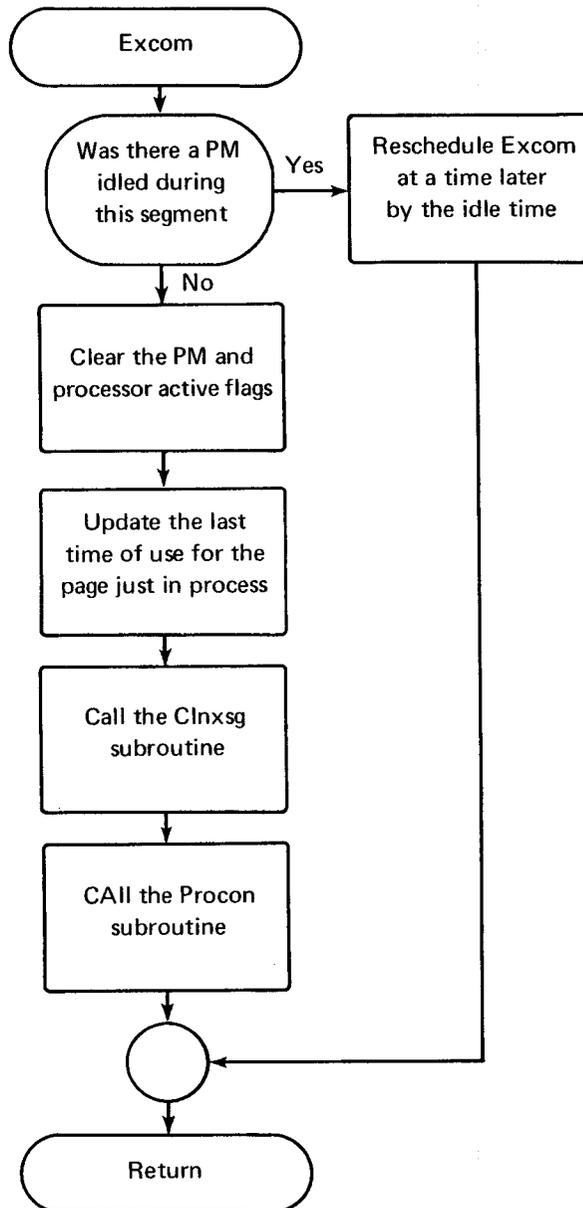


Fig. C11—This is an event which marks completion of a program segment's execution. If idle time has accumulated during this processing activity, Excom is immediately rescheduled later by the time spent idle and an exit is made. Otherwise, activity flags are cleared, the program page usage data are updated, and subroutine Clnxsg is called to determine the next segment to enter processing. Finally, subroutine Procon is called to determine what action the system must take to process the next segment.

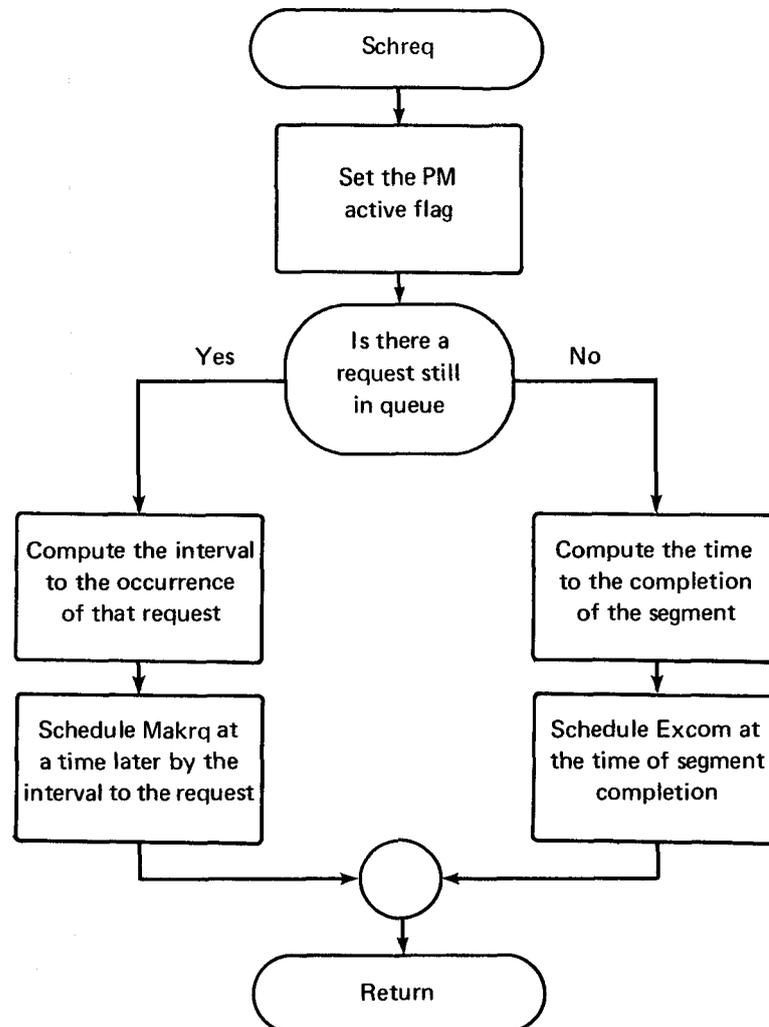


Fig. C12—Schreq. This is a subroutine which schedules the occurrence of each data request during a segment's processing. First the active flag is set and a check is made to determine if any requests are listed. If there are none, the Excom event can be immediately scheduled at a time computed by the interval required to complete the number of instruction executions specified for the segment. If any events are found in the list, the first one is examined and the Makrq event is scheduled to mark the occurrence of that data request in the program.

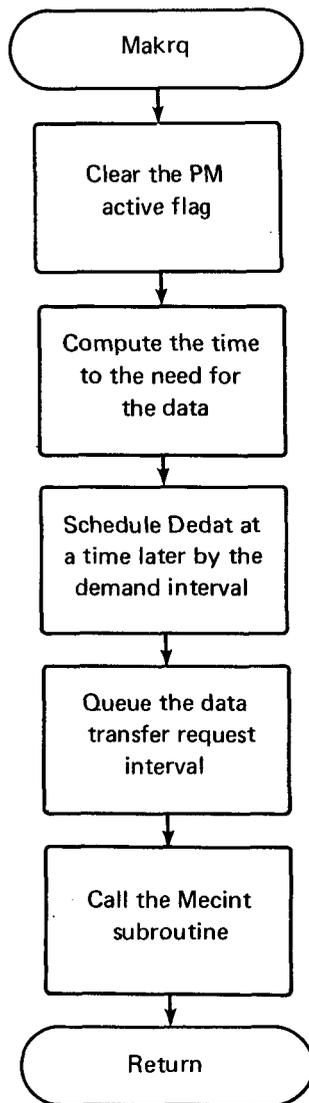


Fig. C13—Makrq. This is an event which marks the occurrence of a data request in a program. The program active flag is cleared, and the Dedat event is scheduled to mark the requirement for those data by the program making the request. A data transfer request interrupt is listed, and the Mecint subroutine is called to process the request.

Fig. C14—Dedat. This is an event which marks the time at which the data requested by a program are needed in its computations (demands data). If the data transfer has been completed by this time, an exit is made. Otherwise, interrupt program processing.

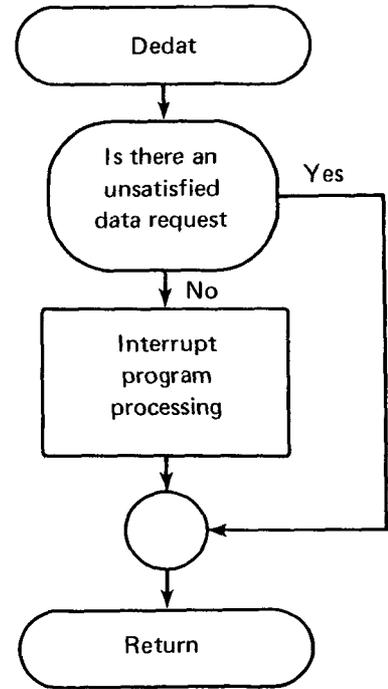
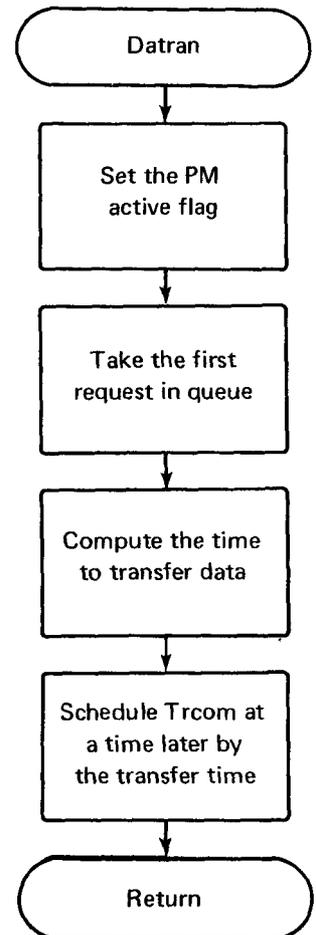


Fig. C15—Datran. This is a subroutine which initiates a data transfer between RAMM and TM. The processor activity flag is set, and the first data request is taken from those filled at the start of the segment execution. The time required for the transfer is computed, and the Trcom event is scheduled accordingly to mark the transfer complete.



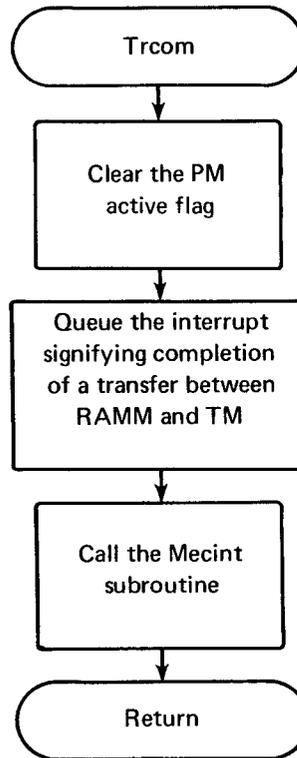
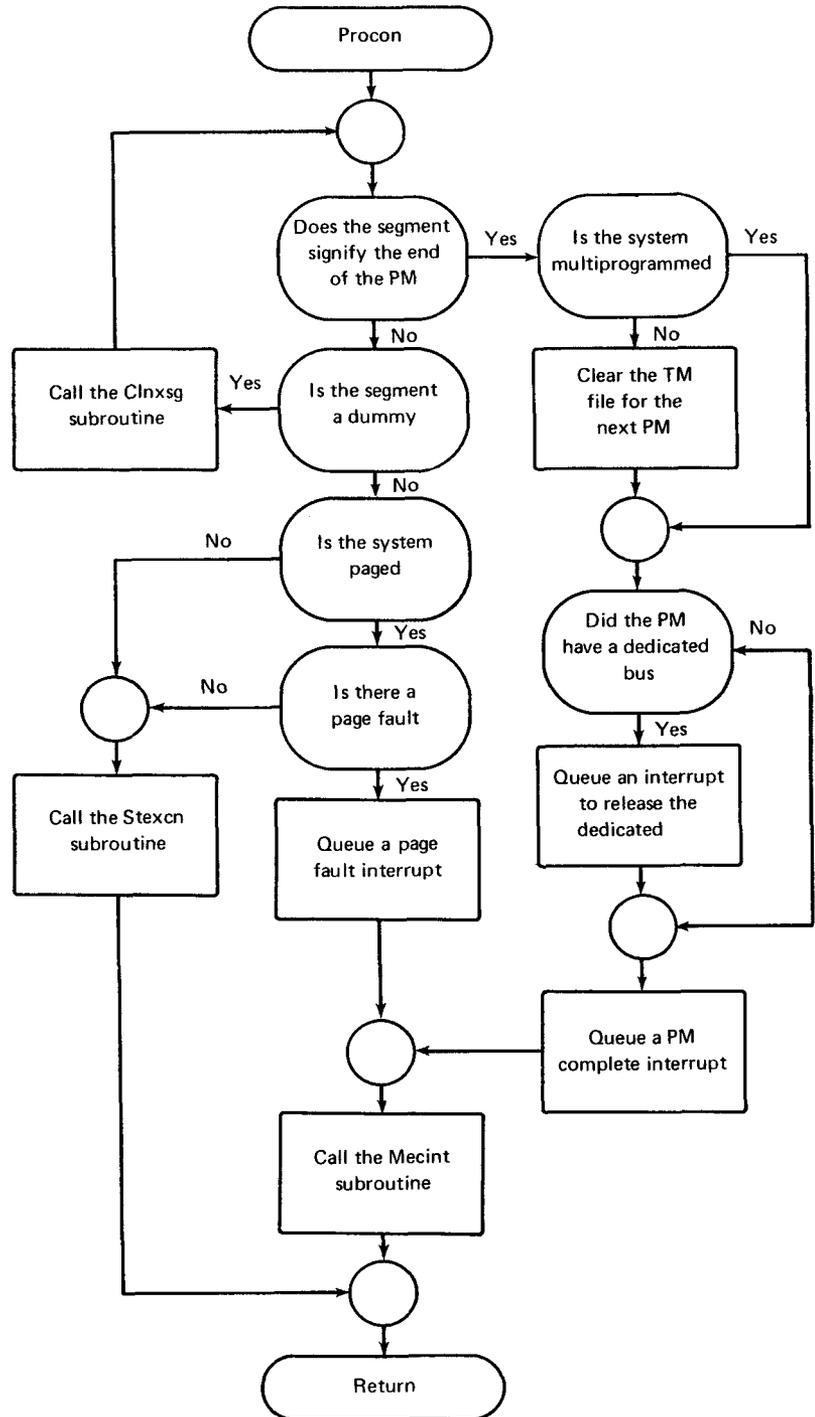


Fig. C16—Trcom. This is an event which marks the completion of a data transfer. The active flag is cleared, a transfer complete interrupt is listed, and the Mecint subroutine is called to process it.

Fig. C17—Procon. This is a subroutine which controls the system action to be taken in response to the next program segment referenced for processing. There are a number of possibilities according to the attributes of this next segment. The segment signifies that the PM is complete, or the segment is a dummy having no processing requirements, or the segment is a normal segment requiring processing. If the segment is a dummy, then subroutine Clnxsg is called to reference the next segment and Procon is started again. If the PM has reached completion, a check is made whether the TM is multiprogrammed, and, if it is not, the file of pages resident in TM is cleared for the next PM. Then the PM is checked to see whether it had a dedicated bus, and, if so, an interrupt is filed to release the bus. A PM complete interrupt would then be listed, and the Mecint subroutine would be called to process these interrupts. If the segment is normal and requires processing, a check is made to see whether the system is paged and, if not, the Stexcn subroutine is called to start processing the segment. Otherwise a check is made for a page fault. If the page is already resident in TM (no page fault), Stexcn is called. In case of a page fault, a page fault interrupt is listed and Mecint is called to process it.



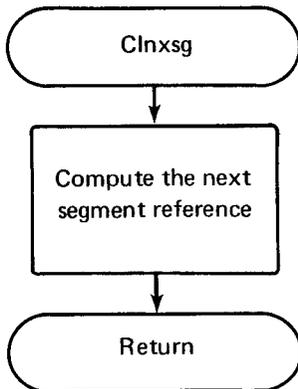


Fig. C18—Clnxsg. This is a subroutine which makes use of the segment referencing probabilities contained in the workload data to compute the next segment reference to occur in a PM's execution.

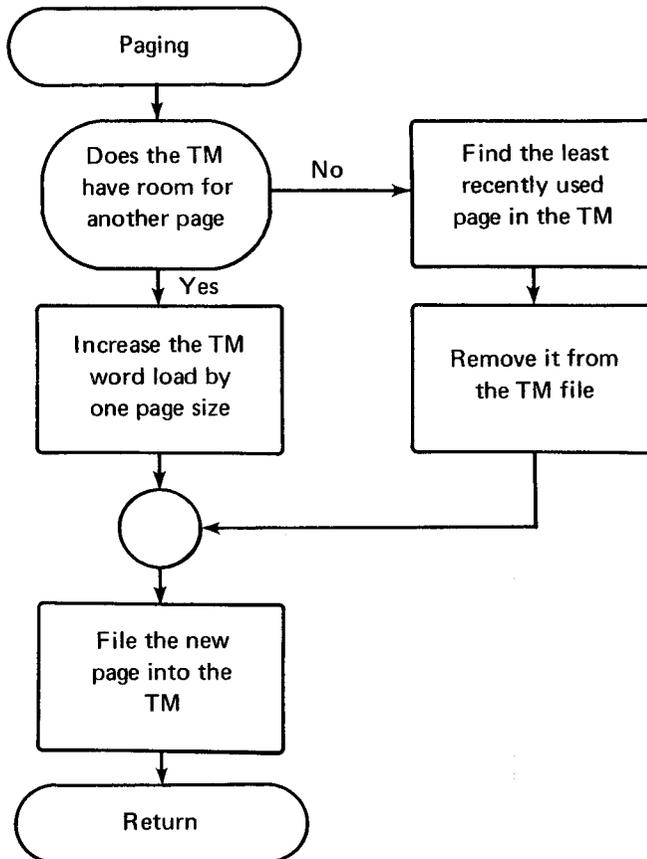
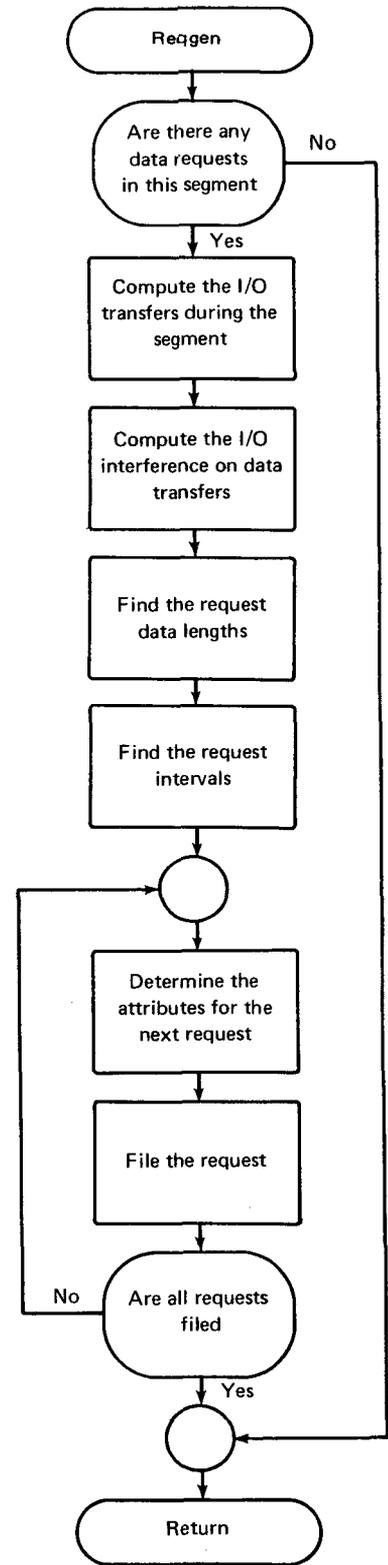


Fig. C19—Paging. This is a subroutine which updates a TM's file of resident pages whenever a page is loaded in. If the TM is not full, its contents are merely incremented by the size of the new page and the page is added to the file. If the TM is already full, the least recently used page is removed from the file and the new page is added.

Fig. C20—Reqgen. This is a subroutine which generates and files the set of data requests to be made by a program segment starting execution. If no data are associated with the segment, an exit is made immediately. Otherwise the delaying effect of I/O activity on the data transfers is computed and the data lengths, request intervals, and other attributes are obtained. The requests are then filed into a list and serviced, one at a time, over the processing time of the segment.



## APPENDIX D

### SIMULATION RESULTS DATA

Figures D1 through D57 display reproduced printouts of simulation results. The statistics produced at the end of a simulation run are the results of continuous compilation of system parameters over the elapsed simulation time. Data have been chosen for compilation and printout such that a meaningful assessment of system performance can be had without resorting to a detailed, step-by-step analysis of an event trace of the simulation run. CPU utilization figures used in the report are derived from the CPU assigned time, TM loading time, data transfer time, total MEC busy time, and the individual MEC routine times as given in the results.

In some simulations one or two PMs missed their completion deadlines a few times over the run. This occurred in systems where the workload and overhead kept CPU activity at close to 100 percent; occasional overruns become statistically possible in a very heavily loaded system. A PM which runs overdue in the simulated system is passed over for reinitialization at each clock time until it has completed processing. That is, its iteration sequence is merely shifted back in phase.

The excess of PM assignment routine activations over PM completions is due to attempts at assignment when resources are not available.

The behavior of the executive is indicated by the frequency and time usage of MEC interrupts and routines. Table D1 provides the key between the executive functions and the numbers used in the data printout to refer to them. Numbers 5, 6, and 7 represent PM reinitialization, PM assignment, and program transfer requests. These routines are not activated by interrupts but by other routines; hence no interrupts are associated with these functions. Interrupt processing takes precedence over executive routine processing and can break into a processing routine. The resulting routine idle time is given.

Total CPU assignment time as shown is taken from the end of each PM assignment routine to the end of the corresponding PM completion routine. This does not include the time consumed by the PM assignment routines, which time must be added on to obtain CPU utilization times as graphed in the report. CPU assignment time includes processing, transfers, and waiting on executive functions.

In a system with a floating executive sharing a CPU with the workload, the results give accumulated time that the executive breaks into the CPU activity which is effecting program processing and transfers.

Table D1  
Key to Executive Interrupt and Routine  
Headings in the Simulation Results  
Printouts

Number	Executive Function
1	Real time clock
2	External PM enable
3	Page fault
4	PM completion
5	PM reinitialization
6	PM assignment
7	Program transfer request
8	Program transfer completion
9	Data transfer request
10	Data transfer completion
11	Dedicated bus selection
12	Dedicated bus release

The data given on paging statistics at the end of the printouts shows the number of references to segments not resident in TM (page faults) and the number of references to a segment in a new page (page jump). This can be helpful in assessing the efficacy of various paging configurations.

Table D2 is an index to the printouts.

**Table D2**  
**Index to the Reproduced Printouts of the Simulation Results**

Figure	System and Workload Model Presented														
	1024- Word TM	2048- Word TM	3072- Word TM	4096- Word TM	Paged TM	Non- paged TM	Multi- programmed TM	Dedi- cated MEC	Floating MEC	Soft- ware MEC	Hard- ware MEC	3-msec Clock Inter- val	4-msec Clock Inter- val	Reduced PM Assign- ment	Shared Programs and Data Bus
<b>GE Workload on a Simplex Processor</b>															
D1				X		X		X		X					
D2				X		X			X	X					
D3	X				X			X		X					
D4	X				X				X	X					
D5	X				X		X	X		X					
D6	X				X		X	X		X					
D7			X		X		X		X	X					
D8				X		X		X		X		X			
D9				X		X		X		X		X			
D10				X		X		X		X				X	
<b>F-111 Workload on a Simplex Processor</b>															
D11				X		X		X		X					
D12				X		X			X	X					
D13	X				X			X		X					
D14	X				X				X	X					
D15	X									X					
D16	X				X		X	X	X	X					
D17			X		X		X	X	X	X					
D18				X	X	X	X	X	X	X			X		
D19				X	X	X	X	X	X	X			X		
D20				X		X		X		X				X	
<b>E-2B Workload on the Simplex Processor</b>															
D21				X		X		X		X					
D22				X		X			X	X					
D23	X				X			X		X					
D24	X				X				X	X					
D25	X				X		X	X	X	X					
D26	X				X		X	X	X	X					
D27			X		X		X		X	X					
D28				X		X		X		X			X		
D29				X		X		X		X			X		
D30				X		X		X		X				X	
<b>GE Workload on a Simplex Processor with an Abbreviated Run Time</b>															
D31				X		X			X	X					
D32	X				X				X	X					
D33			X		X		X		X	X					
<b>F-111 Workload on a Simplex Processor with an Abbreviated Run Time</b>															
D34				X		X			X	X					
D35	X				X				X	X					
D36			X		X		X		X	X					
<b>E-2B Workload on a Simplex Processor with an Abbreviated Run Time</b>															
D37				X		X			X	X					
D38	X				X				X	X					
D39			X		X		X		X	X					
<b>Expanded GE Workload on a Dual Processor</b>															
D40				X		X		X		X					
D41				X		X		X		X					X
D42	X				X			X		X					
D43	X				X			X		X					X
D44		X			X		X	X	X	X					
D45		X			X		X	X	X	X					X
D46				X	X		X	X	X	X					
D47				X	X		X	X	X	X					X
<b>Further Expanded GE Workload on a Triple Processor</b>															
D48				X		X		X		X					
D49				X		X		X		X					X
D50				X		X		X		X					
D51				X		X		X		X					X
D52	X				X			X		X					
D53	X				X			X		X					X
D54					X		X	X		X					
D55		X			X		X	X		X					X
D56		X			X		X	X		X					
D57				X	X		X	X		X					X

ELAPSED TIME = 1000000. USECS

TOTAL PMS ASSIGNED = 4366

PM	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
NUM	3334	500	200	100	100	40	40	10	8	7	18	1	1	1	1	1	1	1	1	1
NUM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MSC	2	19	49	59	58	202	189	915	82	76	84	9840	9794	9794	9794	9792	9791	9791	9789	9652
MSC	1	17	47	57	53	176	162	911	56	55	53	9840	9794	9794	9794	9792	9791	9791	9789	9652

INTERRUPT DATA

INT	1	2	3	4	5	6	7	8	9	10	11	12
NUM	10000	30	0	6728	0	0	0	6728	7911	7911	0	0
USC	6	22	0	5	2	11	5	4	4	4	0	0
USC	211	136	0	95	39	1007	61	98	110	113	0	0
MSC	400.0	1.8	0.0	100.9	190.4	1235.9	107.6	107.6	126.6	126.6	0.0	0.0
USC	0.8	1.4	0.0	0.0	1.1	2.2	0.0	0.4	0.0	0.1	0.0	0.0
USC	7	14	0	7	14	14	7	14	7	7	0	0

AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0.1 USECS  
 LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 21. USECS  
 TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 275156. USECS

MEC ROUTINE DATA

ROU	1	2	3	4	5	6	7	8	9	10	11	12
NUM	10000	30	0	6728	3733	10937	6728	6728	7911	7911	0	0
USC	6	22	0	5	2	11	5	4	4	4	0	0
USC	211	136	0	95	39	1007	61	98	110	113	0	0
MSC	400.0	1.8	0.0	100.9	190.4	1235.9	107.6	107.6	126.6	126.6	0.0	0.0
USC	0.8	1.4	0.0	0.0	1.1	2.2	0.0	0.4	0.0	0.1	0.0	0.0
USC	7	14	0	7	14	14	7	14	7	7	0	0

TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE = IN MSECS  
 AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS = IN USECS  
 LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS = IN USECS

CPU DATA

CPU 1

TOTAL TIME EACH CPU IS ASSIGNED = IN USECS  
 6171815.

TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 4611742. USECS

TOTAL TIME MEC WAS BUSY = 2672619. USEC  
 FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0.

NUMBER OF BORAM TO TASK MEMORY LOADS = 6728  
 TOTAL TIME SPENT LOADING TASK MEMORY = 268510. USECS

NUMBER OF DATA REQUESTS = 7911  
 TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 522549. USECS  
 TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 963945. USECS  
 TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 221026. USECS  
 LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 258. USECS

NUMBER OF SEGMENT REFERENCES = 2018  
 NUMBER OF PAGE FAULTS = 0  
 NUMBER OF PAGE JUMPS = 2018

Fig. D1--Simplex processor simulation results for the GE workload using a 4096-word nonpaged TM and a dedicated software MEC

```

ELAPSED TIME = 10000000; USECS

TOTAL PMS ASSIGNED = 4365

  PH   1   2   3   4   5   6   7   8   9  10  11  12  13  14  15  16  17  18  19  20
  NUM 3332 500 200 100 100 40  40  10  8  15  11  1  1  1  1  1  1  1  1  1
  NUMBER OF ITERATIONS OF EACH PH
  NUM 6  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0
  NUMBER OF TIMES EACH PH MISSED ITS COMPLETION DEADLINE
  MSC 2  16  48  49  48  194  185  908  77  84  77  9832  9768  9766  9762  9760  9759  9758  9757  9526
  AVERAGE TIME BY WHICH EACH PH BEAT ITS COMPLETION DEADLINE = IN MSECS
  MSC 0  16  43  46  41  162  155  903  48  49  42  9832  9768  9766  9762  9760  9759  9758  9757  9526
  SHORTEST TIME BY WHICH EACH PH BEAT ITS COMPLETION DEADLINE = IN MSECS

      INTERRUPT DATA
  INT  1  2  3  4  5  6  7  8  9  10  11  12
  NUM 10000 32  0  6776  0  0  0  6776  8009  8009  0  0
  AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0.1 USECS
  LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 21. USECS
  TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 277214, USECS

      MEC ROUTINE DATA
  ROU  1  2  3  4  5  6  7  8  9  10  11  12
  NUM 10000 32  0  6776  3737 10985  6776  6776  8009  8009  0  0
  AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE = IN USECS
  USC 6  12  0  3  3  13  4  7  4  5  0  0
  LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE = IN USECS
  USC 197 122  0  108  84  1058  61  112  121  112  0  0
  TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE = IN MSECS
  MSC 400,0 2,0  0,0 101,4 190,61241,3 108,4 108,4 128,1 128,1  0,0  0,0
  AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS = IN USECS
  USC 0,9 2,0  0,0  0,1  0,9  2,0  0,0  0,3  0,2  0,2  0,0  0,0
  LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS = IN USECS
  USC 14  7  0  7  14  14  7  7  7  7  0  0

      CPU DATA
  CPU  1
  TOTAL TIME EACH CPU IS ASSIGNED = IN USECS
  USC 7078200,
  TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 4612014, USECS

TOTAL TIME MEC WAS BUSY = 2685*18, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 897134,

NUMBER OF BORAM TO TASK MEMORY LOADS = 6776
TOTAL TIME SPENT LOADING TASK MEMORY = 275334, USECS

NUMBER OF DATA REQUESTS = 8009
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 524623, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 977013, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 224725, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 143, USECS

NUMBER OF SEGMENT REFERENCES = 2184
NUMBER OF PAGE FAULTS = 0
NUMBER OF PAGE JUMPS = 2184

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Fig. D2—Simplex processor simulation results for the GE workload using a 4096-word nonpaged TM and a Floating (shared) software MEC

ELAPSED TIME = 10000000; USECS

TOTAL PMS ASSIGNED = 4367

PM	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
NUM	3332	900	200	100	100	40	40	10	17	9	10	1	1	1	1	1	1	1	1	1
NUM	8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MSC	2	19	49	56	55	201	185	911	84	84	81	9835	9785	9785	9784	9782	9781	9781	9780	9621
MSC	0	17	46	54	50	173	158	906	55	52	50	9835	9785	9785	9784	9782	9781	9781	9780	9621

INTERRUPT DATA

INT	1	2	3	4	5	6	7	8	9	10	11	12
NUM	10000	33	8761	6729	0	0	0	8761	7915	7915	0	0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0.2 USECS												
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 21. USECS												
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 390798, USECS												

MEC ROUTINE DATA

ROU	1	2	3	4	5	6	7	8	9	10	11	12
NUM	10000	33	8761	6729	3737	10939	8761	8761	7915	7915	0	0
USC	10	22	5	5	2	13	0	5	8	2	0	0
USC	238	163	109	112	32	1034	40	150	112	103	0	0
MSC	400.0	2.0	43.8	100.9	190.6	1236.1	140.2	140.2	126.6	126.6	0.0	0.0
USC	0.8	1.5	0.0	0.0	0.8	2.5	0.1	0.2	0.0	0.1	0.0	0.0
USC	14	7	7	7	14	28	7	14	7	7	0	0

CPU DATA

CPU	1
USC	TOTAL TIME EACH CPU IS ASSIGNED = IN USECS 6410320.
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 4614958, USECS	

TOTAL TIME MEC WAS BUSY = 2897877, USEC

FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0.1

NUMBER OF BORAM TO TASK MEMORY LOADS = 8761

TOTAL TIME SPENT LOADING TASK MEMORY = 332918, USECS

NUMBER OF DATA REQUESTS = 7915

TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 523255, USECS

TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 981547, USECS

TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 252252, USECS

LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 168, USECS

NUMBER OF SEGMENT REFERENCES = 8761

NUMBER OF PAGE FAULTS = 8761

NUMBER OF PAGE JUMPS = 2032

Figure D3—Simplex processor simulation results for the GE workload using a 1024-word paged TM and a dedicated software MEC

```

ELAPSED TIME = 10000000, USECS

TOTAL PMS ASSIGNED = 4359

PM      1      2      3      4      5      6      7      8      9      10     11     12     13     14     15     16     17     18     19     20
NUM 3326 500 200 100 100 40 40 10 14 8 12 1 1 1 1 1 1 1 1 1
NUM 23 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
MSC 1 18 47 47 45 191 176 889 78 66 80 9768 9745 9740 9584 9579 9577 9576 9575 9308
MSC *1 15 38 44 37 158 91 838 46 42 40 9768 9745 9740 9584 9579 9577 9576 9575 9308

INTERRUPT DATA
INT      1      2      3      4      5      6      7      8      9      10     11     12
NUM 10000 32 8926 5770 0 0 0 8926 8003 8003 0 0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0,0 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 21, USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 354620, USECS

MEC ROUTINE DATA
RGU      1      2      3      4      5      6      7      8      9      10     11     12
NUM 10000 32 8926 5770 3751 10973 8926 8926 8003 8003 0 0
USC 9 20 5 4 5 14 0 5 4 6 0 0
USC 261 186 112 112 44 1054 40 150 145 107 0 0
MSC 400,0 2,0 44,6 101,6 191,31239,9 142,8 142,8 128,0 128,0 0,0 0,0
USC 1,2 0,7 0,0 0,0 1,5 2,1 0,1 0,2 0,2 0,0 0,0
USC 14 7 7 7 14 28 7 7 7 7 0 0

CPU DATA
CPU      1
USC 7470891,
TOTAL TIME EACH CPU IS ASSIGNED = IN USECS
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 4609862, USECS

TOTAL TIME MEC WAS BUSY = 2875730, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 1065630,

NUMBER OF BRAM TO TASK MEMORY LOADS = 8926
TOTAL TIME SPENT LOADING TASK MEMORY = 339188, USECS

NUMBER OF DATA REQUESTS = 8003
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 522059, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 980725, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 219656, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 177, USECS

NUMBER OF SEGMENT REFERENCES = 8926
NUMBER OF PAGE FAULTS = 8926
NUMBER OF PAGE JUMPS = 2156

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Fig. D4—Simplex processor simulation results for the GE workload using a 1024-word paged TM and a floating software MEC

ELAPSED TIME = 1000000. USECS

TOTAL PMS ASSIGNED = 4364

PM	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
NUM	3332	500	200	100	100	40	40	10	5	15	13	1	1	1	1	1	1	1	1	1
NUM	6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MSC	2	17	49	61	61	207	201	928	79	83	81	9852	9840	9796	9793	9791	9791	9788	9787	9642
MSC	0	17	46	59	54	176	175	924	59	56	54	9852	9840	9796	9793	9791	9791	9788	9787	9642

INTERRUPT DATA

INT	1	2	3	4	5	6	7	8	9	10	11	12
NUM	10000	30	2319	6775	0	0	0	2319	8007	8007	0	0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - 0.0 USECS												
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - 21. USECS												
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - 262199. USECS												

MEC ROUTINE DATA

ROU	1	2	3	4	5	6	7	8	9	10	11	12
NUM	10000	30	2319	6775	3756	10982	2319	2319	8007	8007	0	0
USC	7	4	3	1	11	0	4	4	3	0	0	0
USC	122	116	110	57	952	40	87	112	111	0	0	0
MSC	400.0	1.8	11.6	1.16	190.51241	0	37.1	37.1	128.1	128.1	0.0	0.0
USC	0.7	1.9	.1	0.1	0.8	1.1	0.3	0.5	0.1	0.1	0.0	0.0
USC	14	7	7	7	14	14	7	7	7	7	0	0

CPU DATA

CPU	1
USC	5908964.
TOTAL TIME EACH CPU IS ASSIGNED - IN USECS	
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - 4610610. USECS	

TOTAL TIME MEC WAS BUSY - 2539163. USEC

FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC - 0. U

NUMBER OF BORAM TO TASK MEMORY LOADS - 2319

TOTAL TIME SPENT LOADING TASK MEMORY - 88122. USECS

NUMBER OF DATA REQUESTS - 8007

TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY - 524591. USECS

TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED - 961903. USECS

TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES - 222234. USECS

LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 172. USECS

NUMBER OF SEGMENT REFERENCES - 8957

NUMBER OF PAGE FAULTS - 2319

NUMBER OF PAGE JUMPS - 2182

Fig. D5—Simplex processor simulation results for the GE workload using a 1024-word paged multiprogrammed TM and a dedicated software MEC

```

ELAPSED TIME = 10000000. USECS

TOTAL PMS ASSIGNED = 4358

PM      1   2   3   4   5   6   7   8   9  10  11  12  13  14  15  16  17  18  19  20
NUM 3324 900 200 100 100 40 40 10 11 11 13 1 1 1 1 1 1 1 1 1
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
NUM 27 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC 2 19 49 54 53 198 191 915 77 85 80 9838 9773 9770 9767 9761 9760 9759 9757 9523
SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC -1 16 46 52 46 168 160 909 53 50 48 9838 9773 9770 9767 9761 9760 9759 9757 9523

      INTERRUPT DATA
INT      1   2   3   4   5   6   7   8   9  10  11  12
NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
NUM 10000 34 2247 6769 0 0 0 2247 8003 8003 0 0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - 0.0 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - 21. USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - 261121. USECS

      MEC ROUTINE DATA
ROU      1   2   3   4   5   6   7   8   9  10  11  12
NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
NUM 10000 34 2247 6769 3748 10972 2247 2247 8003 8003 0 0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC 3 20 3 3 2 12 0 6 3 3 0 0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC 197 122 112 110 61 1003 40 129 110 127 0 0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
MSC 400.0 2.1 11.2 101.5 191.11239.8 36.0 36.0 128.0 128.0 0.0 0.0
AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC 0.8 1.6 0.1 0.2 0.6 0.8 0.3 0.6 0.1 0.1 0.0 0.0
LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC 14 7 7 7 14 14 7 7 7 7 0 0

      CPU DATA
CPU      1
TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
USC 6607624.
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - 4600810. USECS

TOTAL TIME MEC WAS BUSY - 2534949. USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC - 717816.

NUMBER OF BORAM TO TASK MEMORY LOADS - 2247
TOTAL TIME SPENT LOADING TASK MEMORY - 85386. USECS

NUMBER OF DATA REQUESTS - 8003
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY - 523039. USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED - 950130. USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES - 215674. USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 140. USECS

NUMBER OF SEGMENT REFERENCES - 8939
NUMBER OF PAGE FAULTS - 2247
NUMBER OF PAGE JUMPS - 2170

```

Fig. D6—Simplex processor simulation results for the GE workload using a 1024-word paged multiprogrammed TM and a floating software MEC

```

ELAPSED TIME = 1000000, USECS

TOTAL PMS ASSIGNED = 4349

PM   1   2   3   4   5   6   7   8   9  10  11  12  13  14  15  16  17  18  19  20
NUM 3325 500 200 100 100 40  40  10  11  9   5   1   1   1   1   1   1   1   1   1
NUMBER OF ITERATIONS OF EACH PM

NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
NUM  22   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0
AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC  2  19  49  55  54 199 194 918  80  81  71 9837 9770 9767 9765 9761 9760 9759 9758 9524
SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC -1  16  45  51  45 167 161 910  52  49  47 9837 9770 9767 9765 9761 9760 9759 9758 9524

      INTERRUPT DATA
INT   1   2   3   4   5   6   7   8   9  10  11  12
NUM 100.0 23  846 6760  0   0   0   0  846 7984 7984  0   0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE =  0.0 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE =  21. USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 241101, USECS

      MEC ROUTINE DATA
ROU   1   2   3   4   5   6   7   8   9  10  11  12
NUM 100.0 23  846 6760 3758 10953  846  846 7984 7984  0   0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC  2  23  4  2  1  14  0  6  3  3  0  0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC 197 122  99 110  76 1019  40  87 109 106  0  0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
MSC 400.0 1.4  4.2 101.4 191.7 1237.7 13.5 13.5 127.7 127.7  0.0  0.0
AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC  0.7  2.7  0.1  0.2  0.6  0.7  0.1  0.2  0.2  0.1  0.0  0.0
LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC  14  7  7  7  14  14  7  7  7  7  0  0

      CPU DATA
CPU   1
USC  TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
      6424238.
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 4602776, USECS

TOTAL TIME MEC WAS BUSY - 2460041, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 642740.

NUMBER OF BORAM TO TASK MEMORY LOADS = 846
TOTAL TIME SPENT LOADING TASK MEMORY = 32148, USECS

NUMBER OF DATA REQUESTS = 7984
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 922076, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 947938, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 211261, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 139, USECS

NUMBER OF SEGMENT REFERENCES = 8902
NUMBER OF PAGE FAULTS = 846
NUMBER OF PAGE JUMPS = 2142
    
```

Fig. D7—Simplex processor simulation results for the GE workload using a 3072-word paged multiprogrammed TM and a floating software MEC

```

ELAPSED TIME = 10002000, USECS

TOTAL PMS ASSIGNED = 4336

PM      1    2    3    4    5    6    7    8    9    10   11   12   13   14   15   16   17   18   19   20
NUM  3334 477 197  98  98  40  10  9  15  9  1  1  1  1  1  1  1  1  1  1
NUMBER OF ITERATIONS OF EACH PM

NUM      0    0    0    0    0    0    0    0    0    0    0    0    0    0    0    0    0    0    0    0
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE

MSC      3    20   50   59   60  214  200  987  91  87  86  9852  9843  9843  9798  9798  9797  9796  9795  9706
AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS

MSC      3    20   50   57   55  178  175  922  61  56  55  9852  9843  9843  9798  9798  9797  9796  9795  9706
SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS

INTERRUPT DATA

INT      1    2    3    4    5    6    7    8    9    10   11   12
NUM  3334  30  0  6711  0  0  0  6712  7918  7918  0  0
NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC

AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0.0 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 14. USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 228361. USECS

MEC ROUTINE DATA

ROU      1    2    3    4    5    6    7    8    9    10   11   12
NUM  3334  30  0  6711  3333 10893  6712  6712  7918  7918  0  0
NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED

USC      3    19  0  2  1  16  1  8  2  2  0  0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS

USC     109  136  0  111  32  514  61  119  113  103  0  0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS

MSC     133.4  1.8  0.0 100.7 170.0 1230.9 107.4 107.4 126.7 126.7 0.0 0.0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS

USC      0.4  1.4  0.0  0.0  1.0  0.9  0.0  0.2  0.0  0.0  0.0  0.0
AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS

USC      7    7    0  14  14  14  7  7  7  7  0  0
LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS

CPL DATA

CFU      1
TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
USC     6039947.
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 4568298. USECS

TOTAL TIME MEC WAS BUSY - 233268. USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0.1

NUMBER OF BORAM TO TASK MEMORY LOADS = 6712
TOTAL TIME SPENT LOADING TASK MEMORY = 272040. USECS

NUMBER OF DATA REQUESTS = 7919
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 518459. USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 923018. USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 203913. USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 234. USECS

NUMBER OF SEGMENT REFERENCES = 2157
NUMBER OF PAGE FAULTS = 0
NUMBER OF PAGE JUMPS = 2157

```

Fig. D8—Simplex processor simulation results for the GE workload using a 4096-word nonpaged TM, a dedicated software MEC, and a 3-msec clock interval

ELAPSED TIME = 10002000, USECS

TOTAL PMS ASSIGNED = 4335

PM	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
NUM	3334	471	197	98	98	40	40	10	9	13	10	1	1	1	1	1	1	1	1	1
NUM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MSC	3	19	49	54	53	210	189	982	88	89	87	9840	9780	9780	9777	9774	9773	9772	9771	9610
MSC	3	17	47	51	49	169	163	913	52	52	49	9840	9780	9780	9777	9774	9773	9772	9771	9610

INTERRUPT DATA

INT	1	2	3	4	5	6	7	8	9	10	11	12
NUM	3334	29	0	6710	0	0	0	6711	7916	7916	0	0
USC	4	14	0	3	2	14	1	7	2	2	0	0
MSC	1.9	159	0	109	32	514	61	116	125	104	0	0
MSC	133.4	1.8	0.0	100.7	170.0	1230.7	107.4	107.4	126.7	126.7	0.0	0.0
USC	0.3	0.7	0.0	0.0	1.1	0.9	0.0	0.4	0.0	0.0	0.0	0.0
USC	14	7	0	7	14	21	7	7	7	7	0	0

MEC ROUTINE DATA

ROU	1	2	3	4	5	6	7	8	9	10	11	12
NUM	3334	29	0	6710	3333	10891	6711	6711	7916	7916	0	0
USC	4	14	0	3	2	14	1	7	2	2	0	0
MSC	1.9	159	0	109	32	514	61	116	125	104	0	0
MSC	133.4	1.8	0.0	100.7	170.0	1230.7	107.4	107.4	126.7	126.7	0.0	0.0
USC	0.3	0.7	0.0	0.0	1.1	0.9	0.0	0.4	0.0	0.0	0.0	0.0
USC	14	7	0	7	14	21	7	7	7	7	0	0

CPU DATA

CPU	1
USC	0.662121.
USC	4667546, USECS

TOTAL TIME MEC WAS BUSY - 2332821, USEC

FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC - 612693. U

NUMBER OF BORAM TO TASK MEMORY LOADS = 6711

TOTAL TIME SPENT LOADING TASK MEMORY = 271662, USECS

NUMBER OF DATA REQUESTS = 7917

TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 517751, USECS

TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 920417, USECS

TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 201301, USECS

LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 285, USECS

NUMBER OF SEGMENT REFERENCES = 2147

NUMBER OF PAGE FAULTS = 0

NUMBER OF PAGE JUMPS = 2147

Fig. D9—Simplex processor simulation results for the GE workload using a 4096-word nonpaged TM, a floating software MEC, and a 3-msec clock interval

```

ELAPSED TIME = 10:00000. USECS

TOTAL PMS ASSIGNED = 4370

PM      1    2    3    4    5    6    7    8    9    10   11   12   13   14   15   16   17   18   19   20
NUM 3334 500 200 100 100 40 40 10 14 11 12 1 1 1 1 1 1 1 1 1
NUMBER OF ITERATIONS OF EACH PM
NUM      0    0    0    0    0    0    0    0    0    0    0    0    0    0    0    0    0    0    0    0
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
MSC      2   19   49   52   51  197  190  914   89   79   78 9838 9780 9777 9774 9773 9772 9771 9769 9610
AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC      1   17   46   51   45  167  161  909   50   48   46 9838 9780 9777 9774 9773 9772 9771 9769 9610
SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS

      INTERRUPT DATA
INT      1    2    3    4    5    6    7    8    9    10   11   12
NUM 10000 35 0 6781 0 0 0 6781 8017 8017 0 0
NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - 0.0 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - 21. USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - 277417. USECS

      MEC ROUTINE DATA
RGU      1    2    3    4    5    6    7    8    9    10   11   12
NUM 10000 35 0 6781 3733 8387 6781 6781 8017 8017 0 0
NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC      7   13  0  1  3  6  3  4  1  1  0  0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC     234 159  0  51  32  424  61  90  94  97  0  0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
MSC     40.0 2.1  .0 11.7 190.4 947.7 108.5 108.5 128.3 128.3 0.0 0.0
AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC     .7  1.2  .0  0.1  1.5  1.6  0.0  0.2  0.1  0.1  0.0  0.0
LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC     14  14  0  7  14  28  7  7  7  7  0  0

      CPU DATA
CPU      1
USC
TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - 4616362. USECS

TOTAL TIME MEC WAS BUSY - 2392917. USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC - 671930.

NUMBER OF BORAM TO TASK MEMORY LOADS - 6781
TOTAL TIME SPENT LOADING TASK MEMORY - 275062. USECS

NUMBER OF DATA REQUESTS - 8017
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY - 523433. USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED - 923408. USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES - 200272. USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 125. USECS

NUMBER OF SEGMENT REFERENCES - 2174
NUMBER OF PAGE FAULTS - 0
NUMBER OF PAGE JUMPS - 2174

```

Fig. D10—Simplex processor simulation results for the GE workload using a 4096-word nonpaged TM, a floating software MEC, and reduced PM assignment activity

```

ELAPSED TIME = 1000000. USECS

TOTAL PMS ASSIGNED = 1396

P# 1 2 3 4 5 6 7 8 9 10 11
NUM NUMBER OF ITERATIONS OF EACH P#
1250 40 5 17 54 5 5 5 5 5 5
NUM NUMBER OF TIMES EACH P# MISSED ITS COMPLETION DEADLINE
1 0 0 0 0 0 0 0 0 0 0
M#C AVERAGE TIME BY WHICH EACH P# BEAT ITS COMPLETION DEADLINE - IN MSECS
6 247 1849 40 18 1833 1839 1842 1849 1343 1843
M#C SHORTEST TIME BY WHICH EACH P# BEAT ITS COMPLETION DEADLINE - IN MSECS
3 246 1830 40 17 1832 1837 1841 1843 1838 1839

INTERRUPT DATA
INT 1 2 3 4 5 6 7 8 9 10 11 12
NUM NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
10000 69 0 1551 1282 2917 1551 1551 3126 3126 0 0
M#C AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - IN USECS
0.5
M#C LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - IN USECS
13
M#C TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - IN USECS
135961

MEC ROUTINE DATA
R# 1 2 3 4 5 6 7 8 9 10 11 12
NUM NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
10000 69 0 1551 1282 2917 1551 1551 3126 3126 0 0
M#C AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
0 1 0 23 0 2 1 6 7 0 0 0
M#C LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
109 66 0 109 16 401 91 103 107 95 0 0
M#C TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
400,0 4,2 0,0 23,3 65,4 329,6 24,8 24,8 50,0 50,0 0,0 0,0
M#C AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
0,8 0,5 0,0 0,0 0,1 0,3 0,0 0,0 0,0 0,0 0,0 0,0
M#C LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
14 7 0 7 7 14 7 7 7 0 0 0

CPU DATA
CPU 1
M#C TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
183871.
M#C TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - IN USECS
1065825.

TOTAL TIME MEC WAS BUSY - 1108102. USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC * TOTAL TIME PMS WERE INTERRUPTED BY THE MEC * 0.

NUMBER OF BURHM IO TASK MEMORY LOADS - 1551
TOTAL TIME SPENT LOADING TASK MEMORY - 236000. USECS

NUMBER OF DATA REQUESTS - 3126
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY - 252659. USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED * 429678. USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES * 103201. USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE * 139. USECS

NUMBER OF SEQUENTIAL REFERENCES - 7308
NUMBER OF PAGE FAULTS - 0
NUMBER OF PAGE JUMPS - 3451
    
```

Fig. D11—Simplex processor simulation results for the F-111 workload using a 4096-word nonpaged TM and a dedicated software MEC

```

ELAPSED TIME = 1000000, USECS

TOTAL PMS ASSIGNED = 1384

PM      1      2      3      4      5      6      7      8      9     10     11
NUMBER OF ITERATIONS OF EACH PM
NUM 1250  40  5  16  43  5  5  5  5  5  5

NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
NUM 0  0  0  0  0  0  0  0  0  0  0

AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC 6  244 1827  47  18 1832 1833 1835 1835 1830 1829

SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC 3  240 1822  46  17 1830 1832 1833 1833 1826 1824

INTERRUPT DATA

INT      1      2      3      4      5      6      7      8      9     10     11     12
NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
NUM 10000  58  0 1539  0  0  0  0 1539 3108 3108  0  0

AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0.5 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 12. USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 135464, USECS

MEC ROUTINE DATA

ROU      1      2      3      4      5      6      7      8      9     10     11     12
NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
NUM 10000  58  0 1539 1279 2894 1539 1539 3108 3108  0  0

AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC 0  3  0  0  0  2  0  6  7  0  0  0

LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC 14  54  0  82  16  401  40  98  86  91  0  0

TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
MSC 40000  3.5  1.0 23.1 65.2 327.0 24.6 24.6 49.7 49.7 0.0 0.0

AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC 0.1 1.1 0.0 0.1 0.0 0.3 0.1 0.0 0.0 0.1 0.0 0.0

LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC 14  14  0  7  7  14  7  7  7  7  0  0

CPU DATA

CPU      1
TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
USC 1969227.

TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 1061340, USECS

TOTAL TIME MEC WAS BUSY - 1103042, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 182057, U

NUMBER OF BORAH TO TASK MEMORY LOADS = 1539
TOTAL TIME SPENT LOADING TASK MEMORY = 236175, USECS

NUMBER OF DATA REQUESTS = 3108
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 291586, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 428744, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 103056, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 139, USECS

NUMBER OF SEGMENT REFERENCES = 7306
NUMBER OF PAGE FAULTS = 0
NUMBER OF PAGE JUMPS = 3452

```

Fig. D12—Simplex processor simulation results for the F-111 workload using a 4096-word nonpaged TM and a floating software MEC

ELAPSED TIME = 10000000, USECS

TOTAL PMS ASSIGNED = 1390

PH	1	2	3	4	5	6	7	8	9	10	11
NUM	1249	40	5	17	49	5	5	5	5	5	5
NUM	2	0	0	0	0	0	0	0	0	0	0
MSC	6	249	1833	47	18	1835	1839	1842	1842	1835	1834
MSC	-5	246	1823	46	12	1832	1837	1840	1836	1822	1823

INTERRUPT DATA

INT	1	2	3	4	5	6	7	8	9	10	11	12
NUM	10000	64	4699	1543	0	0	0	4699	3130	3130	0	0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0,3 USECS												
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 9, USECS												
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 190869, USECS												

MEC ROUTINE DATA

ROU	1	2	3	4	5	6	7	8	9	10	11	12
NUM	10000	64	4699	1543	1286	2905	4699	4699	3130	3130	0	0
USC	0	2	0	9	0	2	0	2	8	1	0	0
USC	108	35	107	48	21	436	40	82	111	95	0	0
MSC	400,0	3,9	23,5	23,2	65,6	328,3	75,2	75,2	50,1	50,1	0,0	0,0
USC	0,9	1,1	0,0	0,0	0,2	0,4	0,0	1,8	0,0	0,0	0,0	0,0
USC	14	14	7	7	7	14	7	7	7	7	0	0

CPU DATA

CPU	1
USC	1881147
TOTAL TIME EACH CPU IS ASSIGNED = IN USECS	
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 1082969, USECS	

TOTAL TIME MEC WAS BUSY = 1285822, USEC

FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0,

NUMBER OF BORAM TO TASK MEMORY LOADS = 4699

TOTAL TIME SPENT LOADING TASK MEMORY = 178562, USECS

NUMBER OF DATA REQUESTS = 3130

TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 292483, USECS

TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 434277, USECS

TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 106294, USECS

LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 215, USECS

NUMBER OF SEGMENT REFERENCES = 8864

NUMBER OF PAGE FAULTS = 4699

NUMBER OF PAGE JUMPS = 3507

Fig. D13—Simplex processor simulation results for the F-111 workload using a 1024-word paged TM and a dedicated software MEC

```

ELAPSED TIME = 1000000, USECS

TOTAL PMS ASSIGNED = 1398

PH  1  2  3  4  5  6  7  8  9  10  11
NUM 1250 40  5  19  54  5  5  5  5  5  5
NUM 0  0  0  0  0  0  0  0  0  0  0
MSC 6  249 1811  47  17 1833 1834 1833 1824 1817 1813
MSC 2  246 1804  46  15 1830 1837 1832 1820 1812 1806

AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE = IN MSECS
SMORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE = IN MSECS

INTERRUPT DATA
INT  1  2  3  4  5  6  7  8  9  10  11  12
NUM 10000  72  4719 1553  0  0  0  4719 3146 3146  0  0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0,3 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 8, USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 191485, USECS

MEC ROUTINE DATA
RQU  1  2  3  4  5  6  7  8  9  10  11  12
NUM 10000  72  4719 1553 1279 2922 4719 4719 3146 3146  0  0
USC 0  3  1  1  0  2  0  2  8  0  0  0
MSC 118 108 108 90  21  436  40  82  112  158  0  0
USC 400,0  4,4  23,6  23,6  65,2  330,2  75,5  75,5  50,3  50,3  0,0  0,0
USC 0,2  0,8  0,0  0,0  0,1  0,4  0,0  1,8  0,0  0,0  0,0  0,0
USC 14  14  7  7  7  14  7  7  7  7  0  0

CPL DATA
CPU  1
USC 2170641,
TOTAL TIME EACH CPU IS ASSIGNED = IN USECS
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 108652, USECS

TOTAL TIME MEC WAS BUSY = 1289A62, LSEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 29362A, 1

NUMBER OF BORAM TO TASK MEMORY LOADS = 4719
TOTAL TIME SPENT LOADING TASK MEMORY = 179322, USECS

NUMBER OF DATA REQUESTS = 314A
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 253251, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 437183, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 108680, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 241, USECS

NUMBER OF SEGMENT REFERENCES = 8867
NUMBER OF PAGE FAULTS = 4719
NUMBER OF PAGE JUMPS = 3511
UTILITY
EXECUTION STARTED AT 1234 +30

```

Fig. D14—Simplex processor simulation results for the F-111 workload using a 1024-word paged TM and a floating software MEC

ELAPSED TIME = 10000000. USECS

TOTAL PMS ASSIGNED = 1404

PM	1	2	3	4	5	6	7	8	9	10	11
NUMBER OF ITERATIONS OF EACH PM	1250	40	5	27	52	5	5	5	5	5	5
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE	0	0	0	0	0	0	0	0	0	0	0
AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS	7	249	1837	48	18	1835	1841	1844	1844	1838	1838
SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS	3	246	1834	46	15	1832	1839	1841	1840	1836	1834

INTERRUPT DATA

INT	1	2	3	4	5	6	7	8	9	10	11	12
NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC	10000	77	1342	1559	0	0	0	1342	3158	3158	0	0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE -	0.1 USECS											
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE -	14. USECS											
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS -	144452. USECS											

MEC ROUTINE DATA

RQU	1	2	3	4	5	6	7	8	9	10	11	12
NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED	10000	77	1342	1559	1279	2933	1342	1342	3158	3158	0	0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS	0	4	2	0	0	2	0	2	2	0	0	0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS	107	104	100	81	21	385	40	82	113	108	0	0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS	400.0	4.7	6.7	23.4	65.2	331.4	21.5	21.5	50.5	50.5	0.0	0.0
AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS	0.2	1.0	0.0	0.0	0.1	0.4	0.2	0.9	0.0	0.0	0.0	0.0
LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS	14	7	7	7	7	14	7	14	7	7	0	0

CPU DATA

CPU	1
TOTAL TIME EACH CPU IS ASSIGNED - IN USECS	1630439.
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS -	1092108. USECS

TOTAL TIME MEC WAS BUSY - 1119902. USEC

FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0.

NUMBER OF BORAM TO TASK MEMORY LOADS - 1342

TOTAL TIME SPENT LOADING TASK MEMORY - 50996. USECS

NUMBER OF DATA REQUESTS - 3158

TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY - 254321. USECS

TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED - 410830. USECS

TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES - 81286. USECS

LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 189. USECS

NUMBER OF SEGMENT REFERENCES - 8861

NUMBER OF PAGE FAULTS - 1342

NUMBER OF PAGE JUMPS - 3499

Fig. D15—Simplex processor simulation results for the F-111 workload using a 1024-word paged multiprogrammed TM and a dedicated software MEC

```

ELAPSED TIME = 1000000. USECS

TOTAL PMS ASSIGNED = 1394

PM      1      2      3      4      5      6      7      8      9      10     11
NUMBER OF ITERATIONS OF EACH PM
NUM 1750  40   5   20  49   5   5   5   5   5   5
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
NUM   0   0   0   0   0   0   0   0   0   0   0
AVERAGE TIME BY WHICH EACH PM MET ITS COMPLETION DEADLINE - IN MSEC
MSC   7  249 1818  48  18 1833 1836 1838 1828 1820 1819
SHORTEST TIME BY WHICH EACH PM MET ITS COMPLETION DEADLINE - IN MSEC
MSC   2  246 1809  44  15 1830 1834 1835 1827 1818 1810

      INTERRUPT DATA
INT      1      2      3      4      5      6      7      8      9      10     11     12
NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
NUM 10000  68 1331 1549   0   0   0 1331 3130 3130  0   0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - 0.1 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - 12. USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 143773. USECS

      MEC ROUTINE DATA
ROI      1      2      3      4      5      6      7      8      9      10     11     12
NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
NUM 10000  68 1331 1549 1279 2914 1331 1331 3130 3130  0   0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC   0   3   3   0   0   2   0   3   2   0   0   0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC 118  76 104  55  21  385  40  82 113 112  0   0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSEC
MSC 400.0  4.1  6.7 23.2 65.2 329.3 21.3 21.3 50.1 50.1 0.0 0.0
AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC  0.1  1.3  0.0  0.0  0.1  0.4  0.1  0.9  0.0  0.1  0.0  0.0
LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC   7   7   7   7   7  14   7  14   7   7   0   0

      CPU DATA
CPU      1
TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
USC 1772399.
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 1075488. USECS

TOTAL TIME MEC WAS BUSY = 1115074. USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC =
                                                                 110308. USEC

NUMBER OF RORAM TO TASK MEMORY LOADS = 1331
TOTAL TIME SPENT LOADING TASK MEMORY = 50578. USECS

NUMBER OF DATA REQUESTS = 3130
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 243016. USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 409328. USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 82003. USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 266. USECS

NUMBER OF SEGMENT REFERENCES = 8831
NUMBER OF PAGE FAULTS = 1331
NUMBER OF PAGE JUMPS = 3477

```

Fig. D16—Simplex processor simulation results for the F-111 workload using a 1024-word paged multiprogrammed TM and a floating software MEC

ELAPSED TIME = 1000000, USECS

TOTAL PMS ASSIGNED = 1400

PM	1	2	3	4	5	6	7	8	9	10	11
NUMBER OF ITERATIONS OF EACH PM	40	5	23	52	5	5	5	5	5	5	5
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE	0	0	0	0	0	0	0	0	0	0	0
AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS	7	249	1835	48	18	1834	1838	1841	1844	1837	1837
SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS	3	246	1833	46	13	1831	1835	1839	1843	1835	1834

INTERRUPT DATA

INT	1	2	3	4	5	6	7	8	9	10	11	12
NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC	100	74	192	1555	0	0	0	192	3148	3148	0	0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE -	0,0 USECS											
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE -	7, USECS											
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS -	128163, USECS											

MEC ROUTINE DATA

ROU	1	2	3	4	5	6	7	8	9	10	11	12
NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED	100	74	192	1555	1279	2926	192	192	3148	3148	0	0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS	0	3	3	0	0	2	0	3	1	0	0	0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS	1,8	59	107	55	61	385	40	75	113	73	0	0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS	406,0	4,5	1,0	23,3	65,2	330,6	3,1	3,1	50,4	50,4	0,0	0,0
AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS	0,1	1,2	0,0	0,0	0,0	0,3	0,2	0,3	0,0	0,0	0,0	0,0
LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS	14	7	7	7	7	7	7	7	7	7	0	0

CPU DATA

CPU 1

USC TOTAL TIME EACH CPU IS ASSIGNED - IN USECS  
1638132,

TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - 1087154, USECS

TOTAL TIME MEC WAS BUSY - 1059709, USEC

FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC - 67542, U

NUMBER OF BORAM TO TASK MEMORY LOADS - 192

TOTAL TIME SPENT LOADING TASK MEMORY - 7296, USECS

NUMBER OF DATA REQUESTS - 3148

TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY - 253967, USECS

TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED - 405130, USECS

TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES - 77162, USECS

LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 222, USECS

NUMBER OF SEGMENT REFERENCES - 8867

NUMBER OF PAGE FAULTS - 192

NUMBER OF PAGE JUMPS - 3507

UTILITY

EXECUTION STARTED AT 1124 -18

Fig. D17—Simplex processor simulation results for the F-111 workload using a 3072-word paged multiprogrammed TM and a floating software MEC

```

ELAPSED TIME = 10000000, USECS

TOTAL PMS ASSIGNED = 1394

PH  1  2  3  4  5  6  7  8  9  10  11
NUM 1250 40  5  22  47  5  5  5  5  5  5
    NUMBER OF ITERATIONS OF EACH PM
NUM  0  0  0  0  0  0  0  0  0  0  0
    NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
MSC  7  249 1844  48  18 1835 1842 1843 1850 1846 1844
    AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC  4  246 1840  46  18 1832 1840 1841 1845 1844 1840
    SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS

    INTERRUPT DATA
INT  1  2  3  4  5  6  7  8  9  10  11  12
NUM 2500 67  0 1549  0  0  0 1549 3129 3129  0  0
    NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
    AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0,8 USECS
    LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 13, USECS
    TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 83461, USECS

    MEC ROUTINE DATA
RBU  1  2  3  4  5  6  7  8  9  10  11  12
NUM 2500 67  0 1549 1269 2913 1549 1549 3129 3129  0  0
    NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
    AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
    USC  0  3  0  0  0  0  0  0  6  8  0  0
    LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
    USC 112 88  0 108 61 310 61 84 110 109  0  0
    TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
    MSC 100,0 4,1 0,0 23,2 64,7 329,2 24,8 24,8 50,1 50,1 0,0 0,0
    AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
    USC 0,1 0,2 0,0 0,0 0,1 0,1 0,0 0,0 0,0 0,0 0,0 0,0
    LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
    USC  7  7  0  7  7  14  7  7  7  0  0  0

    CPU DATA
CPU  1
    TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
    USC 1802639.
    TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 1077335, USECS

    TOTAL TIME MEC WAS BUSY = 754367, USEC
    FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0,
    NUMBER OF BORAM TO TASK MEMORY LOADS = 1549
    TOTAL TIME SPENT LOADING TASK MEMORY = 237417, USECS

    NUMBER OF DATA REQUESTS = 3129
    TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 252872, USECS
    TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 428003, USECS
    TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 102449, USECS
    LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 139, USECS

    NUMBER OF SEGMENT REFERENCES = 7346
    NUMBER OF PAGE FAULTS = 0
    NUMBER OF PAGE JUMPS = 3488

```

Fig. D18—Simplex processor simulation results for the F-111 workload using a 4096-word nonpaged TM, a dedicated software MEC, and a 4-msec clock interval

```

ELAPSED TIME = 1000000, USECS

TOTAL PMS ASSIGNED = 1405

PM  1  2  3  4  5  6  7  8  9  10  11
NUM 125 40 5 25 55 5 5 5 5 5 5
    NUMBER OF ITERATIONS OF EACH PM
NUM  0  0  0  0  0  0  0  0  0  0  0
    NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
MSC  7 249 1834 48 18 1835 1839 1841 1843 1837 1836
    AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC  4 246 1828 46 16 1832 1836 1841 1841 1836 1828
    SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS

    INTERRUPT DATA
INT  2  3  4  5  6  7  8  9  10  11  12
NUM 25  78  0 1560  0  0  0 1560 3158 3158  0  0
    NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
    AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0,7 USECS
    LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 7, USECS
    TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 84098, USECS

    MEC ROUTINE DATA
ROU  1  2  3  4  5  6  7  8  9  10  11  12
NUM 25  78  0 1560 1269 2935 1560 1560 3158 3158  0  0
    NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
    AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC  1  0  0  0  0  1  0  6  6  0  0  0
    LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC  1,7 37  0 93 16 242 40 69 105 91  0  0
    TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
MSC  4,8  0 23,4 64,7 331,7 29,0 29,0 90,5 90,5 0,0 0,0
    AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC  0,1 1,3  0 0,0 0,0 0,1 0,0 0,0 0,0 0,0 0,0 0,0
    LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC  7 14  0 7 7 14 7 7 7 7  0  0

    CPU DATA
CPU  1
USC  1920979
    TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
    TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 1093753, USECS

TOTAL TIME MEC WAS BUSY = 759606, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 97325, U

NUMBER OF BORAM TO TASK MEMORY LOADS = 1560
TOTAL TIME SPENT LOADING TASK MEMORY = 239,10, USECS

NUMBER OF DATA REQUESTS = 3158
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 254036, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 430811, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 103253, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 242, USECS

NUMBER OF SEGMENT REFERENCES = 7354
NUMBER OF PAGE FAULTS = 0
NUMBER OF PAGE JUMPS = 3498
    
```

Fig. D19—Simplex processor simulation results for the F-111 workload using a 4096-word nonpaged TM, a floating software MEC, and a 4-msec clock interval

```

ELAPSED TIME = 10000000, USECS

TOTAL PMS ASSIGNED = 1401

PM      1      2      3      4      5      6      7      8      9      10     11
NUMBER OF ITERATIONS OF EACH PM
NUM 1250  40   5   19  57   5   5   5   5   5   5
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
NUM      0      0      0      0      0      0      0      0      0      0      0
MSC AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
      6 249 1827  47  18 1833 1836 1837 1838 1832 1828
MSC SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
      2 245 1824  45  13 1830 1833 1835 1836 1829 1825

      INTERRUPT DATA
INT      1      2      3      4      5      6      7      8      9      10     11     12
NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
NUM 10000  75   0 1556   0   0   0 1556 3156 3156   0   0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - 0.5 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - 11. USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - 136493, USECS

      MEC ROUTINE DATA
RBU      1      2      3      4      5      6      7      8      9      10     11     12
NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
NUM 10000  75   0 1556 1279 2781 1556 1556 3156 3156   0   0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC      0      2      0      0      0      0      0      1      6      6      0   0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC      94     97     0     45     16    129     61     54     63    115     0   0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
MSC 400.0  4.6   .0 23.3 69.2 314.3 24.9 24.9 50.5 50.5   0.0  0.0
AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC  0.1  0.6   .0  0.0  0.1  0.2  0.0  0.0  0.0  0.1  0.0  0.0
LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC      14     7     0     7     7     7     7     7     7     7     0   0

      CPU DATA
CPU      1
TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
USC 1989785.
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - 1089286, USECS

TOTAL TIME MEC WAS BUSY - 1094674, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC - 168491.

NUMBER OF BORAM TO TASK MEMORY LOADS = 1556
TOTAL TIME SPENT LOADING TASK MEMORY = 238740, USECS

NUMBER OF DATA REQUESTS = 3156
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 293738, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED - 431873, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 103431, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 99, USECS

NUMBER OF SEGMENT REFERENCES = 7376
NUMBER OF PAGE FAULTS = 0
NUMBER OF PAGE JUMPS = 3518
UTILITY
EXECUTION STARTED AT 1840 -50

```

Fig. D20—Simplex processor simulation results for the F-111 workload using a 4096-word nonpaged TM, a floating software MEC, and reduced PM assignment activity

ELAPSED TIME = 1000000. USECS

TOTAL PMS ASSIGNED = 3292

PM	1	2	3	4	5	6	7	8	9	10	11	12
NUM	834	625	74	34	31	625	51	43	31	2	782	200
NUM	0	0	0	0	0	0	0	0	0	0	0	0
MSC	11	14	291	274	302	14	248	237	285	970	11	49
MSC	4	7	281	252	265	7	243	219	263	945	4	40

INTERRUPT DATA

INT	1	2	3	4	5	6	7	8	9	10	11	12
NUM	10000	927	0	3631	0	0	0	3631	4845	4845	0	0
USC	3	5	0	1	1	29	5	10	16	3	0	0
USC	180	119	0	111	77	801	108	178	187	148	0	0
USC	14	21	0	7	14	21	7	14	7	7	0	0

MEC ROUTINE DATA

ROU	1	2	3	4	5	6	7	8	9	10	11	12
NUM	10000	927	0	3631	1414	6935	3631	3631	4845	4845	0	0
USC	3	5	0	1	1	29	5	10	16	3	0	0
USC	180	119	0	111	77	801	108	178	187	148	0	0
USC	14	21	0	7	14	21	7	14	7	7	0	0

CPU DATA

CPU	1
USC	3049575.
USC	1336112. USECS

TOTAL TIME MEC WAS BUSY = 1933166. USEC

FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0.

NUMBR OF BORAM TO TASK MEMORY LOADS = 3631

TOTAL TIME SPENT LOADING TASK MEMORY = 810683. USECS

NUMBR OF DATA REQUESTS = 4845

TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 405291. USECS

TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 739802. USECS

TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 204672. USECS

LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 387. USECS

NUMBR OF SEGMENT REFERENCES = 24443

NUMBR OF PAGE FAULTS = 0

NUMBR OF PAGE JUMPS = 17117

Fig. D21—Simplex processor simulation results for the E-2B workload using a 4096-word nonpaged TM and a dedicated software MEC

```

ELAPSED TIME = 10100000, USECS

TOTAL PMS ASSIGNED = 3306

PM      1      2      3      4      5      6      7      8      9      10     11     12
NUMBER OF ITERATIONS OF EACH PM
NUM  834  625  34  34  31  625  35  35  31  3  819  200
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
NUM   0   0   0   0   0   0   0   0   0   0   0   0
AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC  11  14  292  270  302  13  247  235  284  981  10  49
SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC   5   7  282  231  281   6  234  212  272  950   3  41

      INTERRUPT DATA
INT      1      2      3      4      5      6      7      8      9      10     11     12
NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
NUM  1000  979   0  3613   0   0   0  3613  4830  4830   0   0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - 0,5 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - 14, USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - 195055, USECS

      MEC ROUTINE DATA
ROU      1      2      3      4      5      6      7      8      9      10     11     12
NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
NUM  1000  979   0  3613  1414  6969  3613  3613  4830  4830   0   0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC   4   5   0   2   1  29   5  10  16   3   0   0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC  162  124   0  111  83  672  108  151  160  164   0   0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
MSC  406,0  29,7  3,0  54,2  72,1  787,5  57,8  57,8  77,3  77,3  0,0  0,0
AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC   0,3  0,9   0  0,1  0,3  1,5  0,1  1,4  0,1  0,1  0,0  0,0
LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC   14  21   0   7  14  21   7  14   7   7   0   0

      CPU DATA
CPU      1
TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
USC  3435414,
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - 1269830, USECS

TOTAL TIME MEC WAS BUSY - 1838756, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC - 436447, U

NUMBER OF BORAM TO TASK MEMORY LOADS - 3613
TOTAL TIME SPENT LOADING TASK MEMORY - 798471, USECS

NUMBER OF DATA REQUESTS - 4830
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY - 404684, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED - 735417, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES - 203479, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 354, USECS

NUMBER OF SEGMENT REFERENCES - 23966
NUMBER OF PAGE FAULTS - 0
NUMBER OF PAGE JUMPS - 16685

```

Fig. D22—Simplex processor simulation results for the E-2B workload using a 4096-word nonpaged TM and a floating software MEC

```

ELAPSED TIME = 1000000. USECS

TOTAL PMS ASSIGNED = 3234

PM 1 2 3 4 5 6 7 8 9 10 11 12
NUM 834 625 34 34 31 625 46 38 31 2 734 200
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
NUM 0 0 0 0 0 0 0 0 0 0 0 0
AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC 11 15 291 274 301 14 248 241 286 970 10 49
SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC 4 6 279 252 269 6 241 228 266 945 4 41

INTERRUPT DATA
INT 1 2 3 4 5 6 7 8 9 10 11 12
NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
NUM 10000 880 10736 3553 0 0 0 10736 4754 4754 0 0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - 0.4 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - 14. USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - 317891. USECS

MEC ROUTINE DATA
ROU 1 2 3 4 5 6 7 8 9 10 11 12
NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
NUM 10000 880 10736 3553 1414 6810 10736 10736 4754 4754 0 0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC 4 6 4 2 2 35 0 0 25 7 0 0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC 177 119 146 114 93 809 63 197 206 171 0 0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
MSC 400.0 53.7 53.7 53.3 72.1 769.5 171.8 171.8 76.1 76.1 0.0 0.0
AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC 0.7 1.4 0.0 0.1 0.9 2.9 0.1 0.9 0.1 0.1 0.0 0.0
LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC 21 21 7 7 14 21 7 14 7 7 0 0

CPU DATA
CPU 1
TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
USC 2835873.
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - 1195836. USECS

TOTAL TIME MEC WAS BUSY - 2215870. USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC -

NUMBER OF BORAM TO TASK MEMORY LOADS - 10736
TOTAL TIME SPENT LOADING TASK MEMORY - 407968. USECS

NUMBER OF DATA REQUESTS - 4754
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY - 402329. USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED - 794328. USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES - 246093. USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 359. USECS

NUMBER OF SEGMENT REFERENCES - 26951
NUMBER OF PAGE FAULTS - 10736
NUMBER OF PAGE JUMPS - 16029
    
```

Fig. D23—Simplex processor simulation results for the E-2B workload using a 1024-word paged TM and a dedicated software MEC

```

ELAPSED TIME = 10000000, USECS

TOTAL PMS ASSIGNED = 3217

PH  1  2  3  4  5  6  7  8  9  10  11  12
NUM 834 625 34 34 31 625 31 38 31 2 732 200
NUM 0 0 0 0 0 0 0 0 0 0 0 0
MSC 11 14 289 268 295 14 247 236 283 962 10 49
MSC 2 6 285 235 260 5 233 206 268 930 2 40

INTERERRUPT DATA
INT  1  2  3  4  5  6  7  8  9  10  11  12
NUM 10000 901 10657 3536 0 0 0 10657 4728 4728 0 0
MSC 0,4 14,0 31644,9
MSC 0,4 14,0 31644,9

MEC ROUTINE DATA
RBU  1  2  3  4  5  6  7  8  9  10  11  12
NUM 10000 901 10657 3536 1414 6814 10657 10657 4728 4728 0 0
MSC 400,0 53,0 53,3 53,0 72,1 770,0 170,5 170,5 75,6 75,6 0,0 0,0
MSC 0,9 1,6 0,0 0,1 1,0 2,8 0,1 0,8 0,1 0,1 0,0 0,0
MSC 14 14 7 7 14 28 7 14 7 7 0 0

CPL DATA
CPU 1
JSC 3511812,
MSC 1236046, USECS

TOTAL TIME MEC WAS BUSY = 2212951, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 642487,

NUMBER OF BORAM TO TASK MEMORY LOADS = 10657
TOTAL TIME SPENT LOADING TASK MEMORY = 404966, USECS

NUMBER OF DATA REQUESTS = 4728
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 401217, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 789086, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 243191, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 405, USECS

NUMBER OF SEGMENT REFERENCES = 24963
NUMBER OF PAGE FAULTS = 10657
NUMBER OF PAGE JUMPS = 16174
UTILITY
EXECUTION STARTED AT 1240 +43

```

Fig. D24—Simplex processor simulation results for the E-2B workload using a 1024-word paged TM and a floating software MEC

ELAPSED TIME = 10000000; USECS

TOTAL PMS ASSIGNED = 3268

PM	1	2	3	4	5	6	7	8	9	10	11	12
NUM	834	625	34	34	31	625	30	32	31	2	781	200
NUM	0	0	0	0	0	0	0	0	0	0	0	0
MSC	11	15	291	274	301	14	248	237	266	971	11	49
MSC	4	7	288	255	273	6	245	219	275	950	2	42

INTERRUPT DATA

INT	1	2	3	4	5	6	7	8	9	10	11	12
NUM	10000	908	9917	3563	0	0	0	9917	4779	4779	0	0
MSC	0,3											
MSC	14											
MSC	307041											

MEC ROUTINE DATA

RGU	1	2	3	4	5	6	7	8	9	10	11	12
NUM	10000	908	9917	3563	1414	6848	9917	9917	4779	4779	0	0
USC	5	6	4	1	2	33	0	8	24	7	0	0
USC	185	118	130	109	84	728	108	197	206	177	0	0
MSC	400,0	55,4	49,6	53,4	72,1	773,8	158,7	158,7	76,5	76,5	0,0	0,0
USC	0,7	1,2	0,0	0,4	0,7	2,7	0,1	0,8	0,1	0,1	0,0	0,0
USC	14	14	7	7	14	21	7	14	7	7	0	0

CPL DATA

CPU 1

USC 2852810,

TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 1280128, USECS

TOTAL TIME MEC WAS BUSY = 2181669, USEC

FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0,

NUMBER OF BORAN TO TASK MEMORY LOADS = 9917

TOTAL TIME SPENT LOADING TASK MEMORY = 376846, USECS

NUMBER OF DATA REQUESTS = 4779

TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 402238, USECS

TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 786525, USECS

TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 239578, USECS

LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 437, USECS

NUMBER OF SEGMENT REFERENCES = 27392

NUMBER OF PAGE FAULTS = 9917

NUMBER OF PAGE JUMPS = 14531

Fig. D25—Simplex processor simulation results for the E-2B workload using a 1024-word paged multiprogrammed TM and a dedicated software MEC

```

ELAPSED TIME = 10000000. USECS

TOTAL PMS ASSIGNED = 3228

PM      1      2      3      4      5      6      7      8      9      10     11     12
NUMBER OF ITERATIONS OF EACH PM
NUM  434  625   34   34   31  625   41   37   31   2  734  200
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
NUM      0      0      0      0      0      0      0      0      0      0      0      0
AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC  11  14  288  268  293  14  247  234  282  966  10  48
SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC   2   5  280  251  263   5  229  209  250  937   2  38

      INTERRUPT DATA
INT      1      2      3      4      5      6      7      8      9      10     11     12
NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
NUM  10000  903  9913  3543   0   0   0  9913  4739  4739   0   0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - 0.3 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - 14. USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - 306250. USECS

      MEC ROUTINE DATA
ROI      1      2      3      4      5      6      7      8      9      10     11     12
NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
NUM  10000  903  9913  3543  1414  6823  9913  9913  4739  4739   0   0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC   4   6   4   2   3   33   0   8   24   7   0   0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC  157  115  156  109   93  752  108  150  169  172   0   0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
MSC  400.0  55.1  49.6  53.1  72.1  771.0  158.6  158.6  75.8  75.8  0.0  0.0
AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC   0.9  1.5  0.0  0.1  1.0  2.6  0.1  0.8  0.1  0.0  0.0  0.0
LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC   14  14   7   7  14  21   7  14   7   7   0   0

      CPU DATA
CPU      1
TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
USC  3478695.
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - 1295359. USECS

TOTAL TIME MEC WAS BUSY - 2176020. USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 607472.

NUMBER OF ROMAM TO TASK MEMORY LOADS - 9913
TOTAL TIME SPENT LOADING TASK MEMORY - 376694. USECS

NUMBER OF DATA REQUESTS - 4739
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY - 401825. USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED - 784210. USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES - 237701. USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 353. USECS

NUMBER OF SEGMENT REFERENCES - 27506
NUMBER OF PAGE FAULTS - 9913
NUMBER OF PAGE JUMPS - 16627
UTILITY
EXECUTION STARTED AT 1727 -26

```

Fig. D26—Simplex processor simulation results for the E-2B workload using a 1024-word paged multiprogrammed TM and a floating software MEC

ELAPSED TIME = 1000000, USECS

TOTAL PMS ASSIGNED = 3249

PM	1	2	3	4	5	6	7	8	9	10	11	12
NUM	834	625	34	34	31	625	40	49	31	2	744	200
NUM	0	0	0	0	0	0	0	0	0	0	0	0
MSC	11	10	291	273	300	14	247	238	284	968	11	49
MSC	2	0	262	245	272	5	227	213	257	944	2	40

INTERRUPT DATA

INT	1	2	3	4	5	6	7	8	9	10	11	12
NUM	1000	883	3666	3612	0	0	0	3666	4804	4804	0	0
USC	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
USC	14	14	14	14	14	14	14	14	14	14	14	14
USC	220045	220045	220045	220045	220045	220045	220045	220045	220045	220045	220045	220045

MEC ROUTINE DATA

ROU	1	2	3	4	5	6	7	8	9	10	11	12
NUM	1000	883	3666	3612	1414	6872	3666	3666	4804	4804	0	0
USC	3	6	4	2	1	30	0	6	20	7	0	0
USC	178	114	151	110	61	752	56	134	175	169	0	0
MSC	400.0	23.9	18.3	54.2	72.1	776.5	58.7	58.7	76.9	76.9	0.0	0.0
USC	1.5	1.2	0.0	0.1	0.5	1.8	0.1	0.5	0.1	0.1	0.0	0.0
USC	14	14	7	7	14	21	7	14	7	7	0	0

CPU DATA

CPU 1

USC TOTAL TIME EACH CPU IS ASSIGNED - IN USECS 2730010.

USC TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 1274335, USECS

TOTAL TIME MEC WAS BUSY = 1866108, USEC

FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 344672.

NUMBER OF BORAM TO TASK MEMORY LOADS = 3666

TOTAL TIME SPENT LOADING TASK MEMORY = 139308, USECS

NUMBER OF DATA REQUESTS = 4804

TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 404363, USECS

TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 764217, USECS

TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 213362, USECS

LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 347, USECS

NUMBER OF SEGMENT REFERENCES = 27235

NUMBER OF PAGE FAULTS = 3666

NUMBER OF PAGE JUMPS = 16300

UTILITY

EXECUTION STARTED AT 1130 +24

Fig. D27—Simplex processor simulation results for the E-2B workload using a 3072-word paged multiprogrammed TM and a floating software MEC

```

ELAPSED TIME = 10000000, USECS

TOTAL PMS ASSIGNED = 3269

PH  1  2  3  4  5  6  7  8  9  10  11  12
NUM 834 625 34 34 31 625 45 31 31 2 784 193
NUM NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
    0  0  0  0  0  0  0  0  0  0  0  0
MSC AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE = IN MSECS
    11 15 295 277 305 15 240 236 288 972 11 49
MSC SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE = IN MSECS
    A 12 280 256 277 8 238 222 272 948 4 42

      INTERRUPT DATA
INT  1  2  3  4  5  6  7  8  9  10  11  12
NUM 2500 911 0 3560 0 0 0 3560 4713 4713 0 0
MSC AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0,7 USECS
    LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 12, USECS
    TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 139699, USECS

      MEC ROUTINE DATA
RBU  1  2  3  4  5  6  7  8  9  10  11  12
NUM 2500 911 0 3560 1354 6841 3560 3560 4713 4713 0 0
MSC AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE = IN USECS
    2  5  0  1  1  29  1  9  14  2  0  0
MSC LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE = IN USECS
    110 116 0 120 61 405 101 122 131 172 0 0
MSC TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE = IN MSECS
    100,0 55,6 0,0 53,4 69,1 773,0 57,0 57,0 75,4 75,4 0,0 0,0
MSC AVERAGE TIME EACH ROUTINE IS IDLER BY INTERRUPTS = IN USECS
    0,2 0,7 0,0 0,0 0,2 0,9 0,0 1,3 0,0 0,0 0,0 0,0
MSC LONGEST TIME EACH ROUTINE IS IDLER BY INTERRUPTS = IN USECS
    14 14 0 7 14 21 7 7 7 7 0 0

      CPL DATA
CPU  1
MSC TOTAL TIME EACH CPU IS ASSIGNED = IN USECS
    2907748.
MSC TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 1262698, USECS

TOTAL TIME MEC WAS BUSY = 1455493, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0,

NUMBER OF BRAM TO TASK MEMORY LOADS = 3560
TOTAL TIME SPENT LOADING TASK MEMORY = 791956, USECS

NUMBER OF DATA REQUESTS = 4713
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 400377, USECS
TOTAL TIME PROCESSORS ARE IDLER WAITING FOR DATA REQUESTS TO BE SATISFIED = 710338, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 190247, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 229, USECS

NUMBER OF SEGMENT REFERENCES = 23684
NUMBER OF PAGE FAULTS = 0
NUMBER OF PAGE JUMPS = 16481

```

Fig. D28—Simplex processor simulation results for the E-2B workload using a 4096-word nonpaged TM, a dedicated software MEC, and a 4-msec clock interval

```

ELAPSED TIME = 10:00000, USECS

TOTAL PMS ASSIGNED = 3266

PM      1      2      3      4      5      6      7      8      9     10     11     12
NUMBER OF ITERATIONS OF EACH PM
NUM  834 620  54  34  31 620  34  41  31  2 782 193
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
NUM      0      0      0      0      0      0      0      0      0      0      0      0
AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC  11 10 295 276 304 15 247 237 286 966 11 49
SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC   4  8 288 244 265  8 230 218 272 936  4 42

      INTERRUPT DATA
INT      1      2      3      4      5      6      7      8      9     10     11     12
NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
NUM  25  937  0 3597 1304 6904 3597 3597 4782 4782  0  0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - 0,7 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - 11, USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - 141365, USECS

      MEC ROUTINE DATA
ROU      1      2      3      4      5      6      7      8      9     10     11     12
NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
NUM  25  937  0 3597 1304 6904 3597 3597 4782 4782  0  0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC   2  5  0  1  1  29  1  9  14  2  0  0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC  14  122  0 111  61  537  101  178  187  172  0  0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
MSC  100  57,2  5,0  54,0  69,1 780,2  57,6  57,6  76,5  76,5  0,0  0,0
AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC  0,3  0,8  0,0  0,0  0,3  1,0  0,0  1,3  0,0  0,0  0,0  0,0
LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC  14  14  0  7  14  21  7  14  7  7  0  0

      CPU DATA
CPU      1
TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
USC  313004
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - 1327808, USECS

TOTAL TIME MEC WAS BUSY - 1469811, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC - 317451.

NUMBER OF BORAM TO TASK MEMORY LOADS - 3597
TOTAL TIME SPENT LOADING TASK MEMORY - 801063, USECS

NUMBER OF DATA REQUESTS - 4782
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY - 401920, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED - 720133, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES - 194305, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 390, USECS

NUMBER OF SEGMENT REFERENCES - 24104
NUMBER OF PAGE FAULTS - 0
NUMBER OF PAGE JUMPS - 16970
    
```

Fig. D29—Simplex processor simulation results for the E-2B workload using a 4096-word nonpaged TM, a floating software MEC, and a 4-msec clock interval

```

ELAPSED TIME = 10:00000, USECS

TOTAL PMS ASSIGNED = 3236

PM      1    2    3    4    5    6    7    8    9    10   11   12
NUMBER OF ITERATIONS OF EACH PM
NUM 834 625  64  34  31 625  37  36  31  2 747 200
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
NUM      0    0    0    0    0    0    0    0    0    0    0    0
AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC  11  14 292 271 300  14 248 234 282 973  11  49
SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC   4   7 276 201 222   6 244 199 212 950   4  41

      INTERRUPT DATA
INT      1    2    3    4    5    6    7    8    9    10   11   12
NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
NUM 100.0 889   0 3547   0   0   0 3547 4739 4739   0   0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - 0.5 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - 14, USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - 192227, USECS

      MEC ROUTINE DATA
RQU      1    2    3    4    5    6    7    8    9    10   11   12
NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
NUM 100.0 889   0 3547 1414 5242 3547 3547 4739 4739   0   0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC   3   4   0   1   1   2   5   6  12   1   0   0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC  177 119   0   55  84  288  129  111  131  108   0   0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
MSC  40.0 54.2   .0 53.2 72.1 592.3 56.8 56.8 75.8 75.8  0.0  0.0
AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC  0.3 1.2   .0  0.1  0.3  0.7  0.1  1.8  0.1  0.1  0.0  0.0
LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC   14  14   0   7  14  14   7  14   7   7   0   0

      CPU DATA
CPU      1
TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
USC 3312055.
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - 1312058, USECS

TOTAL TIME MEC WAS BUSY - 1629273, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC - 349374.

NUMBER OF BORAM TO TASK MEMORY LOADS = 3547
TOTAL TIME SPENT LOADING TASK MEMORY = 791650, USECS

NUMBER OF DATA REQUESTS = 4739
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 401629, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 702047, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 184449, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 167, USECS

NUMBER OF SEGMENT REFERENCES = 23846
NUMBER OF PAGE FAULTS = 0
NUMBER OF PAGE JUMPS = 16589
UTILITY
EXECUTION STARTED AT 1836 -05

```

Fig. D30—Simplex processor simulation results for the E-2B workload using a 4096-word nonpaged TM, a floating software MEC, and a reduced PM assignment activity

ELAPSED TIME = 1000000 USECS

TOTAL PMS ASSIGNED = 443

PM	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
NUM	332	50	20	10	10	4	4	1	1	1	1	1	1	1	1	1	1	1	1	1
NUM	6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MSC	1	18	47	48	47	193	184	904	90	48	46	9832	9768	9766	9762	9760	9759	9758	9757	9526
MSC	0	17	45	46	43	165	154	904	90	48	46	9832	9768	9766	9762	9760	9759	9758	9757	9526

INTERRUPT DATA

INT	1	2	3	4	5	6	7	8	9	10	11	12
NUM	1000	1	0	712	0	0	0	712	870	870	0	0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - 0,1 USECS												
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - 7, USECS												
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - 29155, USECS												

MEC ROUTINE DATA

RBU	1	2	3	4	5	6	7	8	9	10	11	12
NUM	1000	0	0	712	377	1124	712	712	870	870	0	0
USC	5	0	0	4	4	12	4	7	5	4	0	0
USC	96	0	0	106	32	514	40	105	111	112	0	0
MSC	40,0	0,0	0,0	10,7	19,2	127,0	11,4	11,4	13,9	13,9	0,0	0,0
USC	1,1	0,0	0,0	0,1	1,1	1,8	0,1	0,2	0,2	0,1	0,0	0,0
USC	14	0	0	7	14	14	7	7	7	7	0	0

CPL DATA

CPU 1

USC TOTAL TIME EACH CPU IS ASSIGNED - IN USECS 766551

TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - 493711, USECS

TOTAL TIME MEC WAS BUSY - 276498, USECS

FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC - 107448

NUMBER OF BORAM TO TASK MEMORY LOADS - 712

TOTAL TIME SPENT LOADING TASK MEMORY - 40908, USECS

NUMBER OF DATA REQUESTS - 870

TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY - 61303, USECS

TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED - 110491, USECS

TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES - 25286, USECS

LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 163, USECS

NUMBER OF SEGMENT REFERENCES - 590

NUMBER OF PAGE FAULTS - 0

NUMBER OF PAGE JUMPS - 590

Fig. D31--Simplex processor simulation results for the GE workload using a 4096-word nonpaged TM, a floating software MEC, and an abbreviated run time

```

ELAPSED TIME = 100000, USECS

TOTAL PMS ASSIGNED = 437

PM 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
NUM 326 50 20 10 10 4 4 1 1 1 1 1 1 1 1 1 1 1 1 1
NUM NUMBER OF ITERATIONS OF EACH PM
NUM 23 6 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
MSC AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC 1 16 46 46 43 128 163 641 46 42 40 9768 9745 9740 9584 9579 9577 9576 9575 9308
MSC SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC -1 15 38 44 37 158 93 641 46 42 40 9766 9745 9740 9584 9579 9577 9576 9575 9308

INTERRUPT DATA
INT 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 1 1296 706 0 0 0 1296 864 864 0 0
MSC AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - 0,1 USECS
MSC LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - 12, USECS
MSC TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - 42189, USECS

MEC ROUTINE DATA
RBU 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 0 1296 706 391 1112 1296 1296 864 864 0 0
MSC AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
MSC 6 0 6 4 7 14 0 6 5 6 0 0
MSC LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
MSC 116 0 112 110 44 480 40 87 107 103 0 0
MSC TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
MSC 40,0 0,0 6,5 10,6 19,9 125,7 20,7 20,7 13,8 13,8 0,0 0,0
MSC AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
MSC 1,6 0,0 0,0 0,0 2,3 2,1 0,1 0,2 0,3 0,0 0,0 1,0
MSC LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
MSC 12 0 7 7 12 11 7 7 7 7 0 0

CPU DATA
CPU 1
MSC TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
MSC 849093,
MSC TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - 490411, USECS

TOTAL TIME MEC WAS BUSY - 313976, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC - 133087,

NUMBER OF BRANCH TO TASK MEMORY LOADS = 1296
TOTAL TIME SPENT LOADING TASK MEMORY = 49248, USECS

NUMBER OF DATA REQUESTS = 864
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 81165, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 112375, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 25290, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 177, USECS

NUMBER OF SEGMENT REFERENCES = 1296
NUMBER OF PAGE FAULTS = 1296
NUMBER OF PAGE JUMPS = 590

```

Fig. D32—Simplex processor simulation results for the GE workload using a 1024-word paged TM, a floating software MEC, and an abbreviated run time

ELAPSED TIME = 1000000 USECS

TOTAL PMS ASSIGNED = 436

PM	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
NUM	325	50	20	10	10	4	4	1	1	1	1	1	1	1	1	1	1	1	1	1
NUM	20	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MSC	1	18	48	54	52	196	191	910	53	50	48	9837	9770	9767	9765	9761	9760	9759	9758	9524
MSC	1	16	45	51	45	167	161	910	53	50	48	9837	9770	9767	9765	9761	9760	9759	9758	9524

INTERRUPT DATA

INT	1	2	3	4	5	6	7	8	9	10	11	12
NUM	1000	1	551	705	0	0	0	551	863	863	0	0
USC											0.1	
USC											7	
USC											31738	

MEC ROUTINE DATA

RGU	1	2	3	4	5	6	7	8	9	10	11	12
NUM	1000	0	551	705	394	1110	551	551	863	863	0	0
USC	3	0	5	3	3	12	0	7	5	4	0	0
USC	113	0	99	110	44	385	40	87	102	106	0	0
MSC	40.0	0.0	2.8	10.4	20.1	125.4	8.8	8.8	13.8	13.8	0.0	0.0
USC	1.1	0.0	0.1	0.2	1.3	1.2	0.1	0.2	0.2	0.2	0.0	0.0
USC	14	0	7	7	14	14	7	7	7	7	0	0

CPL DATA

CPU	1
USC	751167
USC	409061

TOTAL TIME MEC WAS BUSY = 275040, USEC

FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 93280,

NUMBER OF BORAM TO TASK MEMORY LOADS = 551

TOTAL TIME SPENT LOADING TASK MEMORY = 20938, USECS

NUMBER OF DATA REQUESTS = 863

TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 61072, USECS

TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 110090, USECS

TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 25077, USECS

LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 139, USECS

NUMBER OF SEGMENT REFERENCES = 1295

NUMBER OF PAGE FAULTS = 551

NUMBER OF PAGE JUMPS = 590

Fig. D33--Simplex processor simulation results for the GE workload using a 3072-word paged multiprogrammed TM, a floating software MEC, and an abbreviated run time

```

ELAPSED TIME = 20000, USECS

TOTAL PMS ASSIGNED = 35

PM 1 2 3 4 5 6 7 8 9 10 11
NUM NUMBER OF ITERATIONS OF EACH PM
    25 1 1 1 1 1 1 1 1 1 1
NUM NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
    0 0 0 0 0 0 0 0 0 0 0
MSC AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
    5 245 1822 46 18 1833 1832 1833 1834 1830 1824
MSC SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
    7 245 1822 46 18 1833 1832 1833 1834 1830 1824

INTERRUPT DATA
INT 1 2 3 4 5 6 7 8 9 10 11 12
NUM NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
    200 1 0 65 0 0 0 66 142 142 0 0
MSC AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - IN USECS
    0,4
MSC LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - IN USECS
    7,
MSC TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - IN USECS
    4319,

MEC ROUTINE DATA
RBU 1 2 3 4 5 6 7 8 9 10 11 12
NUM NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
    200 0 0 66 24 91 66 66 142 142 0 0
MSC AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
    3 0 0 3 1 3 4 5 4 3 0 0
MSC LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
    100 0 0 34 16 47 40 78 53 91 0 0
MSC TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
    8,0 0,0 0,0 1,0 1,2 10,3 1,1 1,1 2,3 2,3 0,0 0,0
MSC AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
    0,7 0,0 0,0 0,6 0,6 0,9 0,0 0,3 0,4 0,2 0,0 0,0
MSC LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
    14 0 0 7 7 7 0 7 7 7 0 0

CPU DATA
CPU 1
MSC TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
    172752,
MSC TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - IN USECS
    128317,

TOTAL TIME MEC WAS BUSY - 31477, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC - 14219,

NUMBER OF BURAH TO TASK MEMORY LOADS - 46
TOTAL TIME SPENT LOADING TASK MEMORY - 8662, USECS

NUMBER OF DATA REQUESTS - 142
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY - 10506, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED - 18472, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES - 4220, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 139, USECS

NUMBER OF SEGMENT REFERENCES - 314
NUMBER OF PAGE FAULTS - 0
NUMBER OF PAGE JUMPS - 225
UTILITY
EXECUTION STARTED AT 1892 -03

```

Fig. D34—Simplex processor simulation results for the F-111 workload using a 4096-word nonpaged TM, a floating software MEC, and an abbreviated run time

```

ELAPSED TIME = 200000 USECS

TOTAL PMS ASSIGNED = 35

PMS 1 2 3 4 5 6 7 8 9 10 11
NUM 25 1 1 1 1 1 1 1 1 1 1
NUMBER OF TIMES EACH PMS MISSED ITS COMPLETION DEADLINE
NUM 0 0 0 0 0 0 0 0 0 0 0
AVERAGE TIME BY WHICH EACH PMS BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC 5 246 18.5 46 18 1630 1832 1632 1823 1818 1807
SHORTEST TIME BY WHICH EACH PMS BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC 2 246 18.5 46 18 1630 1832 1632 1823 1818 1807

INTERRUPT DATA
INT 1 2 3 4 5 6 7 8 9 10 11 12
NUM 200 1 228 64 0 0 0 228 147 147 0 0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - 0.2 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - 7. USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - 7119. USECS

MEC ROUTINE DATA
ROU 1 2 3 4 5 6 7 8 9 10 11 12
NUM 200 0 228 66 24 91 228 228 147 147 0 0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC 4 0 4 1 2 0 2 4 1 0 0 0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC 118 0 107 74 23 47 0 75 50 47 0 0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
MSC 8.0 0.0 1.1 1.0 1.2 10.3 3.6 3.6 2.4 2.4 0.0 0.0
AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC 1.0 0.0 1.0 0.1 1.2 1.3 0.1 0.8 0.2 0.1 0.0 0.0
LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC 7 0 0 7 7 7 7 7 7 7 0 0

CPU DATA
CPU 1
USC TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
67944.
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - 132587. USECS

TOTAL TIME MEC WAS BUSY - 40756. USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC - 18746.

NUMBER OF SCHED TO TASK SCHED LOADS - 228

TOTAL TIME SPENT LOADING TASK MEMORY - 8664. USECS

NUMBER OF DATA REQUESTS - 147
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY - 10727. USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED - 18721. USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES - 4314. USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 120. USECS

NUMBER OF SEGMENT REFERENCES - 389
NUMBER OF PAGE FAULTS - 228
NUMBER OF PAGE JUMPS - 235
UTILITY
    
```

Fig. D35—Simplex processor simulation results for the F-111 workload using a 1024-word paged TM, a floating software MEC, and an abbreviated run time

```

ELAPSED TIME = 200600; USECS

TOTAL PMS ASSIGNED = 35

PM 1 2 3 4 5 6 7 8 9 10 11
NUM 25 1 1 1 1 1 1 1 1 1 1
NUM NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
0 0 0 0 0 0 0 0 0 0 0
MSC AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
6 246 1833 46 18 1831 1835 1839 1843 1835 1834
MSC SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
3 246 1833 46 18 1831 1835 1839 1843 1835 1834

INTERRUPT DATA
INT 1 2 3 4 5 6 7 8 9 10 11 12
NUM 200 1 30 66 0 0 0 30 142 142 0 0
MSC AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - 0,1 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - 7, USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - 4277, USECS

MEC ROUTINE DATA
ROU 1 2 3 4 5 6 7 8 9 10 11 12
NUM 200 0 30 66 24 91 30 30 142 142 0 0
USC AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
2 0 6 0 0 1 0 1 3 1 0 0
USC LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
118 0 107 46 16 47 0 31 89 40 0 0
MSC TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
8,0 0,0 0,2 1,7 1,2 10,3 0,5 0,5 2,3 2,3 0,0 0,0
USC AVERAGE TIME EACH ROUTINE IS IDLE BY INTERRUPTS - IN USECS
0,5 0,0 0,0 0,1 0,0 0,8 0,2 0,5 0,1 0,1 0,0 0,0
USC LONGEST TIME EACH ROUTINE IS IDLE BY INTERRUPTS - IN USECS
7 0 0 7 0 7 7 7 7 7 0 0

CPL DATA
CPU 1
USC TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
162689,
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - 129567, USECS

TOTAL TIME MEC WAS BUSY - 30428, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC - 11552,

NUMBER OF BORAM TO TASK MEMORY LOADS - 30
TOTAL TIME SPENT LOADING TASK MEMORY - 1140, USECS

NUMBER OF DATA REQUESTS - 142
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY - 10695, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED - 17883, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES - 3739, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 222, USECS

NUMBER OF SEGMENT REFERENCES - 379
NUMBER OF PAGE FAULTS - 30
NUMBER OF PAGE JUMPS - 225
UTILITY
EXECUTION STARTED AT 1158 -10
    
```

Fig. D36—Simplex processor simulation results for the F-111 workload using a 3072-word paged multiprogrammed TM, a floating software MEC, and an abbreviated run time

```

ELAPSED TIME = 10000, USECS

TOTAL PMS ASSIGNED = 40

PH 1 2 3 4 5 6 7 8 9 10 11 12
NUM NUMBER OF ITERATIONS OF EACH PH
    9 7 1 1 1 7 1 1 1 1 8 2

NUM NUMBER OF TIMES EACH PH MISSED ITS COMPLETION DEADLINE
    0 0 0 0 0 0 0 0 0 0 0 0

MSC AVERAGE TIME BY WHICH EACH PH BEAT ITS COMPLETION DEADLINE - IN MSECS
    10 13 267 260 261 13 246 243 272 950 10 46

MSC SHORTEST TIME BY WHICH EACH PH BEAT ITS COMPLETION DEADLINE - IN MSECS
    7 10 267 260 261 10 246 243 272 950 8 46

INTERRUPT DATA

INT 1 2 3 4 5 6 7 8 9 10 11 12
NUM NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
    100 7 0 49 0 0 0 49 77 77 0 0

AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - 0,6 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - 8, USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - 2513, USECS

MEC ROUTINE DATA

ROU 1 2 3 4 5 6 7 8 9 10 11 12
NUM NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
    100 7 0 49 13 78 49 49 77 77 0 0

USC AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
    3 6 0 0 1 20 5 7 12 1 0 0

USC LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
    96 30 0 37 16 242 61 47 63 91 0 0

MSC TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
    4,0 0,4 0,0 0,7 0,7 8,8 0,8 0,8 1,2 1,2 0,0 0,0

USC AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN LSECS
    0,4 2,0 0,0 0,7 0,5 0,9 0,4 1,4 0,0 0,1 0,0 0,0

USC LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN LSECS
    7 7 0 0 7 14 7 7 0 7 0 0

CPL DATA

CPU 1
USC TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
    56434,

TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - 22761, USECS

TOTAL TIME MEC WAS BUSY - 21184, LSEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC - 6953,

NUMBER OF BORAH TO TASK MEMORY LOADS - 49
TOTAL TIME SPENT LOADING TASK MEMORY - 10693, USECS

NUMBER OF DATA REQUESTS - 77
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY - 11002, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED - 15840, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES - 2940, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 167, USECS

NUMBER OF SEGMENT REFERENCES - 512
NUMBER OF PAGE FAULTS - 0
NUMBER OF PAGE JUMPS - 319

UTILITY
EXECUTION STARTED AT: 1851 -36
    
```

Fig. D37—Simplex processor simulation results for the E-2B workload using a 4096-word nonpaged TM, a floating software MEC, and an abbreviated run time

```

ELAPSED TIME = 10,000, USECS

TOTAL PMS ASSIGNED = 38

PM      1      2      3      4      5      6      7      8      9      10     11     12
NUMBER OF ITERATIONS OF EACH PM
NUM      9      7      1      1      1      7      1      1      1      1      6      2
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
NUM      0      0      0      0      0      0      0      0      0      0      0      0
MSC      9      13     265     247     260     13     246     244     268     930      9      46
AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC      6      10     265     247     260      9     246     244     268     930      6      45
SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS

      INTERRUPT DATA
INT      1      2      3      4      5      6      7      8      9      10     11     12
NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
NUM      1.0      7      1.5     47      0      0      0      175     71      0      0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - 0.4 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - 10, USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - 4922, USECS

      MEC ROUTINE DATA
ROU      1      2      3      4      5      6      7      8      9      10     11     12
NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
NUM      1.0      7      1.5     47      13     76     175     175     71     71      0      0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC      6      1      5      1      24      0      7     17      2      0      0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC      1.7      7     105     25     32     303     16     87     91     96      0      0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
MSC      4.0     0.4     0.9     0.7     0.7     8.6     2.8     2.8     1.1     1.1     0.0     0.0
AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC      1.8     6.0     0.0     0.0     1.6     2.5     0.1     0.8     0.1     0.0     0.0     0.0

      CPU DATA
CPU      1
TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
USC      70889,
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - 28913, USECS

TOTAL TIME MEC WAS BUSY - 27652, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC - 12403,

NUMBER OF BORAH TO TASK MEMORY LOADS - 175
TOTAL TIME SPENT LOADING TASK MEMORY - 6650, USECS

NUMBER OF DATA REQUESTS - 71
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY - 10894, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED - 15771, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES - 3092, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 149, USECS

NUMBER OF SEGMENT REFERENCES - 669
NUMBER OF PAGE FAULTS - 175
NUMBER OF PAGE JUMPS - 425
UTILITY
EXECUTION STARTED AT 1814 -14

```

Fig. D38—Simplex processor simulation results for the E-2B workload using a 1024-word paged TM, a floating software MEC, and an abbreviated run time

```

ELAPSED TIME = 100000; USECS

TOTAL PMS ASSIGNED = 41

PH 1 2 3 4 5 6 7 8 9 10 11 12
NUM 9 7 1 1 1 7 1 1 1 1 9 2
NUM 0 0 0 0 0 0 0 0 0 0 0 0
HSC 9 14 289 256 276 13 246 245 272 944 10 47
MSC 5 12 289 256 276 11 246 245 272 944 6 47

INTERLUPT DATA
INT 1 2 3 4 5 6 7 8 9 10 11 12
NUM 100 9 89 50 0 0 0 89 77 0 0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0,3 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 8, USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 3437, USECS

MEC ROUTINE DATA
RBU 1 2 3 4 5 6 7 8 9 10 11 12
NUM 100 9 89 50 13 81 89 89 77 77 0 0
USC 4 3 3 0 2 18 1 4 12 3 0 0
USC 99 15 57 18 16 249 40 82 107 96 0 0
MSC 4,0 0,5 0,4 0,7 0,7 9,2 1,4 1,4 1,2 1,2 0,0
USC 1,2 0,8 0,2 0,4 1,1 1,0 0,2 0,6 0,3 0,1 0,0
USC 14 7 7 4 14 14 7 7 7 0 0

CPU DATA
CPU 1
USC 56635,
TOTAL TIME EACH CPU IS ASSIGNED = IN USECS
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 25965, USECS

TOTAL TIME MEC WAS BUSY = 24309, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC + TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 7297,

NUMBER OF BORAM TO TASK MEMORY LOADS = 89
TOTAL TIME SPENT LOADING TASK MEMORY = 3382, USECS

NUMBER OF DATA REQUESTS = 77
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 11020, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 15912, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 2857, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 164, USECS

NUMBER OF SEGMENT REFERENCES = 631
NUMBER OF PAGE FAULTS = 89
NUMBER OF PAGE JUMPS = 386
UTILITY
EXECUTION STARTED AT 1157 -44
    
```

Fig. D39—Simplex processor simulation results for the E-2B workload using a 3072-word paged multiprogrammed TM, a floating software MEC, and an abbreviated run time

```

ELAPSED TIME = 1000000, USECS

TOTAL PMS ASSIGNED = 526

PM 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
NUM 334 50 20 10 10 4 4 1 1 1 1 10 10 10 10 10 10 10 10 10
NUMBER OF ITERATIONS OF EACH PM

NUM 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE

MSEC 2 19 49 60 50 199 194 916 58 55 53 74 69 69 67 66 66 66 58 17
AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE = IN MSEC

MSEC 1 18 49 59 50 172 166 916 58 55 53 74 69 69 67 66 66 66 51 15
SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE = IN MSEC

INTERRUPT DATA

INT 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 1 0 1074 0 0 0 1074 1583 0 0
NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC

AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0,5 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 14, USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 44205, USECS

MEC ROUTINE DATA

ROU 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 0 0 1074 373 1784 1906 1074 2370 1583 0 0
NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED

USC 13 0 0 0 11 16 8 18 10 15 0 0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE = IN USECS

USC 130 0 0 104 430 447 79 137 154 155 0 0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE = IN USECS

MSEC 40,0 0,0 0,0 16,1 19,0 145,1 30,9 17,2 37,9 25,3 0,0 0,0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE = IN MSEC

USC 1,3 0,0 0,0 0,2 1,7 4,6 0,9 0,5 0,8 0,3 0,0 0,0
AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS = IN USECS

USC 14 0 0 14 14 21 14 7 14 14 0 0
LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS = IN USECS

CPL DATA

CPU 1 2
USC 797976, 588350,
TOTAL TIME EACH CPU IS ASSIGNED = IN USECS

TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 828855, USECS

TOTAL TIME MEC WAS BUSY = 375358, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0,

NUMBER OF BORAM TO TASK MEMORY LOADS = 1074
TOTAL TIME SPENT LOADING TASK MEMORY = 176098, USECS

NUMBER OF DATA REQUESTS = 1583
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 161854, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 302771, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 79272, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 471, USECS

NUMBER OF SEGMENT REFERENCES = 4334
NUMBER OF PAGE FAULTS = 0
NUMBER OF PAGE JUMPS = 4334

```

Fig. D40—Dual processor simulation results for the expanded GE workload using a 4096-word nonpaged TM and a dedicated software MEC

```

ELAPSED TIME = 1000000. USECS

TOTAL PMS ASSIGNED = 526

PM 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
NUM 334 50 20 10 10 4 4 1 1 1 1 10 10 10 10 10 10 10 10 10
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
NUM 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
MSC AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC 2 19 49 54 50 195 187 911 54 52 50 74 69 69 67 67 66 66 52 16
SHORTFST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC 1 17 46 54 44 167 159 911 54 52 50 74 69 69 67 67 66 66 47 13

INTERRUPT DATA
INT 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 1 0 1074 0 0 0 0 1074 1583 1583 0 0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0.5 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 14. USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 44205. USECS

MEC ROUTINE DATA
RMI 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 0 0 1074 373 1240 3767 1074 5816 1583 0 0
USC 11 0 0 6 29 14 5 19 6 9 0 0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC 121 0 0 111 421 281 79 148 154 155 0 0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
MSC TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
MSC 40.0 0.0 0.0 16.1 19.0 140.1 60.3 17.2 93.1 25.3 0.0 0.0
USC AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC 1.3 0.0 0.0 0.3 2.5 4.1 0.8 0.6 0.9 0.2 0.0 0.0
LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC 14 0 0 7 14 21 14 7 14 7 0 0

CPU DATA
CPU 1 2
USC TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
USC 815514. 669110.
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 828855. USECS

TOTAL TIME MEC WAS BUSY = 455298. USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0.

NUMBER OF BORAM TO TASK MEMORY LOADS = 1074
TOTAL TIME SPENT LOADING TASK MEMORY = 176098. USECS

NUMBER OF DATA REQUESTS = 1583
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 161854. USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 364986. USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 151548. USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 933. USECS

NUMBER OF SEGMENT REFERENCES = 4334
NUMBER OF PAGE FAULTS = 0
NUMBER OF PAGE JUMPS = 4334
    
```

Fig. D41—Dual processor simulation results for the expanded GE workload using a 4096-word nonpaged TM, a dedicated software MEC, and a shared program/data bus

ELAPSED TIME = 1000000, USECS

TOTAL PMS ASSIGNED = 521

PM	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
NUM	330	50	20	10	10	4	4	1	1	1	1	10	10	10	10	10	10	10	10	9
NUM	7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4
MSC	1	19	48	45	43	192	183	905	57	54	51	73	60	59	58	56	56	55	54	-0
MSC	-1	17	47	38	37	167	157	905	57	54	51	73	58	56	55	54	53	52	48	-8

INTERRUPT DATA

INT	1	2	3	4	5	6	7	8	9	10	11	12
NUM	1000	1	5366	1067	0	0	0	5366	1574	1574	0	0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0.4 USECS												
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 14. USECS												
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 111636, USECS												

MEC ROUTINE DATA

ROUT	1	2	3	4	5	6	7	8	9	10	11	12
NUM	1000	0	5366	1067	395	1207	7689	5366	2726	1574	0	0
USC	12	0	9	6	34	21	6	14	13	10	0	0
USC	136	0	162	119	215	307	102	102	187	171	0	0
MSC	40.0	0.0	26.8	16.0	20.1	136.4	123.0	85.9	43.6	25.2	0.0	0.0
USC	4.4	0.0	0.1	1.0	7.8	7.5	1.5	0.4	1.3	0.9	0.0	0.0
USC	21	0	7	14	21	21	14	14	14	14	0	0

CPU DATA

CPU	1	2
USC	907116.	772279.
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 824280, USECS		

TOTAL TIME MEC WAS BUSY = 628687, USEC  
 FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0.

NUMBER OF BORAM TO TASK MEMORY LOADS = 5366  
 TOTAL TIME SPENT LOADING TASK MEMORY = 203908, USECS

NUMBER OF DATA REQUESTS = 1574  
 TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 161185, USECS  
 TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 317732, USECS  
 TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 101489, USECS  
 LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 506, USECS

NUMBER OF SEGMENT REFERENCES = 5366  
 NUMBER OF PAGE FAULTS = 5366  
 NUMBER OF PAGE JUMPS = 4298

Fig. D42—Dual processor simulation results for the expanded GE workload using a 1024-word paged TM, a dedicated software MEC

```

ELAPSED TIME = 100000. USECS

TOTAL PMS ASSIGNED = 510

PM 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
NUM 319 50 20 10 10 4 4 1 1 1 1 10 10 10 10 10 10 10 10 9
NUM 36 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
MSC 1 18 46 30 28 175 108 902 55 52 50 72 53 52 50 48 47 47 46 -2
MSC -1 15 42 20 20 140 55 902 55 52 50 71 50 47 46 44 44 44 43 -10

INTERRUPT DATA

INT 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 1 5273 1049 0 0 0 5272 1550 1550 0 0
MSC 0.5 14. 109865.
USC 0.5 14. 109865.

MEC ROUTINE DATA

ROUT 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 0 5273 1049 424 1138 12467 5272 3175 1550 0 0
MSC 40.0 0.0 26.4 15.7 21.6 128.6 199.5 84.4 50.8 24.8 0.0 0.0
USC 4.3 0.0 0.2 1.3 8.8 7.0 1.7 0.4 1.3 0.4 0.0 0.0
MSC 21 0 7 14 21 21 14 14 14 14 0 0
USC 21 0 7 14 21 21 14 14 14 14 0 0

CPU DATA

CPU 1 2
NUM 925410. 863912.
MSC 812005.
USC 812005.

TOTAL TIME MEC WAS BUSY = 701607. USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0.

NUMBER OF BORAM TO TASK MEMORY LOADS = 5273
TOTAL TIME SPENT LOADING TASK MEMORY = 200374. USECS

NUMBER OF DATA REQUESTS = 1550
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 199587. USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 323376. USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 108527. USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 731. USECS

NUMBER OF SEGMENT REFERENCES = 5273
NUMBER OF PAGE FAULTS = 5273
NUMBER OF PAGE JUMPS = 4222
    
```

Fig. D43—Dual processor simulation results for the expanded GE workload using a 1024-word paged TM, a dedicated software MEC, and a shared program/data bus

```

ELAPSED TIME = 1000000, USECS

TOTAL PMS ASSIGNED = 524

PH 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
NUM 333 50 20 10 10 4 4 1 1 1 1 10 10 10 10 10 10 10 9
NUM NUMBER OF TIMES EACH PH MISSED ITS COMPLETION DEADLINE
    1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 3
MSC AVERAGE TIME BY WHICH EACH PH BEAT ITS COMPLETION DEADLINE - IN MSECS
    2 19 49 56 55 198 195 917 57 55 52 73 64 62 61 60 60 60 57 1
MSC SHORTEST TIME BY WHICH EACH PH BEAT ITS COMPLETION DEADLINE - IN MSECS
    -1 18 48 55 47 170 170 917 57 55 52 73 63 61 60 59 59 59 49 -4

```

```

INTERRUPT DATA

INT 1 2 3 4 5 6 7 8 9 10 11 12
NUM NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
    1000 1 4736 1072 0 0 0 4735 1580 1580 0 0
MSC AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - 0.5 USECS
MSC LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - 14. USECS
MSC TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - 102928, USECS

```

```

MEC ROUTINE DATA

RQU 1 2 3 4 5 6 7 8 9 10 11 12
NUM NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
    1000 0 4736 1072 382 1248 5373 4735 2647 1580 0 0
MSC AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
    17 0 10 8 24 16 4 11 13 11 0 0
MSC LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
    130 0 159 119 286 351 86 175 150 171 0 0
MSC TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
    40.0 0.0 23.7 16.1 19.5 141.0 86.0 75.8 42.4 25.3 0.0 0.0
MSC AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
    3.6 0.0 0.1 1.0 7.2 7.7 0.8 0.4 0.9 0.9 0.0 0.0
MSC LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
    21 0 7 14 21 21 14 14 14 14 0 0

```

```

CPU DATA

CPU 1 2
MSC TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
    899701 674945
MSC TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - 827330, USECS

```

```

TOTAL TIME MEC WAS BUSY = 572554, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC - 0

```

```

NUMBER OF BRAM TO TASK MEMORY LOADS = 4735
TOTAL TIME SPENT LOADING TASK MEMORY = 179930, USECS

```

```

NUMBER OF DATA REQUESTS = 1580
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 161631, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 314362, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 96953, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 520, USECS

```

```

NUMBER OF SEGMENT REFERENCES = 5395
NUMBER OF PAGE FAULTS = 4736
NUMBER OF PAGE JUMPS = 4322

```

Fig. D44—Dual processor simulation results for the expanded GE workload using a 2048-word paged multiprogrammed TM and a dedicated software MEC

```

ELAPSED TIME = 1000000 USECS

TOTAL PMS ASSIGNED = 319

PMS 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
NUM 328 50 20 10 10 4 4 1 1 1 1 10 10 10 10 10 10 10 10 9
NUM 15 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 6
MSC 2 19 48 46 44 192 188 914 58 54 53 73 58 57 56 55 55 54 53 0
MSC 01 18 47 41 40 168 165 914 58 54 53 72 56 55 54 53 53 52 51 09

INTERRUPT DATA
INT 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 1 4673 1064 0 0 0 4672 1568 1568 0 0
MSC 0,5 14 101815 0,5 14 101815 0,5 14 101815 0,5 14 101815
MSC 0,5 14 101815 0,5 14 101815 0,5 14 101815 0,5 14 101815

MEC ROUTINE DATA
RBU 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 0 4673 1064 398 1212 8659 4672 3212 1568 0 0
MSC 40,0 0,0 23,4 15,9 20,3 137,0 138,5 74,8 51,4 29,1 0,0 0,0
MSC 4,0 0,0 0,1 1,3 7,3 7,5 1,3 0,4 1,1 0,4 0,0 0,0
MSC 21 0 7 14 21 21 14 14 21 7 0 0

CPL DATA
CPU 1 2
USC 910074, 744407,
MSC 821430, 821430,

TOTAL TIME MEC WAS BUSY = 628155, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC =

NUMBER OF BORAM TO TASK MEMORY LOADS = 4672
TOTAL TIME SPENT LOADING TASK MEMORY = 177536, USECS

NUMBER OF DATA REQUESTS = 1568
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 160801, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 325814, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 107921, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 836, USECS

NUMBER OF SEGMENT REFERENCES = 5348
NUMBER OF PAGE FAULTS = 4673
NUMBER OF PAGE JUMPS = 4284
    
```

Fig. D45—Dual processor simulation results for the expanded GE workload using a 2048-word paged multiprogrammed TM, a dedicated software MEC, and a shared program/data bus

```

ELAPSED TIME = 1000000. USECS

TOTAL PMS ASSIGNED = 526

P# 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
NUM 334 50 20 10 10 4 4 1 1 1 1 10 10 10 10 10 10 10 10 10
NUMBER OF ITERATIONS OF EACH PM
NUM 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
MSC 2 19 49 63 58 200 198 921 62 60 58 74 71 69 68 67 67 67 60 26
AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS
MSC 1 19 49 61 53 176 172 921 62 60 58 74 69 67 66 64 64 64 55 18
SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN MSECS

INTERRUPT DATA
INT 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 1 1344 1074 0 0 0 1344 1583 1583 0 0
NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0.3 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 10. USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 55503. USECS

MEC ROUTINE DATA
R# 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 0 1344 1074 373 1281 1547 1344 2317 1583 0 0
NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
USC 13 0 9 7 11 11 4 13 13 10 0 0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC 130 0 159 112 247 305 86 170 164 163 0 0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
MSC 40.0 0.0 6.7 16.1 19.0 144.8 24.8 21.5 37.1 25.3 0.0 0.0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
USC 1.9 0.0 0.1 0.9 2.2 4.9 0.9 0.4 0.9 0.6 0.0 0.0
AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC 14 0 7 7 21 21 14 14 14 14 0 0
LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS

CPU DATA
CPU 1 2
USC 720520. 555213.
TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 828855. USECS

TOTAL TIME MEC WAS BUSY = 390765. USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0.

NUMBER OF RORAM TO TASK MEMORY LOADS = 1344
TOTAL TIME SPENT LOADING TASK MEMORY = 51072. USECS

NUMBER OF DATA REQUESTS = 1583
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 161854. USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 299092. USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 82907. USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 461. USECS

NUMBER OF SEGMENT REFERENCES = 5408
NUMBER OF PAGE FAULTS = 1344
NUMBER OF PAGE JUMPS = 4334

```

Fig. D46—Dual processor simulation results for the expanded GE workload using a 4096-word paged multiprogrammed TM and a dedicated software MEC

ELAPSED TIME = 1000000. USECS

TOTAL PMS ASSIGNED = 525

PM	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
NUM	333	50	20	10	10	4	4	1	1	1	1	10	10	10	10	10	10	10	10	10
NUM	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MSC	2	19	49	61	56	199	196	917	58	55	53	74	69	67	66	65	65	65	59	24
MSC	0	18	48	60	49	172	169	917	58	55	53	74	68	65	65	63	63	62	51	18

INTERRUPT DATA

INT	1	2	3	4	5	6	7	8	9	10	11	12
NUM	1000	1	1483	1073	0	0	0	1483	1582	1582	0	0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0.3 USECS												
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 14. USECS												
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 57428. USECS												

MEC ROUTINE DATA

ROU	1	2	3	4	5	6	7	8	9	10	11	12
NUM	1000	0	1483	1073	371	1285	2902	1483	2709	1582	0	0
USC	15	0	9	6	19	14	4	13	12	9	0	0
USC	132	0	159	115	364	285	63	169	172	156	0	0
MSC	40.0	0.0	7.4	16.1	18.9	145.2	46.4	23.7	43.3	25.3	0.0	0.0
USC	1.9	0.0	0.3	0.9	2.5	4.8	1.0	0.5	1.1	0.4	0.0	0.0
USC	21	0	7	14	21	21	14	14	14	7	0	0

CPU DATA

CPU	1	2
USC	752407.	565982.
TOTAL TIME EACH CPU IS ASSIGNED - IN USECS		
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 828305. USECS		

TOTAL TIME MEC WAS BUSY = 423880. USEC

FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0.

NUMBER OF BORAM TO TASK MEMORY LOADS = 1483

TOTAL TIME SPENT LOADING TASK MEMORY = 56354. USECS

NUMBER OF DATA REQUESTS = 1582

TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 161821. USECS

TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 306669. USECS

TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 92759. USECS

LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 769. USECS

NUMBER OF SEGMENT REFERENCES = 5407

NUMBER OF PAGE FAULTS = 1483

NUMBER OF PAGE JUMPS = 4334

Fig. D47--Dual processor simulation results for the expanded GE workload using a 4096-word paged multiprogrammed TM, a dedicated software MEC, and a shared program/data bus

ELAPSED TIME = 1000000, USECS

TOTAL PMS ASSIGNED = 618

PH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
NUM	334	50	20	10	10	10	10	1	1	1	1	20	20	20	20	20	20	20	20	10
NUM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MSC	2	19	44	64	62	72	41	985	62	59	57	24	20	19	18	18	18	18	18	36
MSC	1	19	36	63	56	72	37	985	62	59	57	24	20	19	18	18	17	17	17	35

INTERRUPT DATA

INT	1	2	3	4	5	6	7	8	9	10	11	12
NUM	1000	1	0	1318	0	0	0	1318	2061	2061	0	0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0.6 USECS												
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 12. USECS												
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 54313, USECS												

MEC ROUTINE DATA

RQU	1	2	3	4	5	6	7	8	9	10	11	12
NUM	1000	0	0	1318	373	1583	4055	1318	4407	2061	0	0
USC	15	0	0	13	23	37	6	25	11	18	0	0
USC	133	0	0	133	293	558	101	150	159	158	0	0
MSC	40.0	0.0	0.0	19.8	19.0	178.9	64.9	21.1	70.5	33.0	0.0	0.0
USC	1.2	0.0	0.0	0.7	2.1	6.1	1.2	0.6	1.2	0.9	0.0	0.0
USC	14	0	0	14	14	28	14	7	14	14	0	0

CPU DATA

CPU	1	2	3
USC	779184.	625897.	495400.
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 1046343, USECS			

TOTAL TIME MEC WAS BUSY = 501441, USEC  
 FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0.

NUMBER OF BORAM TO TASK MEMORY LOADS = 1318  
 TOTAL TIME SPENT LOADING TASK MEMORY = 231614, USECS

NUMBER OF DATA REQUESTS = 2061  
 TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 240748, USECS  
 TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 476798, USECS  
 TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 146445, USECS  
 LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 619, USECS

NUMBER OF SEGMENT REFERENCES = 5770  
 NUMBER OF PAGE FAULTS = 0  
 NUMBER OF PAGE JUMPS = 5770

Fig. D48—Triple processor simulation results for the further expanded GE workload using a 4096-word nonpaged TM and a dedicated software MEC

```

ELAPSED TIME = 100000. USECS

TOTAL PMS ASSIGNED = 618

PM 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
NUM 354 50 20 10 10 10 10 1 1 1 1 20 20 20 20 20 20 20 20 20
NUMBER OF ITERATIONS OF EACH PM
NUM 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
MSC 2 10 30 51 48 71 26 922 51 26 24 24 17 16 15 14 13 13 13 28
AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN USECS
MSC 1 17 23 51 22 71 24 922 51 26 24 24 16 14 14 13 13 12 12 27
SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE - IN USECS

INTERRUPT DATA
INT 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 1 0 1318 0 0 0 1318 2061 0 0
NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE - 0.6 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE - 13. USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS - 54313. USECS

MEC ROUTINE DATA
ROU 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 0 0 1318 3/3 1512 6853 1318 11416 2061 0 0
NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
USC 15 0 0 12 137 80 8 25 12 17 0 0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
USC 125 0 0 121 851 1041 93 150 138 173 0 0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE - IN USECS
MSC 40.0 0.0 0.0 19.8 19.0 170.9 109.6 21.1 182.7 33.0 0.0 0.0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE - IN MSECS
USC 1.6 0.0 0.0 0.6 1.7 6.1 1.1 0.6 1.1 0.2 0.0 0.0
AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS
USC 21 0 0 14 14 21 14 14 21 7 0 0
LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS - IN USECS

CPU DATA
CPU 1 2 3
USC 744272. 703675. 673607.
TOTAL TIME EACH CPU IS ASSIGNED - IN USECS
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS - 1046343. USECS

TOTAL TIME MEC WAS BUSY - 650330. USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC - 0.

NUMBER OF HOPKIN TO TASK MEMORY LOADS - 1318
TOTAL TIME SPENT LOADING TASK MEMORY - 231614. USECS

NUMBER OF DATA REQUESTS - 2001
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY - 240748. USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED - 675568. USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES - 351457. USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 2799. USECS

NUMBER OF SEGMENT REFERENCES - 5770
NUMBER OF PAGE FAULTS - 0
NUMBER OF PAGE JUMPS - 5770
    
```

Fig. D49—Triple processor simulation results for the further expanded GE workload using a 4096-word nonpaged TM, a dedicated software MEC, and a shared program/data bus

```

ELAPSED TIME = 1000000, USECS

TOTAL PMS ASSIGNED = 618

PM 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
NUM 334 50 20 10 10 10 10 1 1 1 1 20 20 20 20 20 20 20 10
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
NUM 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE * IN MSECS
MSC 2 19 49 67 67 73 48 961 67 65 64 24 21 21 21 21 21 21 21 48
SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE * IN MSECS
MSC 2 19 48 66 64 73 48 961 67 65 64 24 21 20 20 20 20 19 19 47

INTERRUPT DATA
INT 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 1 0 131 0 0 0 1318 2061 2061 0 0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0,3 USECS
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 7, USECS
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 27932, USECS

MEC ROUTINE DATA
RBU 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 0 0 1310 373 1416 5252 1318 4582 2061 0 0
AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE * IN USECS
USC 2 0 0 2 24 19 3 5 5 3 0 0
LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE * IN USECS
USC 23 0 0 34 430 544 63 42 54 41 0 0
TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE * IN MSECS
MSC 26,0 0,0 0,0 13,4 13,4 38,8 78,8 19,8 68,7 30,9 0,0 0,0
AVERAGE TIME EACH ROUTINE IS IDLE BY INTERRUPTS * IN USECS
USC 0,6 0,0 0,0 0,4 0,4 0,7 0,6 0,2 0,6 0,2 0,0 0,0
LONGEST TIME EACH ROUTINE IS IDLE BY INTERRUPTS * IN USECS
USC 7 0 0 3 3 7 7 7 7 7 0 0

CPL DATA
CPU 1 2 3
USC 809976, 575859, 406824,
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 1046343, USECS

TOTAL TIME MEC WAS BUSY * 317519, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC * TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 8,
NUMBER OF BORAM TO TASK MEMORY LOADS = 1318
TOTAL TIME SPENT LOADING TASK MEMORY = 231614, USECS

NUMBER OF DATA REQUESTS = 2061
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 240748, USECS
TOTAL TIME PROCESSORS ARE IDLE WAITING FOR DATA REQUESTS TO BE SATISFIED = 394781, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 107084, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 799, USECS

NUMBER OF SEGMENT REFERENCES = 5770
NUMBER OF PAGE FAULTS = 0
NUMBER OF PAGE JUMPS = 5770

```

Fig. D50—Triple processor simulation results for the further expanded GE workload using a 4096-word nonpaged TM and a dedicated hardware MEC

```

ELAPSED TIME = 1000000. USECS

TOTAL PMS ASSIGNED = 618

PM 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
NUM 334 50 20 10 10 10 10 1 1 1 1 20 20 20 20 20 20 20 20 10
NUMBER OF TIMES EACH PM MISSED ITS COMPLETION DEADLINE
NUM 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
MSC AVERAGE TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE = IN MSECS
MSC 2 19 43 60 58 72 36 937 57 55 52 25 19 18 18 18 18 17 17 37
MSC SHORTEST TIME BY WHICH EACH PM BEAT ITS COMPLETION DEADLINE = IN MSECS
MSC 1 18 35 58 50 72 34 937 57 45 52 25 17 17 16 15 15 14 13 37

INTERRUPT DATA
INT 1 2 3 4 5 6 7 8 9 10 11 12
NUM NUMBER OF TIMES EACH INTERRUPT IS SERVICED BY THE MEC
NUM 1000 1 0 1318 0 0 0 1318 2061 2061 0 0
MSC AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0.3 USECS
MSC LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 6. USECS
MSC TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 27932. USECS

MEC ROUTINE DATA
ROU 1 2 3 4 5 6 7 8 9 10 11 12
NUM NUMBER OF TIMES EACH MEC ROUTINE IS PROCESSED
NUM 1000 0 0 1318 373 1554 8498 1318 11740 2061 0 0
MSC AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE = IN USECS
MSC 3 0 0 2 77 42 4 4 7 5 0 0
MSC LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE = IN USECS
MSC 25 0 0 33 850 962 74 46 74 43 0 0
MSC TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE = IN MSECS
MSC 26.0 0.0 0.0 13.2 13.4 37.3 127.5 19.8 176.1 30.9 0.0 0.0
MSC AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS = IN USECS
MSC 0.7 0.0 0.0 0.2 0.7 0.5 0.6 0.3 0.5 0.2 0.0 0.0
MSC LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS = IN USECS
MSC 10 0 0 7 7 7 7 7 10 3 0 0

CPU DATA
CPU 1 2 3
MSC TOTAL TIME EACH CPU IS ASSIGNED = IN USECS
MSC A00873. 666237. 575199.
MSC TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 1046343. USECS

TOTAL TIME MEC WAS BUSY = 472091. USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0.

NUMBER OF BORAW TO TASK MEMORY LOADS = 1318
TOTAL TIME SPENT LOADING TASK MEMORY = 231614. USECS

NUMBER OF DATA REQUESTS = 2061
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 240748. USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 575593. USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 284462. USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 1024. USECS

NUMBER OF SEGMENT REFERENCES = 5770
NUMBER OF PAGE FAULTS = 0
NUMBER OF PAGE JUMPS = 5770
    
```

Fig. D51—Triple processor simulation results for the further expanded GE workload using a 4096-word nonpaged TM, a dedicated hardware MEC, and a shared program/data bus

ELAPSED TIME = 10800001 USECS

TOTAL PMS ASSIGNED = 410

PM	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
NUM	334	50	20	10	10	10	10	1	1	1	1	20	20	20	20	20	20	20	20	10
NUM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MSC	2	19	43	63	59	73	39	954	60	58	56	25	14	13	12	11	11	11	11	27
MSC	1	18	34	61	57	73	36	954	60	58	56	25	13	12	12	11	11	11	11	25

INTERRUPT DATA

INT	1	2	3	4	5	6	7	8	9	10	11	12
NUM	1000	1	7088	1318	0	0	0	7088	2061	2061	0	0
USC	AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0,3 USECS											
USC	LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 7, USECS											
USC	TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 74221, USECS											

MEC ROUTINE DATA

RBU	1	2	3	4	5	6	7	8	9	10	11	12
NUM	1000	0	7088	1318	373	1558	13050	7088	4688	2061	0	0
USC	AVERAGE TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE = IN USECS											
USC	LONGEST TIME EACH ROUTINE WAITS IN QUEUE FOR SERVICE = IN USECS											
MSC	TOTAL TIME MEC IS BUSY PROCESSING EACH TYPE OF ROUTINE = IN MSECS											
USC	AVERAGE TIME EACH ROUTINE IS IDLED BY INTERRUPTS = IN USECS											
USC	LONGEST TIME EACH ROUTINE IS IDLED BY INTERRUPTS = IN USECS											

CPU DATA

CPU	1	2	3
USC	TOTAL TIME EACH CPU IS ASSIGNED = IN USECS		
USC	864062,	731685,	625995,
USC	TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 1046343, USECS		

TOTAL TIME MEC WAS BUSY = 602966, USEC

FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0,

NUMBER OF BORAM TO TASK MEMORY LOADS = 7088

TOTAL TIME SPENT LOADING TASK MEMORY = 269344, USECS

NUMBER OF DATA REQUESTS = 2061

TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 240748, USECS

TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 438109, USECS

TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 142945, USECS

LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 574, USECS

NUMBER OF SEGMENT REFERENCES = 7088

NUMBER OF PAGE FAULTS = 7088

NUMBER OF PAGE JUMPS = 9770

Fig. D52—Triple processor simulation results for the further expanded GE workload using a 1024-word paged TM and a dedicated hardware MEC

ELAPSED TIME = 1000000. USECS

TOTAL PMS ASSIGNED = 61A

PM	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
NUM	334	50	20	10	10	10	10	1	1	1	1	20	20	20	20	20	20	20	20	10
NUM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MSC	2	10	3A	60	48	72	28	914	51	4A	21	24	9	8	7	5	5	4	4	3
MSC	1	1A	17	60	16	72	25	914	51	4A	21	24	8	6	5	4	3	3	2	2

INTERRUPT DATA

INT	1	2	3	4	5	6	7	8	9	10	11	12
NUM	1000	1	708A	131A	0	0	0	708A	2061	2061	0	0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0.3 USECS												
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 7. USECS												
TOTAL TIME MFC IS BUSY PROCESSING INTERRUPTS = 74221. USECS												

MEC ROUTINE DATA

ROI	1	2	3	4	5	6	7	8	9	10	11	12
NUM	1000	0	708A	131A	373	1554	27450	708A	5459	2061	0	0
USC	7	0	4	5	130	73	9	8	14	9	0	0
USC	40	0	49	34	635	733	78	71	83	55	0	0
MSC	26.0	0.0	35.4	13.2	13.4	37.3	411.7	106.3	81.9	30.9	0.0	0.0
USC	1.9	0.0	0.7	0.7	4.5	1.4	1.1	0.3	1.0	0.2	0.0	0.0
USC	10	0	7	7	7	10	14	7	10	3	0	0

CPU DATA

CPU	1	2	3
USC	912667.	9082A3.	806237.
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 1046343. USECS			

TOTAL TIME MFC WAS BUSY = 830435. USEC

FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0.

NUMBER OF BORAM TO TASK MEMORY LOADS = 708B

TOTAL TIME SPENT LOADING TASK MEMORY = 269344. USECS

NUMBER OF DATA REQUESTS = 2061

TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 240748. USECS

TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 477476. USECS

TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 179277. USECS

LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 624. USECS

NUMBER OF SEGMENT REFERENCES = 708B

NUMBER OF PAGE FAULTS = 708B

NUMBER OF PAGE JUMPS = 5770

Fig. D53—Triple processor simulation results for the further expanded GE workload using a 1024-word paged TM, a dedicated hardware MEC, and a shared program/data bus

```

ELAPSED TIME = 1000000, USECS

TOTAL PMS ASSIGNED = 618

PH 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
NUM 334 50 20 10 10 10 10 1 1 1 1 20 20 20 20 20 20 20 20 10
NUM 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
MSECS 2 19 49 66 62 73 49 956 62 60 58 25 15 14 14 14 14 14 14 32
MSECS 1 18 45 65 57 73 44 956 62 60 58 25 14 14 14 14 13 13 29

INTERRUPT DATA
INT 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 1 6174 1318 0 0 0 6174 2061 2061 0 0
MSECS 0.3 7 67640

MFC ROUTINE DATA
RBU 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 0 6174 1318 373 1484 10160 6174 4372 2061 0 0
MSECS 3 0 3 3 30 21 8 6 10 5 0 0
MSECS 24 0 51 37 260 147 85 58 91 55 0 0
MSECS 24.0 0.0 30.9 13.4 13.4 38.1 152.4 92.6 65.6 30.9 0.0 0.0
MSECS 1.7 0.0 0.4 0.6 3.6 1.4 1.2 0.4 1.0 0.8 0.0 0.0
MSECS 10 0 7 7 10 10 10 7 10 7 0 0

CPU DATA
CPU 1 2 3
MSECS 833764 693128 520800
MSECS 1046343

TOTAL TIME MEC WAS BUSY = 530687, USEC
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0,
NUMBER OF JOHAM TO TASK MEMORY LOADS = 6174
TOTAL TIME SPENT LOADING TASK MEMORY = 234612, USECS
NUMBER OF DATA REQUESTS = 2061
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 240748, USECS
TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 420493, USECS
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 127592, USECS
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 592, USECS
NUMBER OF SEGMENT REFERENCES = 7088
NUMBER OF PAGE FAULTS = 6174
NUMBER OF PAGE JUMPS = 5770
    
```

Fig. D54—Triple processor simulation results for the further expanded GE workload using a 2048-word paged multiprogrammed TM and a dedicated hardware MEC

```

ELAPSED TIME = 100400. USECS

TOTAL PMS ASSIGNED = 015

PM 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
NUM 331 50 20 10 10 10 10 1 1 1 1 20 20 20 20 20 20 20 20 10
NUM 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
MSC 2 19 42 61 53 73 36 928 52 49 32 25 10 10 10 9 8 8 8 12
MSC 1 10 31 59 22 73 34 928 52 49 32 25 9 8 7 5 5 4 4 10

INTERRUPT DATA
INT 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 1 6116 1315 0 0 0 6116 2058 2058 0 0
MSC 0.3 7. 67190.

```

MEC ROUTINE DATA

```

RQU 1 2 3 4 5 6 7 8 9 10 11 12
NUM 1000 0 6116 1315 377 1958 23415 6116 5268 2058 0 0
MSC 5 0 4 4 123 62 8 8 14 7 0 0
MSC 31 0 43 36 1094 1187 86 66 71 55 0 0
MSC 26.0 0.0 30.6 13.1 18.4 37.4 351.2 91.7 79.0 30.9 0.0 0.0
MSC 2.0 0.0 0.5 0.7 3.9 1.5 1.0 0.3 1.0 0.2 0.0 0.0
MSC 10 0 7 7 10 10 14 7 10 7 0 0

```

CPU DATA

```

CPU 1 2 3
MSC 867839. 836529. 710950.
MSC 1044693.

```

TOTAL TIME MEC WAS BUSY - 740739. USEC  
FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC - TOTAL TIME PMS WERE INTERRUPTED BY THE MEC - 0.

NUMBER OF BORAH TO TASK MEMORY LOADS - 6116  
TOTAL TIME SPENT LOADING TASK MEMORY - 232408. USECS

NUMBER OF DATA REQUESTS - 2058  
TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY - 240649. USECS  
TOTAL TIME PROCESSORS ARE IDLE WAITING FOR DATA REQUESTS TO BE SATISFIED - 464729. USECS  
TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES - 169147. USECS  
LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE - 1265. USECS

NUMBER OF SEGMENT REFERENCES - 7085  
NUMBER OF PAGE FAULTS - 6116  
NUMBER OF PAGE JUMPS - 5770

Fig. D55—Triple processor simulation results for the further expanded GE workload using a 2048-word paged multiprogrammed TM, a dedicated hardware MEC, and a shared program/data bus



ELAPSED TIME = 100000, USECS

TOTAL PMS ASSIGNED = 618

PM	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
NUM	334	50	20	10	10	10	10	1	1	1	1	20	20	20	20	20	20	20	20	20
NUM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MSC	2	19	49	65	63	73	49	956	62	60	58	25	21	21	20	20	20	20	20	51
MSC	1	19	49	65	57	73	47	956	62	60	58	25	16	16	15	15	15	14	14	50

INTERRUPT DATA

INT	1	2	3	4	5	6	7	8	9	10	11	12
NUM	1000	1	2240	1310	0	0	0	2240	2061	2061	0	0
AVERAGE TIME ALL INTERRUPTS WAIT IN QUEUE FOR SERVICE = 0,2 USECS												
LONGEST TIME ANY INTERRUPT WAITS IN QUEUE FOR SERVICE = 7, USECS												
TOTAL TIME MEC IS BUSY PROCESSING INTERRUPTS = 39316, USECS												

MEC ROUTINE DATA

ROU	1	2	3	4	5	6	7	8	9	10	11	12
NUM	1000	0	2240	1310	373	1624	6542	2240	5395	2061	0	0
USC	2	0	2	2	19	20	5	5	7	4	0	0
USC	27	0	44	32	445	331	63	58	68	41	0	0
MSC	26,0	0,0	11,2	13,2	13,4	39,0	90,1	33,6	80,9	30,9	0,0	0,0
USC	0,9	0,0	0,3	0,3	1,2	0,7	0,7	0,3	0,7	0,3	0,0	0,0
USC	7	0	7	7	10	10	10	7	10	7	0	0

CPL DATA

CPU	1	2	3
USC	776992,	562824,	401940,
TOTAL TIME ALL PROCESSORS SPENT EXECUTING INSTRUCTIONS = 1046343, USECS			

TOTAL TIME MEC WAS BUSY = 385670, USEC

FOR A SIMPLEX PROCESSOR WITH A FLOATING MEC = TOTAL TIME PMS WERE INTERRUPTED BY THE MEC = 0.

NUMBER OF BORAM TO TASK MEMORY LOADS = 2240

TOTAL TIME SPENT LOADING TASK MEMORY = 85120, USECS

NUMBER OF DATA REQUESTS = 2061

TOTAL TIME SPENT TRANSFERRING DATA BETWEEN RAMM AND TASK MEMORY = 240748, USECS

TOTAL TIME PROCESSORS ARE IDLED WAITING FOR DATA REQUESTS TO BE SATISFIED = 421584, USECS

TOTAL TIME DATA REQUESTS WAIT IN QUEUE FOR RAMM MODULES = 131566, USECS

LONGEST TIME ANY DATA REQUEST WAITS IN QUEUE FOR RAMM MODULE = 1265, USECS

NUMBER OF SEGMENT REFERENCES = 7088

NUMBER OF PAGE FAULTS = 2240

NUMBER OF PAGE JUMPS = 5770

Fig. D57—Triple processor simulation results for the further expanded GE workload using a 4096-word paged multiprogrammed TM, a dedicated hardware MEC, and a shared program/data bus



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13. ABSTRACT  Simulation of a proposed naval Advanced Avionic Digital Computer (AADC) has been underway to arrive at architectures which efficiently meet the needs of expected program workloads. Models of avionic program workloads have been derived from various sources and used to drive these simulations. These models consist of sets of nearly independent program modules which effect periodic, known demands on system resources.  Simplex and multiprocessor configurations of the AADC have been modeled, and certain features of proposed AADC executive operation have been incorporated into these models. Guided by previous simulation work, both nonpaged and paged operating systems with multiprogrammed memories have been simulated.  The simplex processor achieves the highest percentage of processor utilization and, with multiprogramming, the lowest level of program transfer overhead. The effectiveness of multiprogramming in the multiprocessor configurations does not match that experienced with the simplex processor, but this effectiveness might be boosted by compartmenting program workloads into separate families under different processing elements.  Under full processor utilization, background executive activities such as system timing account for less overhead than direct executive functions controlling program execution. Sharing of the processing element by executive and program workload thus appears an effective strategy for a simplex system. Multiprocessor demands on the executive indicate that a dedicated executive processor is reasonable for multiprocessor configurations under full workloads.			

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Advanced Avionics Digital Computer (AADC) Simulation Simulator routines Computer system performance Computer programs Simscript Multiprocessors Avionics						
<p>Sharing of busing resources by both data and program transfers appears to offer an acceptable cost-efficiency tradeoff in dual and triple processor operation, but a triple processor would profit more, if cost reduction is paramount, by maintaining separate busing and relinquishing possible hardware executive features for a dedicated software executive.</p>						