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The Four-Frequency Radar Master Console II

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The completion of the master console for the airborne four-frequency radar system, to be used in NRL's wave-propagation studies, was assumed by NRL and has been described previously. Four displays were incorporated into a single console, along with the transmitter, receiver, and antenna-drive control functions. Two cathode-ray tubes present the B and PPI scans, while a third presents dual traces representing linear A sweeps. The initial design required 1.2 kw at 400 cps, lacked adequate display linearities, and presented maintenance problems when installed aboard aircraft. The new console design uses transistor and vacuum-tube modular units. Power requirements were reduced to 1/4 of that used in the original console. Video-amplifier rise times of less than 35 nanoseconds were achieved using transistor circuits. Display distortion and defocusing were materially reduced, and all gain controls are linear.

INTRODUCTION

Background

In conjuction with the commercially contracted development of the airborne four-frequency radar (4FR) system to be used in NRL's wave-propagation studies, the completion of the master console was assumed by NRL and has been described previously.* Four displays were incorporated into a single console, along with the transmitter, receiver, and antenna-drive control functions. Two cathode-ray tubes present the B and PPI scans, while a third displays dual traces representing linear A sweeps. Switching facilities were provided for the various video, trigger, and polarization signals available in the radar system. The time schedule accepted for the delivery of the original master console precluded making major decisions on the choice of cathode-ray tubes, video and trigger switching techniques, vacuum-tube circuits, and chassis designs. The original master console was completed in September 1962 and incorporated into the four-frequency radar system. Design of the other consoles to be included in the radar system was then started.

Accomplishments

The new console designs were developed to use transistor and vacuum-tube modular units. Vacuum tubes were used where their characteristics proved superior. The A-scope presentation used a cathode-ray tube with higher vertical sensitivity and lower deflection-plate capacity than the crt used in the original master console, thus allowing the A video amplifiers to be designed to use transistors. The video switching employs reed-type relays in order to simplify the coaxial wiring and the crosstalk noted previously.* The input power requirements to the new consoles were reduced to less than 1/4 of that of the original master console. Because the new console design incorporated many improvements and superior performance, the first new console (No. 1) replaced the original master console. The second console (No. 2) is identical to No. 1, except for the unrelated 4FR units installed in the console frame. Consequently, console No. 2 can assume the master control functions whenever required.

CIRCUIT DIAGRAMS

The 4FR console function diagram is shown in Fig. 1.† The trigger-pulse lines T_1 (P band), T_2 (L band), T_3 (C band), and T_4 (X band) terminate with 100-ohm resistors. These outputs are selected by frequency-selector relays controlled by the operator from the front panel for the PPI, A1, A2, and B cathode-ray-tube displays. The

NRL Problem R07-02; Project RR 008-01-41-5550. This is a final report on one phase of the problem; work on related phases is continuing. Manuscript submitted December 26, 1963.

*F.R. Fluhr, "Four-Frequency Radar Master Console," NRL Report 5922, June 7, 1963.

†All figures are bound consecutively at the end of this report.

selected trigger is then passed through the trigger buffer, unit 13. A summed output from unit 13 is used to drive the trigger delay buffer in unit 14. The delayed summed trigger from unit 14 then drives the normal sweep generator, unit 11. The four outputs from unit 13 go to the corresponding cathode-ray-tube (crt) unblanking units (units 26, 27, 28, and 29 in Fig. 1). An undelayed summed trigger from unit 14 is used to release the PPI clamp switch, unit 4. This eliminates the starting transient on the PPI display. The delayed-trigger line, upon which all delayed triggers appear in sequence from the radar synchronizer, passes through the delayed-trigger buffer, unit 31, located in the main junction box. The buffer, unit 31, drives the expanded sweep generator, unit 12, in the console and provides a delayed trigger signal to console no. 2. The radar polarization signals drive the polarization buffers in unit 14. The outputs of the polarization buffers go to the polarization-selector relays. The selected polarization signals then go to the corresponding unblanking units. The selection of the horizontal polarization signal results in the inhibiting of the trigger pulse to the unblanking circuit during the vertical polarization period, and vice versa. When a display is set to view both polarizations being received by the radar receiver, no signal is applied to that unblanking unit.

When the console is being operated, the frequency-selector switches are set to the desired positions. The selected trigger pulses drive the buffers in unit 13 and in addition produce a summed trigger output which is delayed by unit 14, which then triggers the normal sweep generator. The sweep-period pulse and the (sawtooth) sweep signal are then presented to the sweep-selector relays. These relays are controlled by the operator to select the normal or expanded sweep signal, which is presented to the corresponding A1, A2 horizontal deflection amplifiers, and the B vertical deflection amplifier. The expanded-sweep-generator unit is identical to the normal sweep-generator unit, except for the length of sweep generated and the delay in its starting time. The sweep-selector relays also connect the corresponding sweep-period pulse to the proper unblanking unit. An additional set of relays selects the corresponding dynamic focus signal for the associated crt display. Since the PPI display does not use the expanded sweep, the normal sweep-period pulse goes directly to the PPI unblanking unit 26, and the dynamic focus goes directly to the PPI crt focus grid.

The signal from the unblanking unit is a negative pulse starting at the trigger and stopping at the end of the sweep. This pulse is coupled to its corresponding crt cathode through a high-voltage capacitor. This pulse, which is dc restored, raises the bias level of the crt and allows the selected sweep period to be brightened on the crt.

The sweep from the normal sweep generator, unit 11, provides the signal to the sine-cosine potentiometer-driven unit 2. This unit drives the sine-cosine potentiometer resistive element, which resolves the normal sweep into the vertical and horizontal sweeps required for the PPI display. The antenna-follower servoamplifier, unit 1, and the servo motor assembly mounted on unit 15 cause the rotation of the sine-cosine potentiometer to follow the radar antenna motion. The servo input signals are designated as the S1, S2, S3 inputs. An ac servo error signal from the radar antenna is inserted into the antenna-follower servo to correct for the dynamic errors of the antenna-control servo; this lack of correction would otherwise degrade the PPI display, since the antenna sweeps in both directions.

The horizontal deflection of the B scope is derived from the antenna sawtooth generator, which controls the radar-antenna drive circuits. Error signals, derived from the antenna sweep error and antenna follow-up error by the antenna error demodulator, unit 6, are summed with the antenna sweep signal in the horizontal B-scope deflection amplifier. Two error signals are required for the B scan, because the radar antenna mechanical drive system has a follow-up error and the antenna sawtooth generator has an independent follow-up error. Both of these error signals must be removed from the B-scan deflection so that each target will appear at the proper point on the crt, whether the antenna is scanning clockwise or counterclockwise.

The radar video is derived from two receivers for each of the four frequencies, one for the horizontally and one for the vertically polarized radar returns. The video is processed by the radar system, to provide for displaying both the direct and gated video in five forms: (a) horizontal and (b) vertical polarization amplitudes, (c) horizontal and (d) vertical phases compared against

a local reference, and (e) the horizontal versus the vertical relative phase. The video switching provides only the direct ungated video for the PPI and B scopes. The A1 and A2 scopes can be switched to present any of the 15 video sources provided by the radar processing equipment. This switching is accomplished by the use of video relays located in the main junction box. The selected video to the four displays comes from the video buffer, unit 30, also located in the main junction box.

The PPI and B scope video amplifiers drive the grids of the crt displays. Provisions are made to present range marks through these amplifiers. The A1 and A2 scope video amplifiers provide push-pull output signals which drive the vertical deflection plates of these crt displays. The range marks are presented with the positive polarity being upward. The range gates are displayed with positive polarity downward. The phase video signals (Hϕ, Vϕ, Hϕvs Vϕ) possess both polarities (bipolar), while the unipolar amplitude video (HA, VA) is presented positive upward.

Figure 1 also includes all of the gain, centering, brightening, delaying, and switching circuits necessary to control the crt displays. The wiring numbers, terminal designations, and unit pin numbers are shown where applicable.

DESCRIPTION OF MODULAR UNITS

Unit 1—Antenna Follower Servoamplifier

The antenna follower amplifier, unit 1, in Fig. 2 provides the necessary amplification for the antenna follower sine-cosine resolver as shown in Fig. 1. This unit operates in conjunction with unit 15 (Figs. 1 and 12). The servoamplifier is a modified plug-in integrator servoamplifier salvaged from an AN/SPS-T2 radar trainer.

Unit 2—PPI Sine-Cosine Potentiometer Driver

The normal sweep is converted to a push-pull signal by the input tube and then applied to two output cathode-follower circuits after passing through a biasing network (Fig. 3). The outputs of the cathode followers then drive the sine-cosine potentiometer in unit 15, (Fig. 1).

Units 3, 5—PPI Vertical and Horizontal Sweep Clamp and Centering

Clamping and centering for the sweep outputs of the PPI deflections amplifiers (units 16 and 17) are controlled by unit 3 for the horizontal crt deflection plates, and unit 5 for the vertical crt deflection plates. The circuit for the identical units is shown in Fig. 4. The clamping is done by dual triodes connected cathode to anode. The signal from the clamp switch, unit 4. The clamps are released before the start of the sweeps so that the switching transients will not be present on the PPI display.

Unit 4—PPI Clamp Switch

The PPI clamp switch unit (Fig. 5) generates the signal which releases the clamps on the PPI sweeps. The undelayed summed trigger from unit 14 is amplified and inverted by Q1 and causes Q3 to be cut off and Q4 to conduct. The negative sweep-period pulse from unit 11 is differentiated and amplified by Q2. This signal cuts Q4 off and turns Q3 on. The signal generated at the collerctor of Q3 is buffered by Q5.

Unit 6—Error-Signal Demodulator

The error signals from the antenna follow-up and antenna-sweep follow-up are 400-cps suppressed-carrier signals. The demodulators use a phase-referenced bridge type demodulator, which is then filtered (Fig. 6). The error-signal inputs and outputs are buffered by cathode followers. The 400-cycle phase reference must correspond to the same phase used in the antenna servo system.

Units 7, 8, 10—A1-A2 Horizontal Centering and B Vertical Centering

The sweeps from the corresponding deflection amplifiers are centered and dc-restored (Fig. 7). The dc restoration is accomplished by dual diodes, which clamp the push-pull sweeps to the centering voltages formed across the 2-μf capacitors.

Unit 9—Dynamic Focusing

Because a large portion of the crt screen was to be used, a means of maintaining crt focus over larger ranges of deflection was incorporated. A one-tube amplifier employing a small amount of

high-frequency feedback was employed at the focusing grid (Fig. 8). The curve of the signal is an approximation of the variation required on the focus grid to maintain spot focus over the usable portion of the crt screen.

Units 11, 12—Sweep Generator

The sweep generator (Fig. 9) uses a bootstrap linear sweep circuit controlled by a flip-flop. The trigger pulse is inverted and amplified by Q1, which then turns Q2 of the flip-flop off. Transistor Q3 starts to conduct and in turn cuts VA off. The sweep circuit starts generating the sawtooth waveform in the bootstrap circuit. The charging capacitors are external to the sweep-generator unit (Fig. 1). The sweep output from VB is fed back to Q4, which is biased off. When the sweep reaches the set amplitude, Q4 goes into conduction and stops the conduction of Q3, thereby restoring the flip-flop. When Q3 turns off, VA goes into conduction and discharges the charging capacitor in the sweep circuit. When the charging capacitor is fully discharged, the sweep generator is ready for the next trigger pulse. Transistor Q5 buffers the waveform at the collector of Q2 and thus provides the positive sweep-period pulse. Since the negative sweep-period pulse is used only at unit 4 from the normal sweep generator (Fig. 1), it is not buffered. A diode is used in the base circuit of Q4, so that the reverse emitter base-voltage rating will not be exceeded.

Unit 13—Trigger Buffer

The trigger buffer unit (Fig. 10) consists of four inverting transistor amplifiers, one for each of the four frequencies. A logical diode OR circuit sums the selected pretrigger signals prior to being delayed in unit 14. Feedback is employed at the input to each amplifier in order to raise the input impedance of the circuit.

Unit 14—Trigger Delay and Polarization Buffer

In Fig. 11, the selected summed pretrigger is amplified and inverted by Q1, which then drives the buffer transistor Q2. The output of Q2 is used to drive the variable delay line and the PPI clamp switch (unit 4). The output of the delay line is buffered by Q3 before going on to the normal sweep generator (unit 11). The buffer circuit Q3 is provided with a feedback loop, which raises its input impedance.

Included in unit 14 are the two polarization-signal buffer circuits, Q4 through Q7. These circuits invert and amplify the input polarization signals, then drive the unblanking circuits through the polarization-selection relays, as shown in Fig. 1.

Unit 15—Servo-Sine/Cosine Potentiometer

The circuit for the servo motor-tachometer, follow-up control transformer, and sine/cosine potentiometer is shown in Fig. 12. This unit works in conjunction with units 1 and 2, as indicated in Fig. 1. Buffer cathode followers are provided at the outputs of the sine/cosine potentiometer.

Units 16, 17—PPI Horizontal and Vertical Deflection Amplifiers

In Fig. 13, the deflection amplifiers for the PPI display consist of dual-triode circuits connected as phase inverters, to provide the necessary push-pull output signal. Adjustments are provided in the unit for amplifier balance and for high- and low-frequency compensation in order to maintain sweep linearity.

Units 18, 19, 21—A1-A2 Horizontal and B-Scan Vertical Deflection Amplifiers

The deflection-amplifier circuit (Fig. 14) is nearly identical to that shown in Fig. 13. The difference is in choice of bias parameters which allow this amplifier to operate in a single direction, whereas the PPI deflection-amplifier outputs had to handle both positive- and negative-going sweeps. The circuit shown in Fig. 14 provides an unidirectional push-pull output sweep.

Units 20, K2W—B-Scan Horizontal Deflection Amplifier

The horizontal deflection amplifier for the B scan shown in Fig. 15 consists of two units. One unit is a Philbrick commercial K2W operational amplifier driving a phase-splitting output circuit. The dual-triode phase splitter is connected within the feedback loop and thus, with the K2W, forms an operational amplifier with a push-pull output. Remote gain control is accomplished by varying the feedback resistance. Provisions are made for summing the various antenna error signals at the input to the K2W.

Units 22, 25—B and PPI Video Amplifiers

The video amplifiers used for the B and PPI presentations are shown in Figs. 16 and 17. In Fig. 16, the amplifier is designed to take bipolar input video and provide bipolar output video. Gain control is obtained from one-hundred-ohm subminiature potentiometers which are terminating resistors for the coaxial input line. Range-mark mixing with the video is accomplished in the input stage by using two transistors, Q1 and Q2, driving a common collector load resistance. The output transistors, Q3 and Q4, are connected in a cascode configuration so that the output video voltage swings can be on the order of plus and minus 15 volts from the quiescent value. The rise time of the amplifier is less than 35 nanoseconds (nsec), and the voltage gain is greater than 20.

The video amplifier shown in Fig. 17 is similar to that used in Fig. 16, except that the input stage has been converted to a differential amplifier driving two high-speed switching diodes which perform the magnitude-selection process. The output stage is the same, except it is biased so that Q3 and Q4 conduct strongly and provide positive going output signals only. The range-mark signals are inserted into one of the differential amplifier inputs (Q2). Gain control is obtained in the same manner as in the circuit in Fig. 16. The two circuits are interchangeable in the console, depending on whether the bipolar or unipolar outputs are preferred.

Range-Gate Mixing

Because the two range-gate signals go to both the A1 and A2 video amplifiers, the range-gate mixing circuit in Fig. 18 was designed. The two gate lines are properly terminated, and the mixing is accomplished with high-speed switching diodes.

Units 23, 24—A1-A2 Video Amplifier

The input stage of the A1-A2 video amplifier (Fig. 19) is the same as that used in Fig. 17, except that an additional input for inserting range-gate signals is provided at the emitter of Q2. Transistors Q1 and Q2 form the input mixing amplifier stage. Transistor Q3 is the split-load phase inverter which drives the push-pull inputs of the output amplifier, consisting of Q4, Q5, Q6, and Q7. A similar type of cascode circuit is used in the output stages as was used in the B and PPI output stages, except that the emitters of Q4 and Q6 drive a common resistor. Each output is capable of providing a plus-to-minus swing of 30 volts, centered at the balanced quiescent point. Negative feedback is provided in order to minimize any distortion in the amplifier. The rise time of the amplifier is less than 35 nsec, and the voltage gain is greater than 25. Gain control is achieved as with the B and PPI video amplifiers, by use of subminiature potentiometers being used as the coaxial-line termination.

A1-A2 Vertical Centering, Clamping, and DC Restoration

The video signals from the A1 and A2 video amplifiers are clamped to the centering voltage, as indicated in the circuit in Fig. 20. The video signals are quickly dc restored to the centering voltages determined by the dual potentiometer. The keyed clamping signals from the unblanking units 27 or 28 also inhibit the clamping circuit during the unblanked portion of the display.

Units 26, 27, 28, 29—Unblanking

The circuit which accomplishes the unblanking function is shown in Fig. 21. This circuit takes the selected trigger, polarization, and sweep-period signals and provides the output signal which brightens the crt. The trigger signal and the polarization signal drive a logic AND circuit at the base of Q1. When both signals are present simultaneously, the trigger pulse is allowed to pass the Q1 buffer, where it is amplified and inverted by Q2. The output of Q2 causes Q4 of the flip-flop to go into conduction and Q5 to cease conducting. These outputs are used to drive the dc restoration clamp at the crt deflection plates, releasing them during the sweep period. The sweep-period pulse is differentiated in the base circuit of Q3, and the trailing edge of the sweep-period pulse is amplified and inverted by Q3. Transistor Q3 then drives Q5 of the flip-flop into conduction, thus causing Q4 to cease conducting. The time interval between the trigger and the trailing edge of the sweep-period pulse is the unblanking period for the normal sweep.

The waveform from Q5 and the sweep-period pulse are combined in a logical AND circuit at the base of Q6. The bias voltage of Q6 is also remotely controlled by the manual intensity control, which allows Q6 to conduct when the simultaneously present signals at the input to the AND circuit exceed the bias value. The output of Q6 drives the crt cathode circuit, causing the crt to brighten.

In the case of the expanded sweep, the trigger occurs long before the sweep period starts. In order not to allow all of the noise which will be present before the sweep starts to be brightened, the AND circuit in the base of Q6 was required. A hard dc clamp was installed on the output of Q6 in order to protect this circuit against transients occurring during console turn off.

B and PPI CRT Circuit

The B and PPI displays use the 5BFP7 crt, which is connected as shown in Fig. 22. The dc restoration diodes shown in the cathode and grid circuits are thermionic because solid-state diodes which would be sufficiently fast cannot withstand the system turnoff transients which are developed. When the bipolar output video is used, the diode in the crt grid circuit must be removed. Each crt is a dual-gun tube. Only one gun each is required for the B and PPI displays, so they have been wired to use different guns in their respective crt's. Thus if one of the guns in use in one of the tubes fails, the B and PPI tubes can be interchanged.

A1-A2 CRT Circuit

The A-scope presentation uses both guns in the 5AFP1 crt. This crt has a higher deflection sensitivity and lower deflection-plate input capacity than the crt used for the B and PPI displays. Because of the improved sensitivity, the A1 and A2 video amplifiers could be designed using transistors. The basic wiring (Fig. 23) is the same as that used for the B and PPI crts, except for the addition of a distortion control and the omission of the grid dc restoration diode.

Unit 30—Video Buffer

The video buffer unit, which is located in the main junction box, consists of four independent linear emitter follower circuits (Fig. 24). Emitter-to-base feedback is used in order to increase the input impedance of each emitter follower.

Unit 31—Delayed Trigger Buffer

The delayed-trigger buffer unit (Fig. 25) is also contained in the main junction box. The large delayed trigger from the 4F radar is clipped by the 12-volt zener diode before going to the buffer emitter-follower Q1. The output of Q1 drives two emitter followers, Q2 and Q3. The output of Q2 goes into the console and triggers the expanded sweep generator. The output of Q3 is used to provide the delayed trigger to console 2.

MASTER CONSOLE CONTROL CIRCUITS

The various control circuits used in the 4F radar are located in the master console (console 1). These circuits are shown in brief form in Fig. 26, indicating their terminations either in the master-console main junction or at the indicated 4F radar system terminal board. Explanation of these circuits will be covered in other reports on the 4F radar system. The rest of the circuits shown in Fig. 26 allow the console to be turned on and off from the front panel independently of the rest of the system, when the system itself is operating. To operate the 4F radar system, the Receiver Filament switch is turned on and the plate ON pushbutton is operated. This supplies the 28-volt dc power to the console plate-supply switch. Also the 400-cps ac power is applied through KAC to the heater transformers and the transistor power supplies. When the Plate Supply switch located on the front panel of the console is thrown on, the dc power supplied by the 4FR system is applied to the console. Relay A then closes and causes relay B to operate. The operation of relay B causes the transistor-circuit supply voltages to be connected through series resistors to the console circuits. Also B connects the +150 volts to the time-delay circuit on relay C. After a short time delay (approximately one second), relay C operates and energizes relay D, which operates and shorts the series resistors in the transistor supply-voltage leads. Relay E is then operated from relay D and allows the high-voltage crt power supplies to turn on. The purpose of the series line resistors is to load the transistor power supplies in steps, so that their overload mechanism will not operate during the turn-on of the console.

POWER-SUPPLY CIRCUITS

The power-supply circuits in the console consist of those for the transistor circuits, high-voltage crt circuits, and heater transformer circuits (Fig. 27). The remainder of the dc power required in the console is supplied by the 4FR. A high-voltage isolating diode is placed in series with the −2.5 kv line in order to isolate power-supply transients during console turn-off.

CONSOLE 1 (MASTER CONSOLE) CONFIGURATION

Figures 28 through 33 are pictures of the master console. Figure 28 shows a front view of the console in operation. The antenna controls and the range-gate control are shown at the bottom of the picture. Figure 29 is the same view as Fig. 28, except that the front panel is open, showing the control switching, the first 14 plug-in units, and the sweep-calibration capacitors. The rear view of the interior of the console is shown in Fig. 30. The deflection amplifier units are shown at the bottom, and the video amplifier and unblanking units are shown mounted between the crt's. The M-block terminal board is shown at the left, and the high-voltage manual cutoff switch is mounted above it. Figure 31 gives an overall rear view of the console, showing the other system components mounted in the console. A picture of the main junction box is given in Fig. 32. The video buffer and delayed-trigger buffer units are shown mounted just above the video-selection relays at the left side of the picture. The steering diodes for the video relays are mounted adjacent to the plug-in units. The console power relays are mounted under the terminal boards, and the transformer is used to excite the range-gate control potentiometer in the console. Representative examples of the modular units are given in Fig. 33. The units represent the three types in which all the active components are transistors, all the active components are vacuum tubes, and the active components are a combination of transistors and tubes. The units shown are an unblanking unit, an antenna-follower resolver driver unit, a sweep-generator unit, and an A1-A2 video-amplifier unit.

PERFORMANCE

The redesigned console requires less than one-fourth the power used by the original master console. The sweep lengths met the requirements of providing range scales of from 1/4 to 200 miles. The video amplifiers all provide pulse risetimes of less than 35 nsec. The gain controls on these amplifiers are stable, whereas the Raysistor controls on the original master console were not. The displays maintain reasonable focus over the entire visible face of the crt. Slight defocusing occurs at the edges of the crt's because of the variation of the dynamic focusing waveform from that actually required for each crt. All transistors are silicon in order to minimize temperature effects, and all tubes, except the deflection amplifiers, are of the premium subminiature variety. The only active components not mounted in removable modular units are the crt's.

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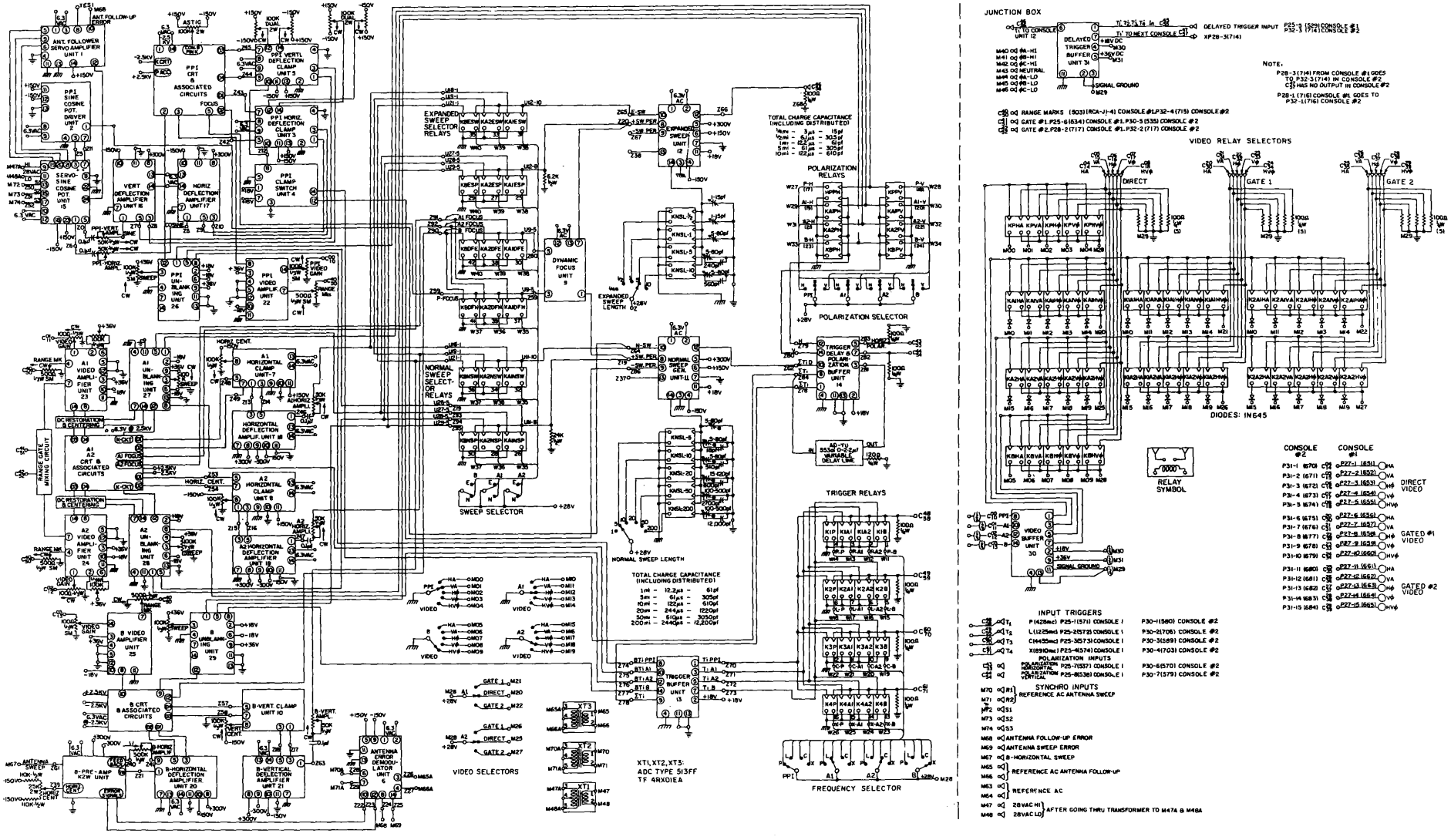

Fig. 1 - Four-frequency-radar master-console function diagram

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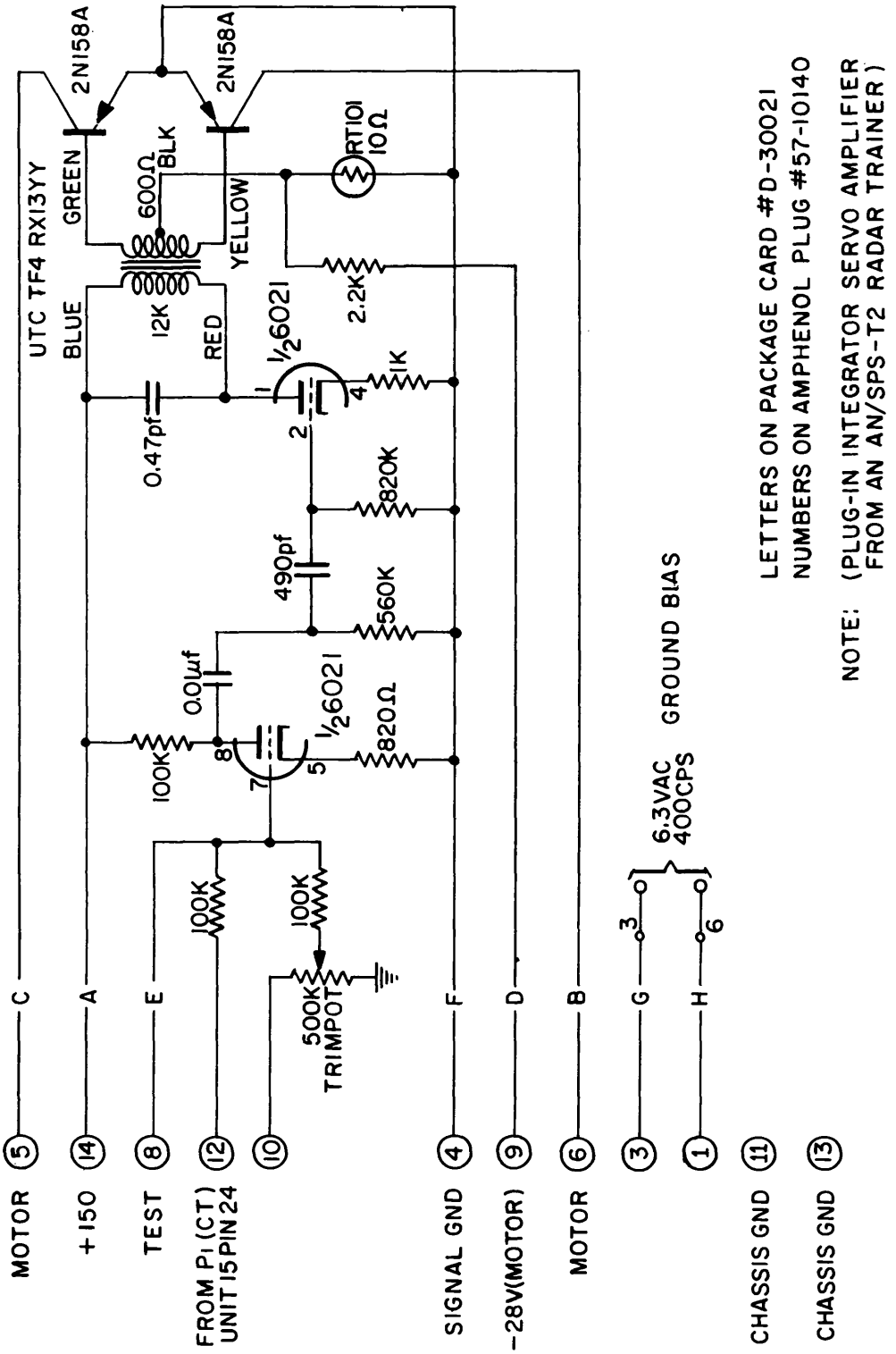


Fig. 2 - Unit 1—Antenna follower servoamplifier

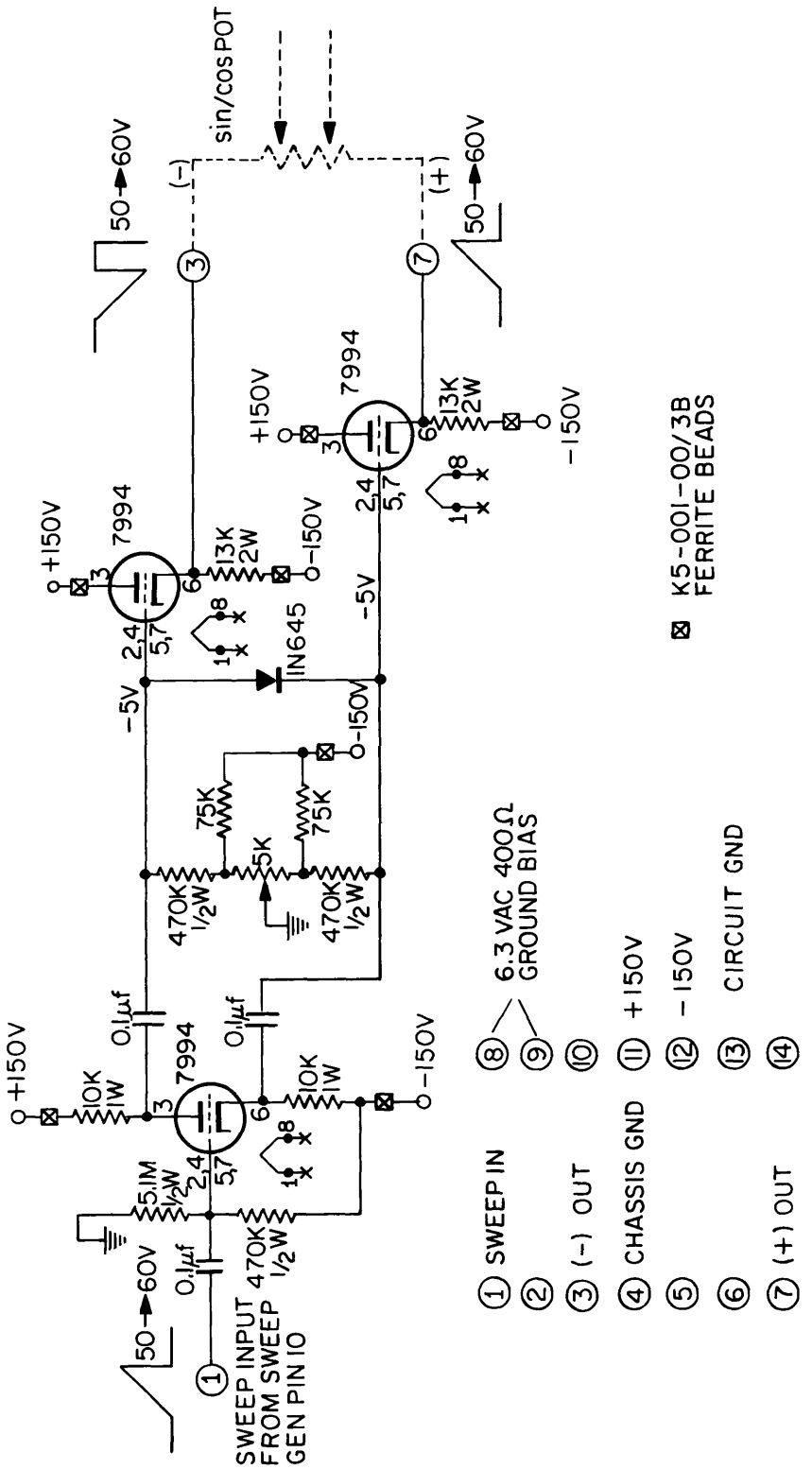


Fig. 3 - Unit 2—PPI sine/cosine potentiometer driver

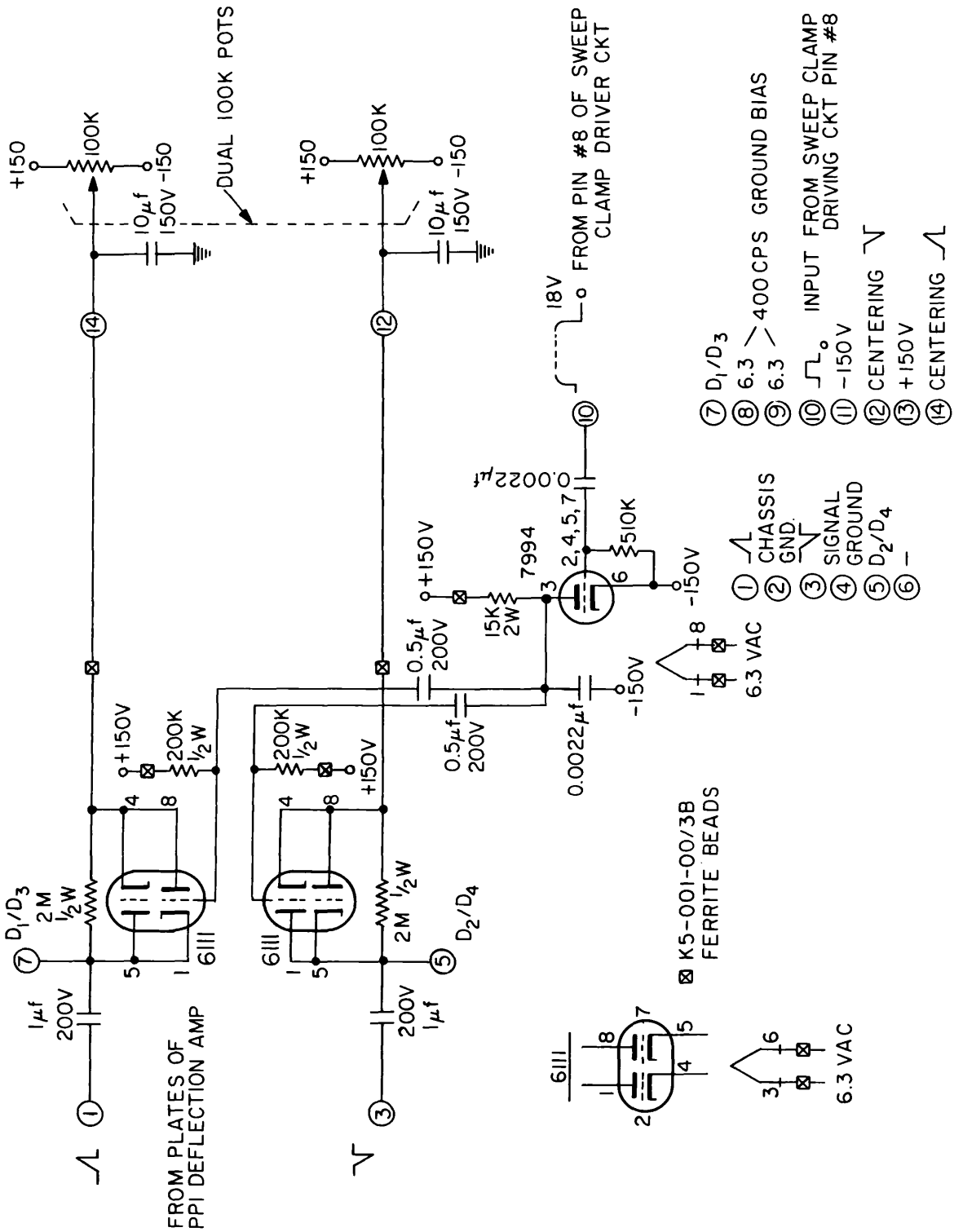


Fig. 4 - Units 3, 5—PPI vertical and horizontal sweep clamp on centering

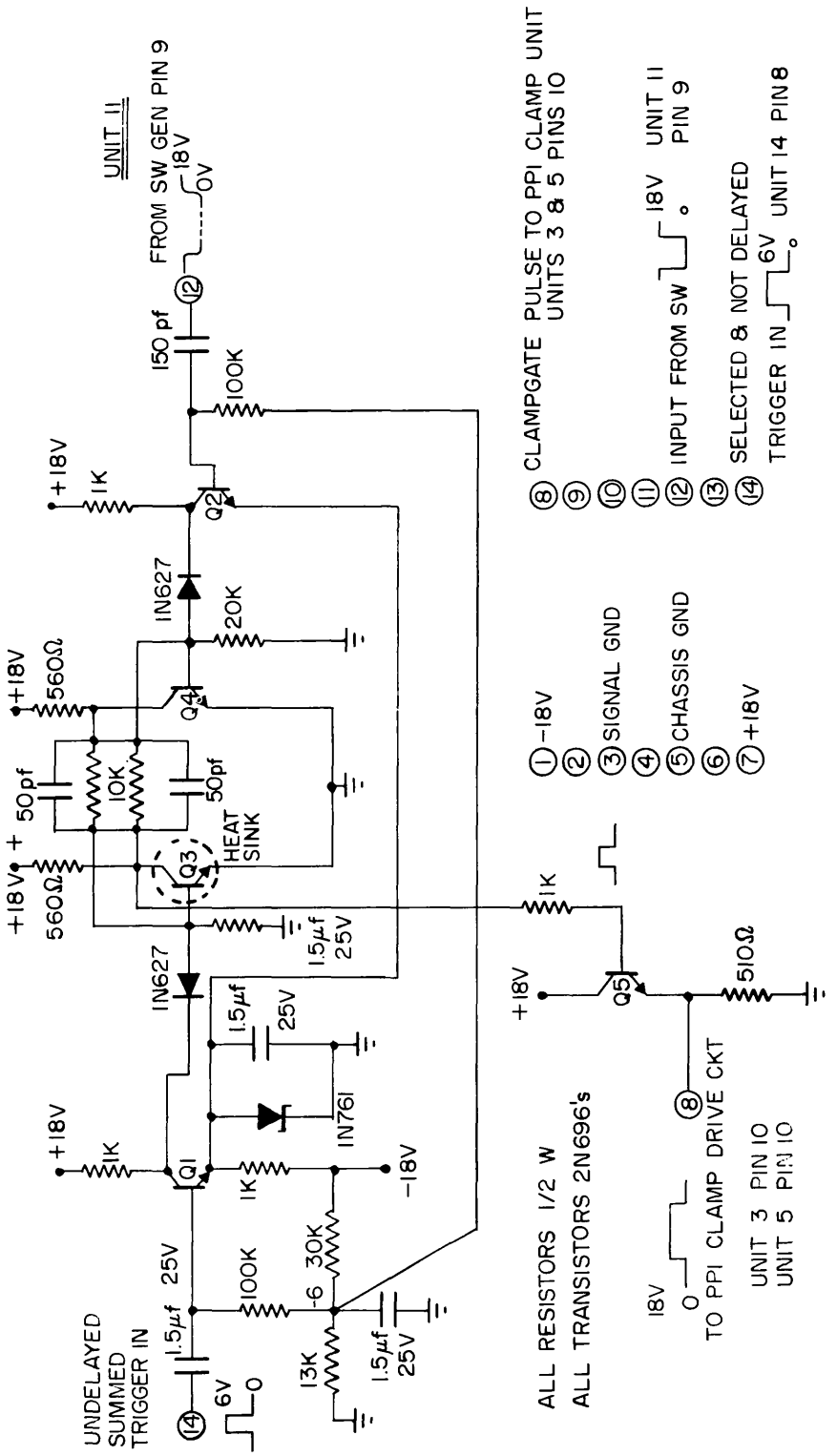


Fig. 5 - Unit 4—PPI clamp switch

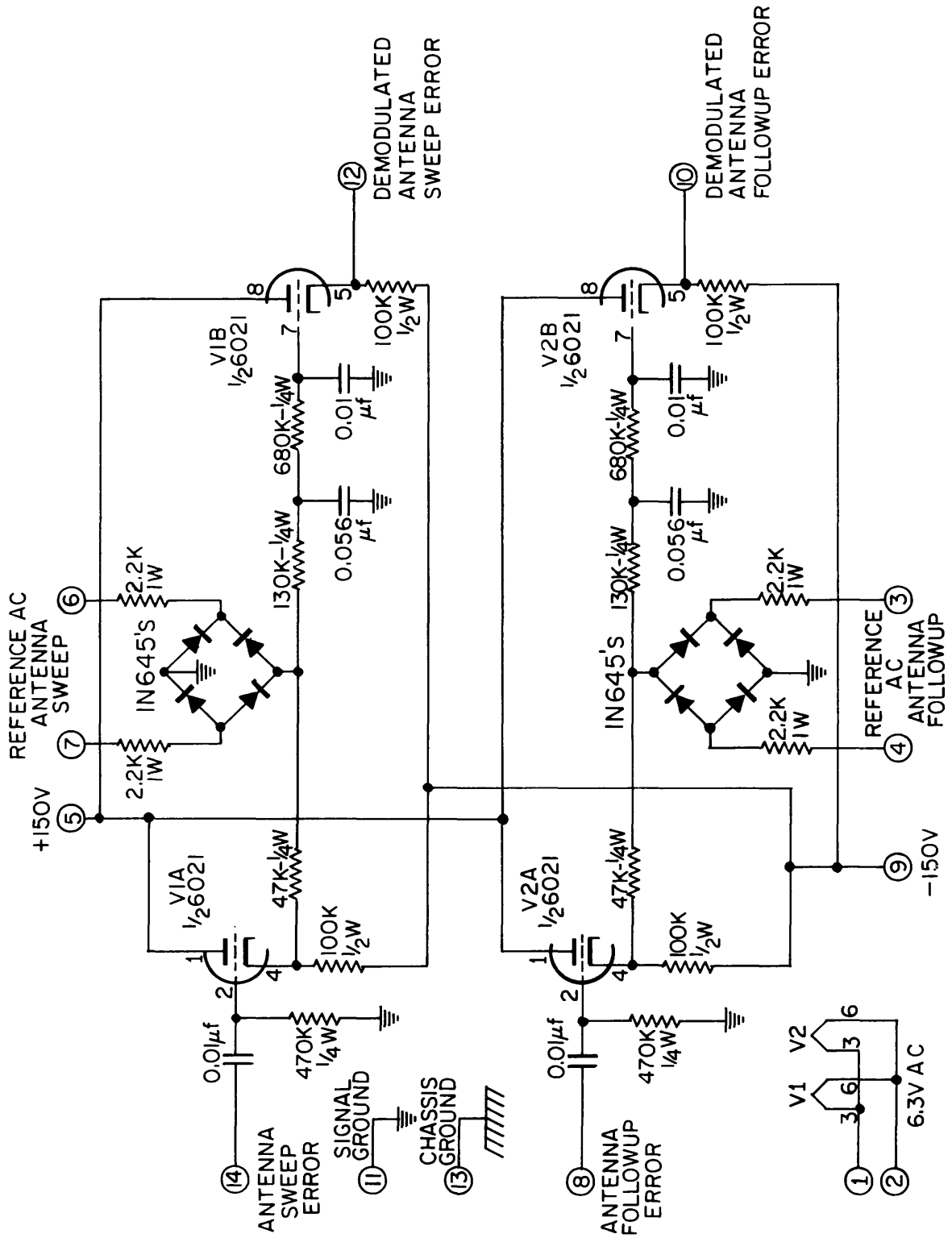


Fig. 6 - Unit 6—Error signal demodulator

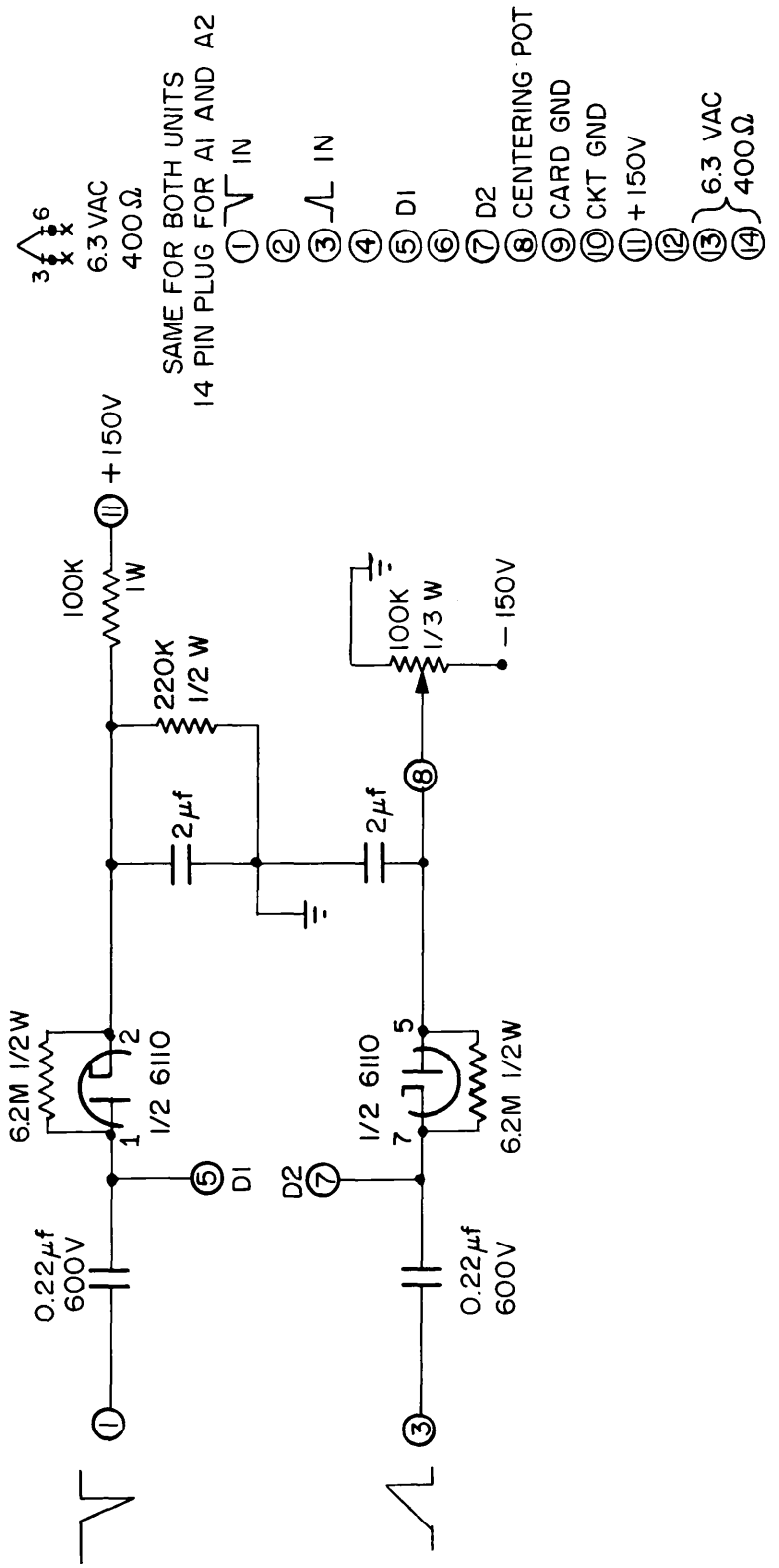


Fig. 7 - Units 7, 8, 10—A1 and A2 horizontal centering and B vertical centering

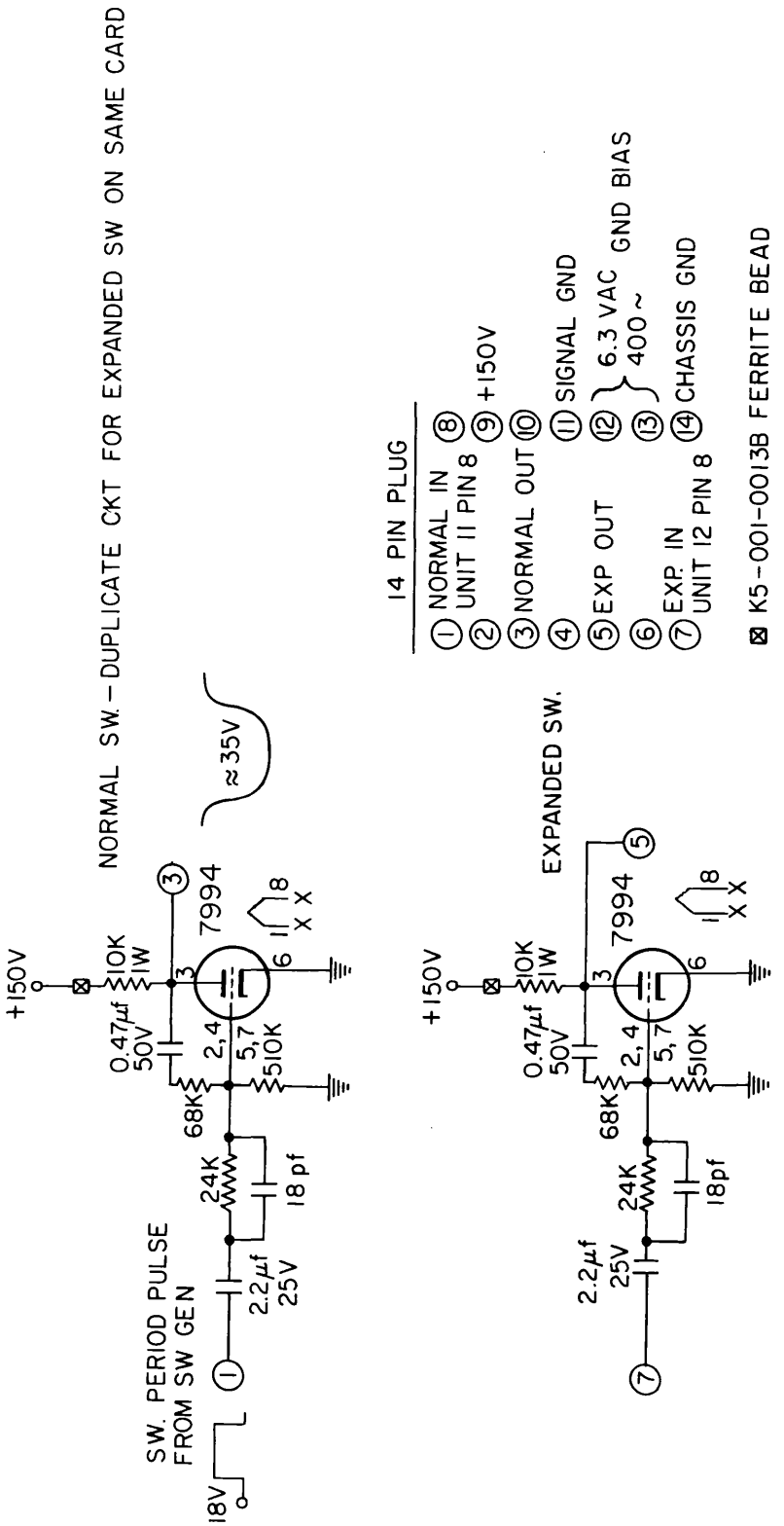


Fig. 8 - Unit 9—Dynamic focusing

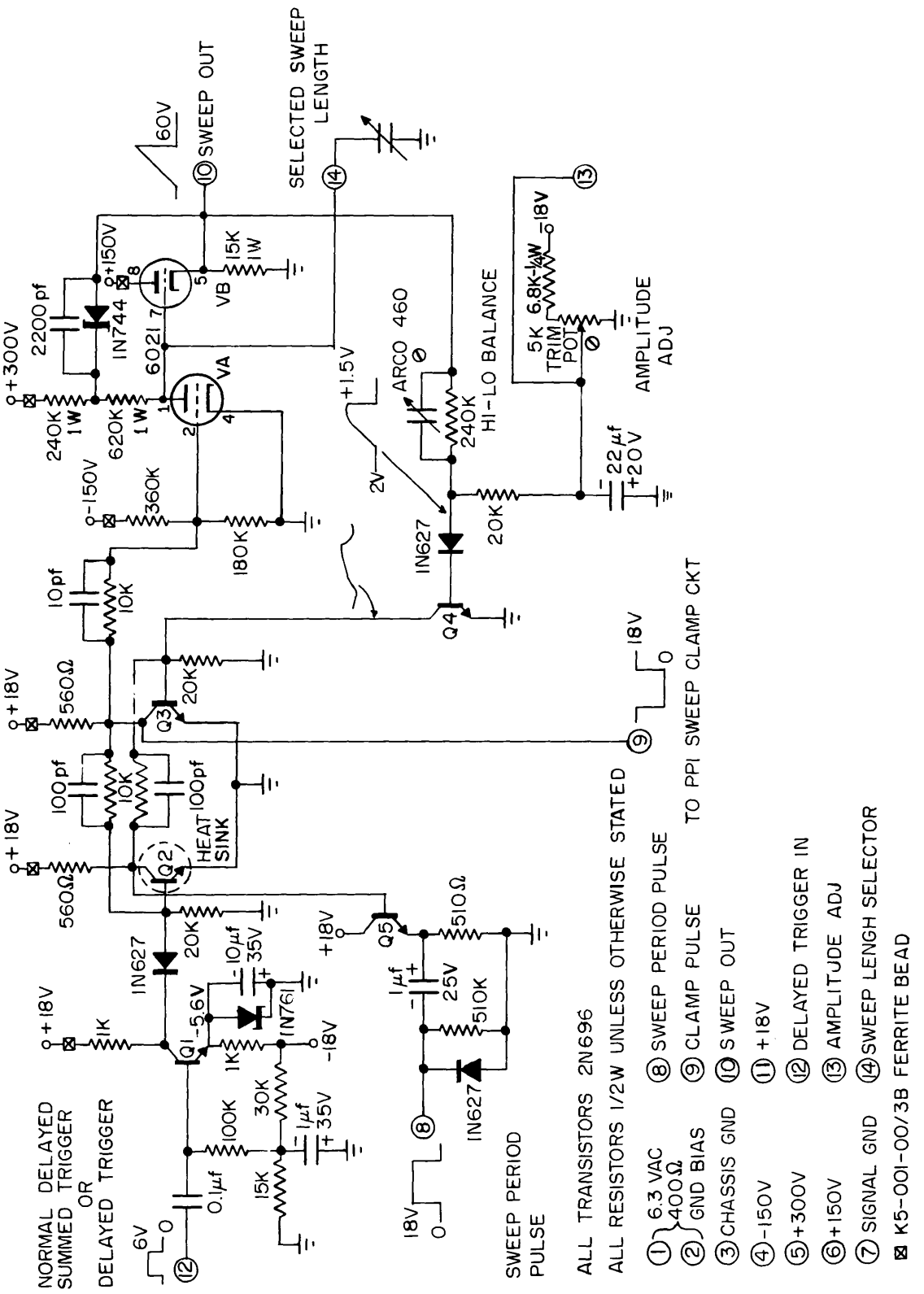


Fig. 9 - Units 11, 12—Sweep generator

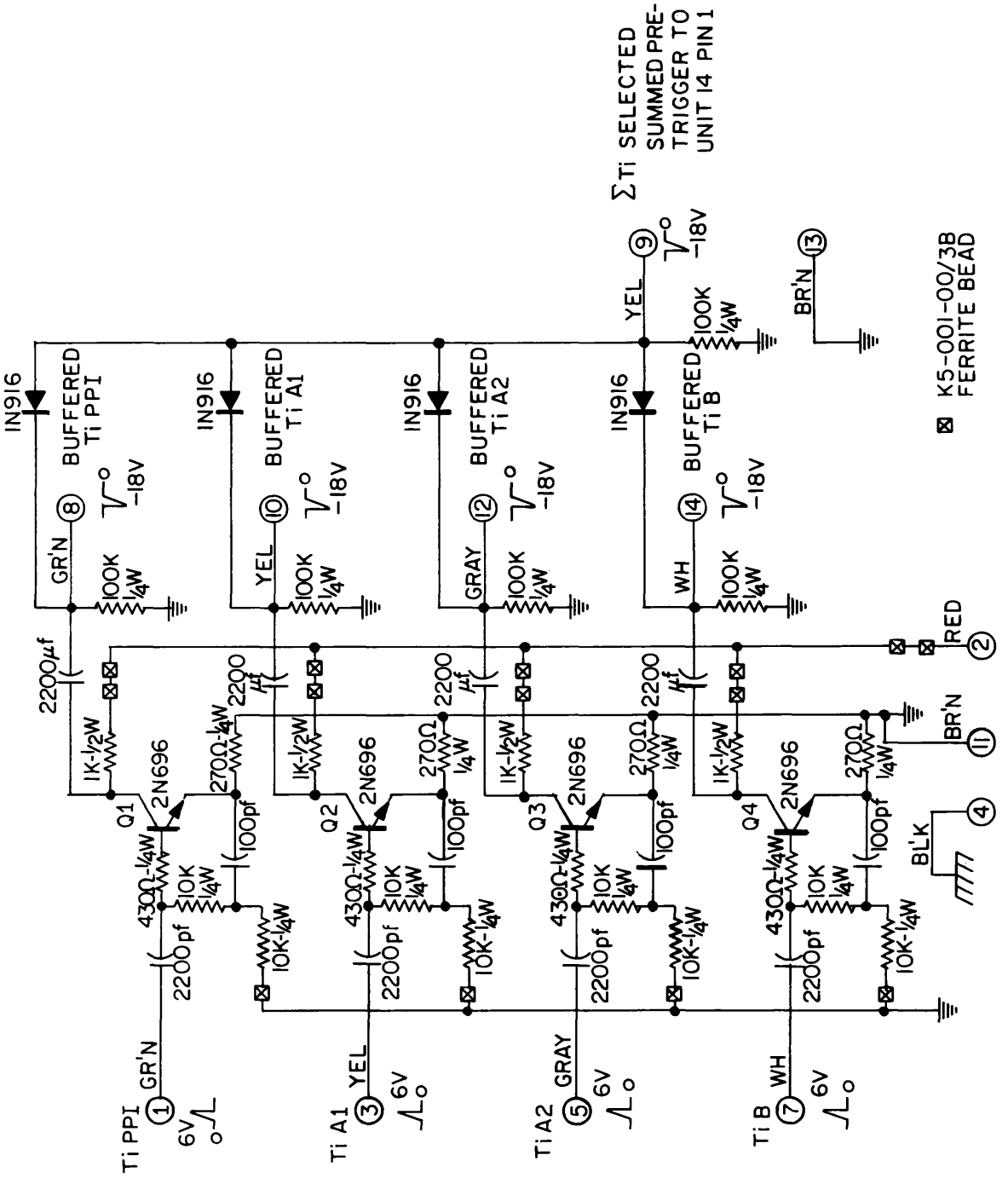


Fig. 10 - Unit 13 – Trigger buffer unit

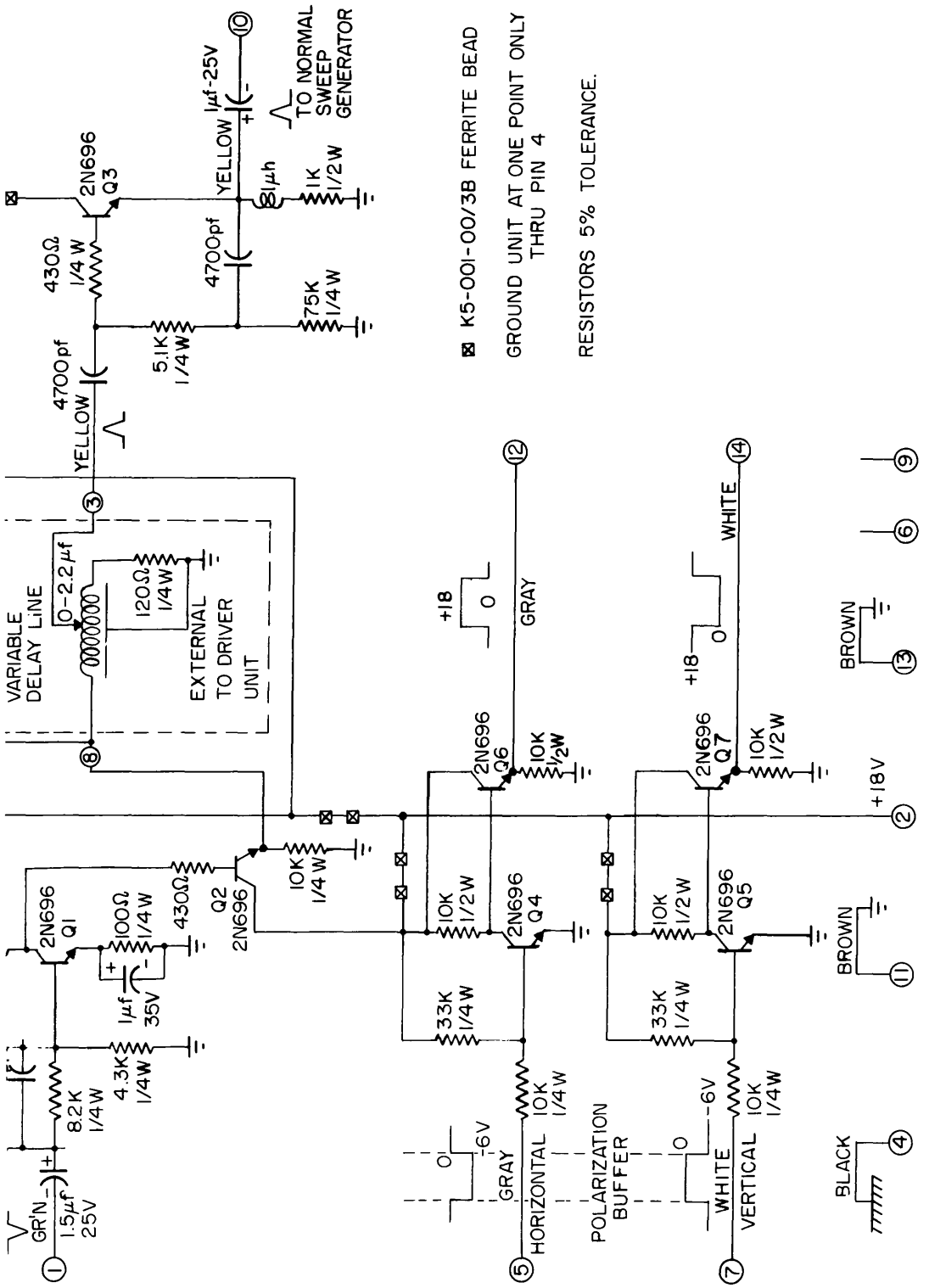


Fig. 11 - Unit 14—Trigger delay and polarization buffer

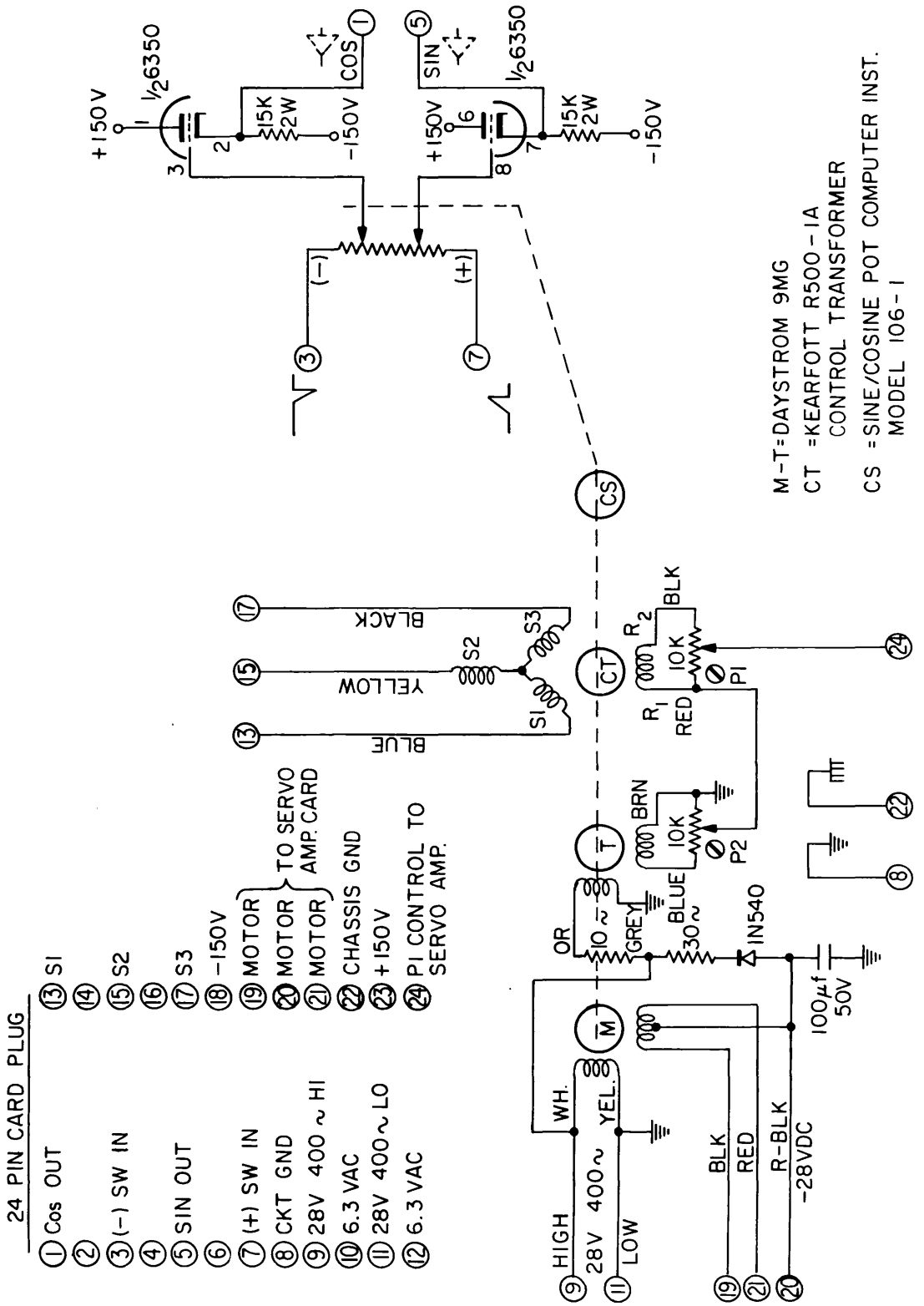


Fig. 12 - Unit 15—Servo-sine/cosine potentiometer

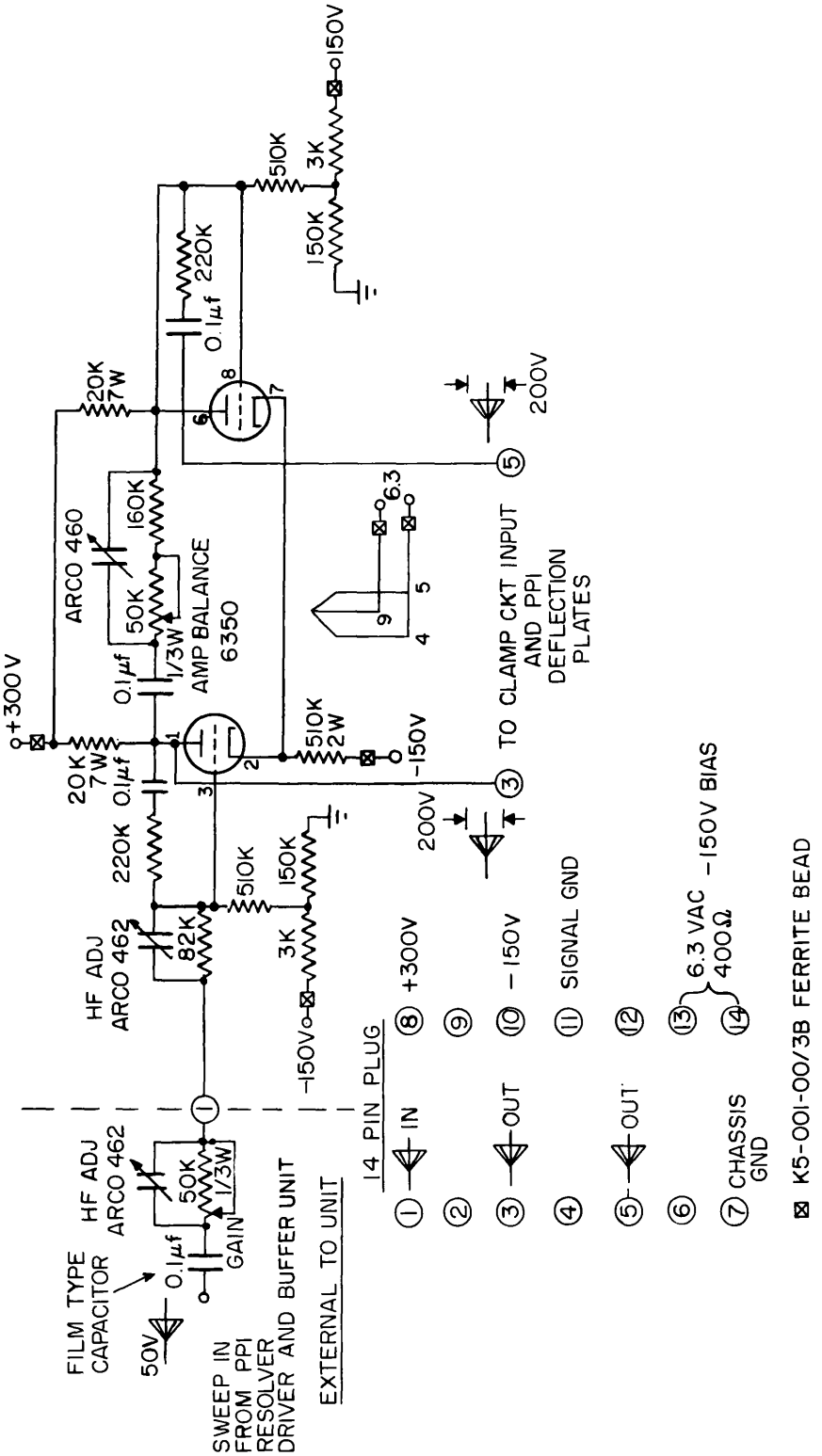


Fig. 13 - Units 16, 17—PPI horizontal and vertical deflection amplifiers

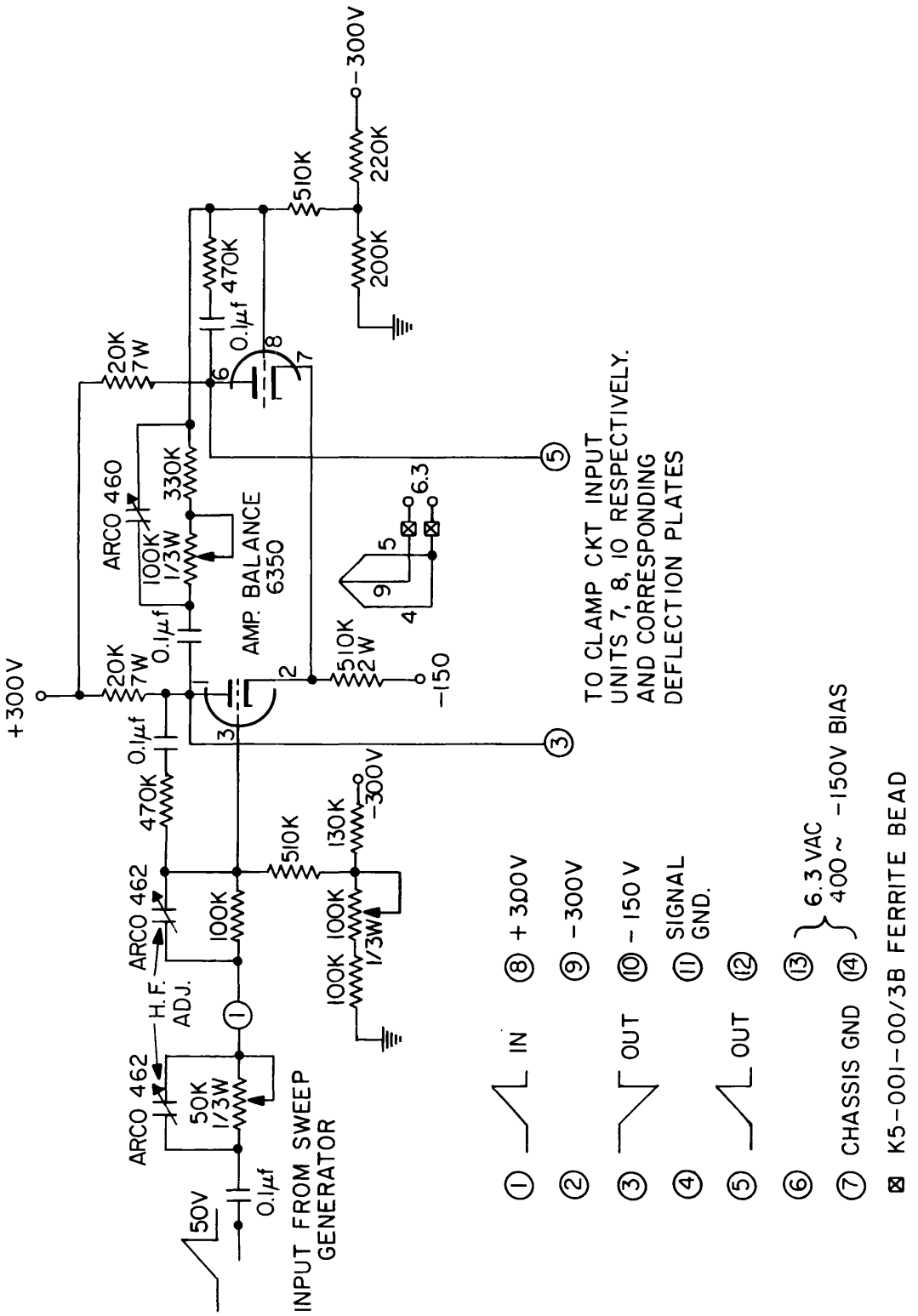


Fig. 14 - Units 18, 19, 21 – A1-A2 horizontal and B scan vertical deflection amplifier

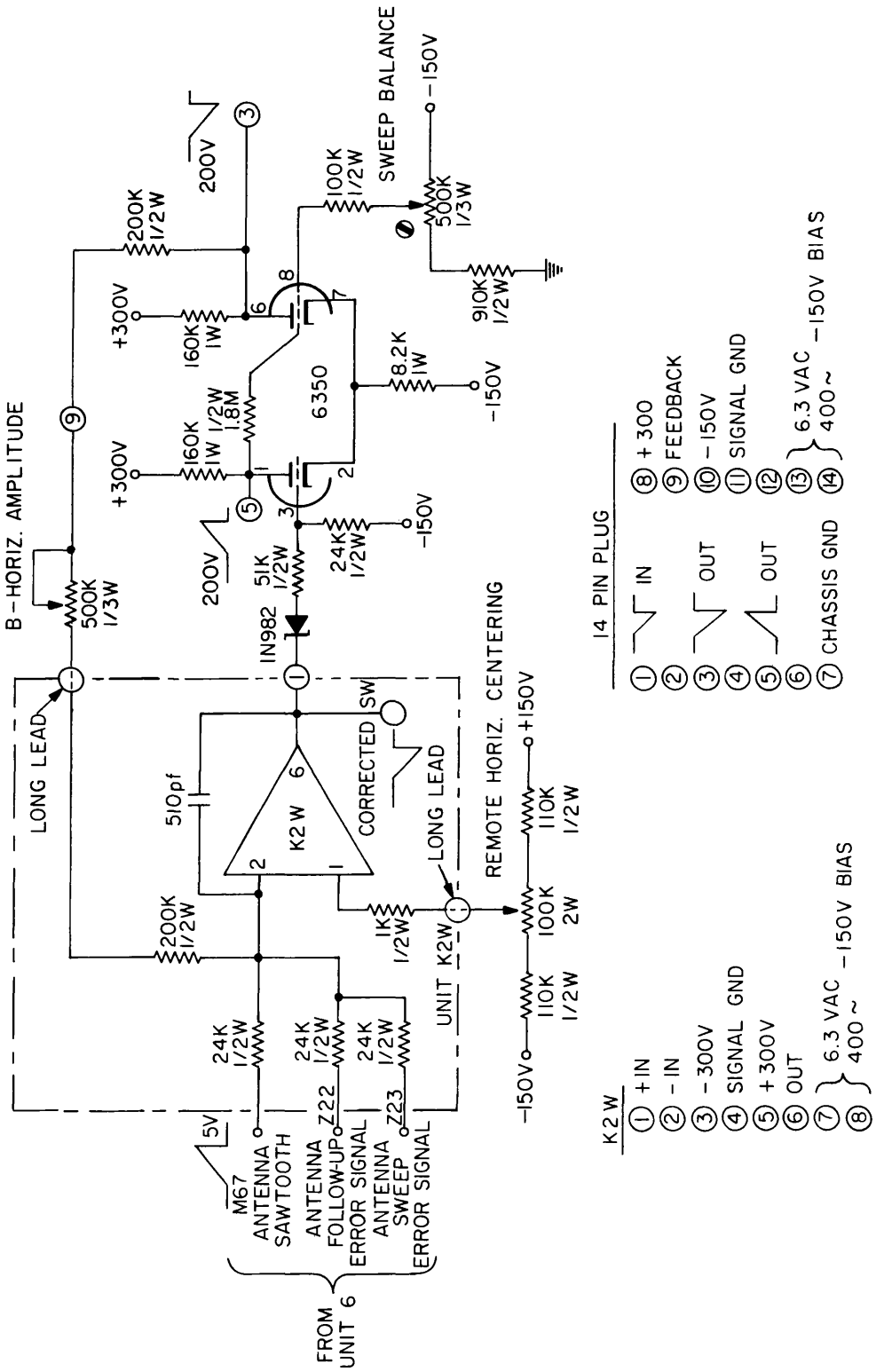


Fig. 15 - Units 20, K2W—B-scan horizontal deflection amplifier

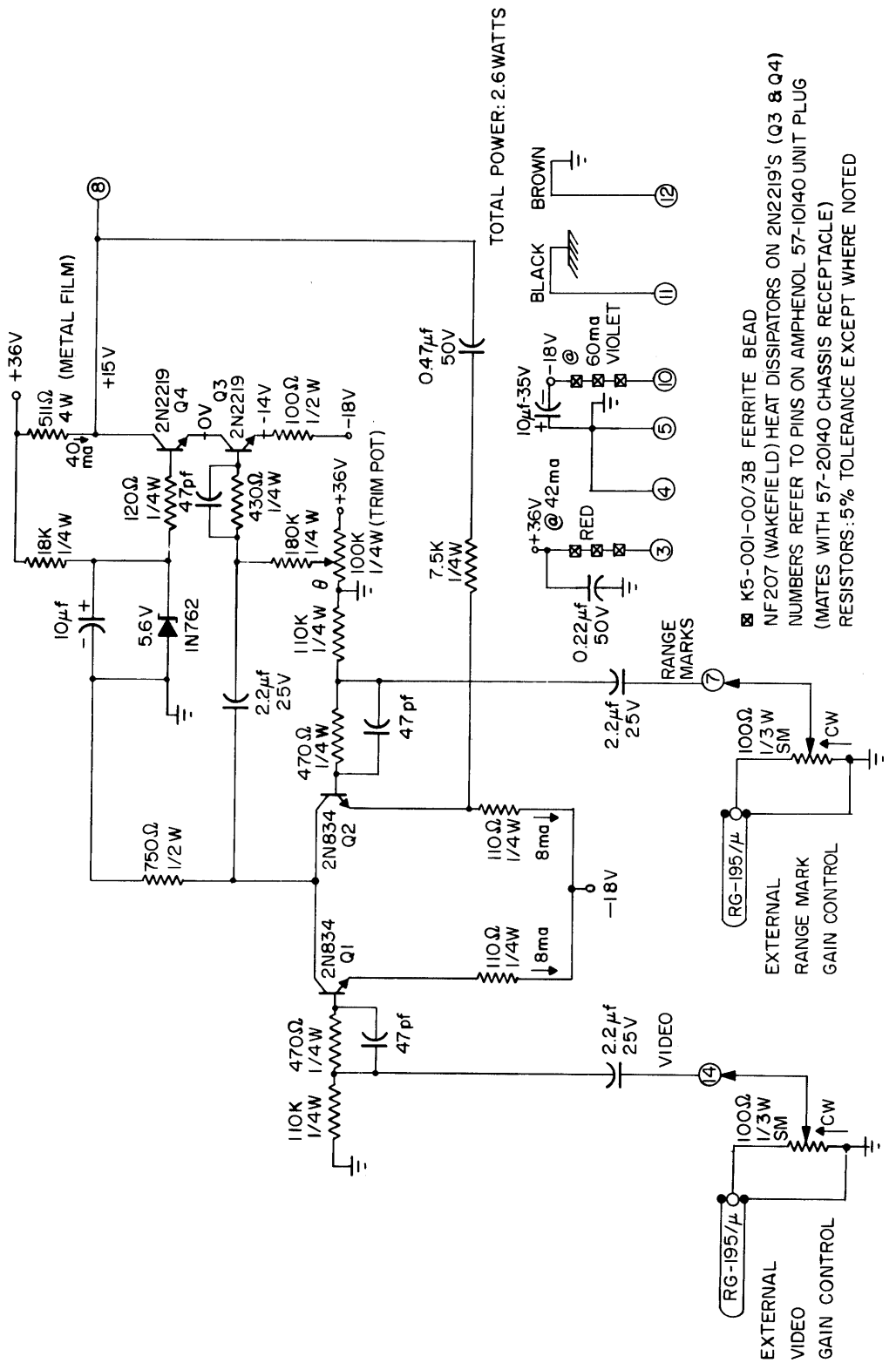


Fig. 16 - Units 22A, 25A–B and PPI video amplifier for bipolar input and output

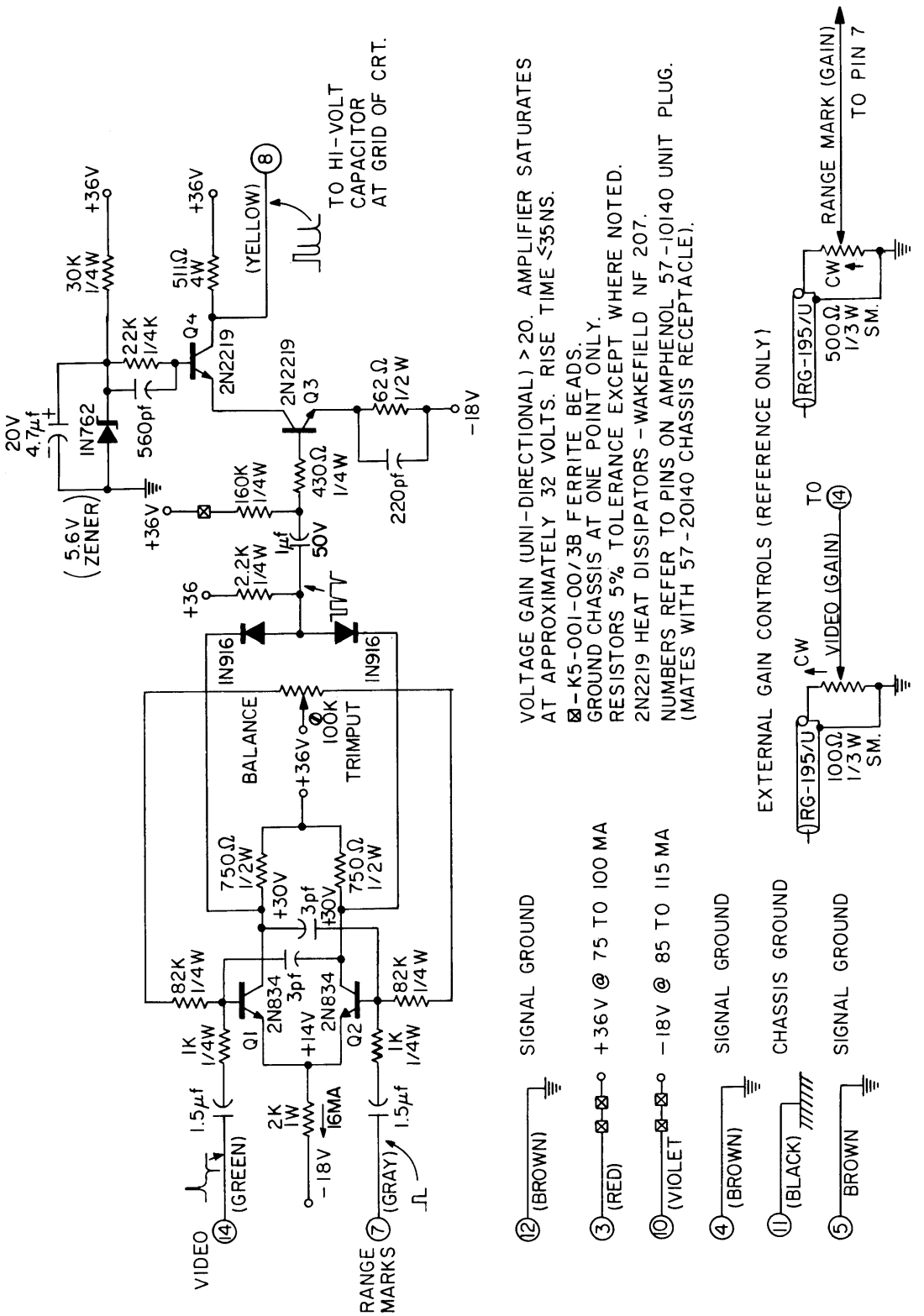


Fig. 17 - Units 22B, 25B–B and PPI video amplifier for bipolar input and unipolar output

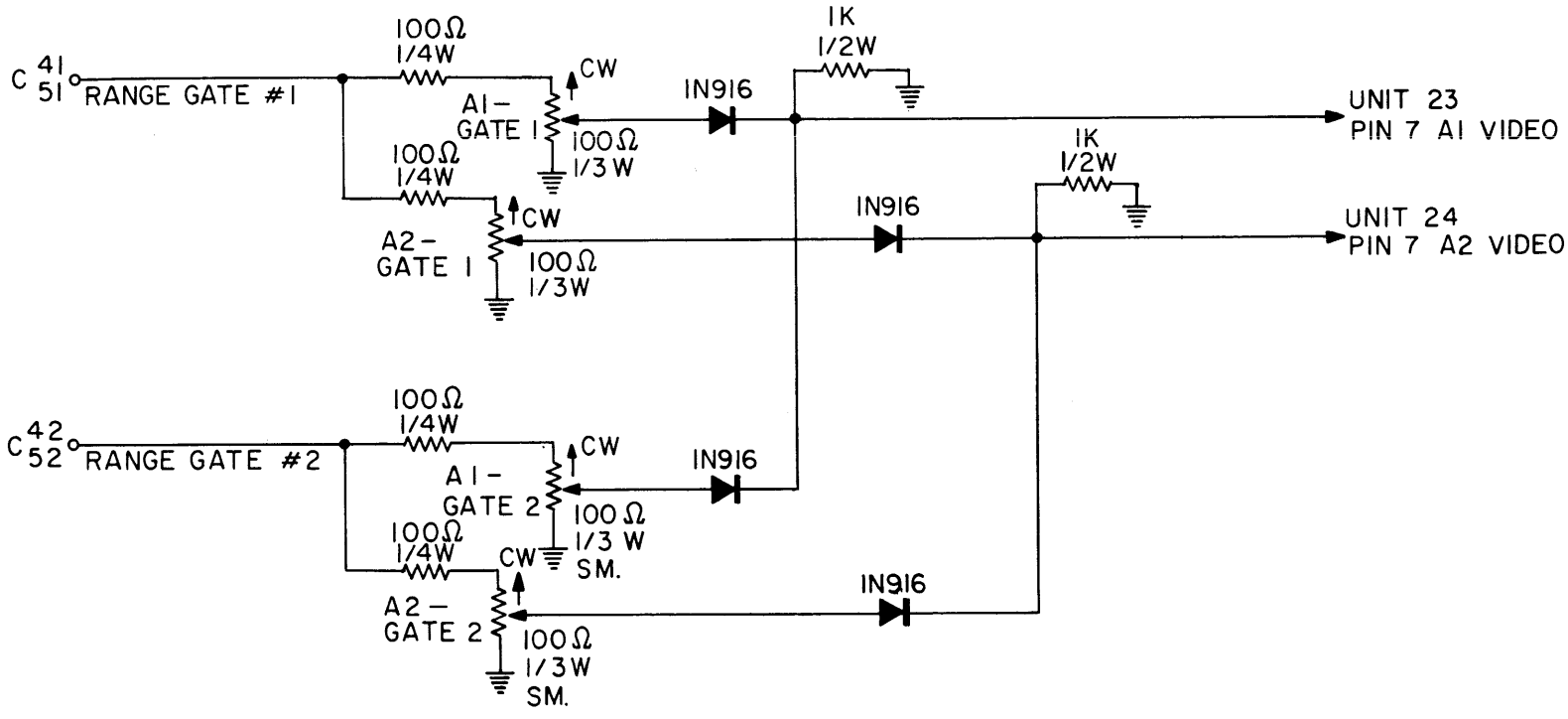


Fig. 18 - Range-gate mixing circuit

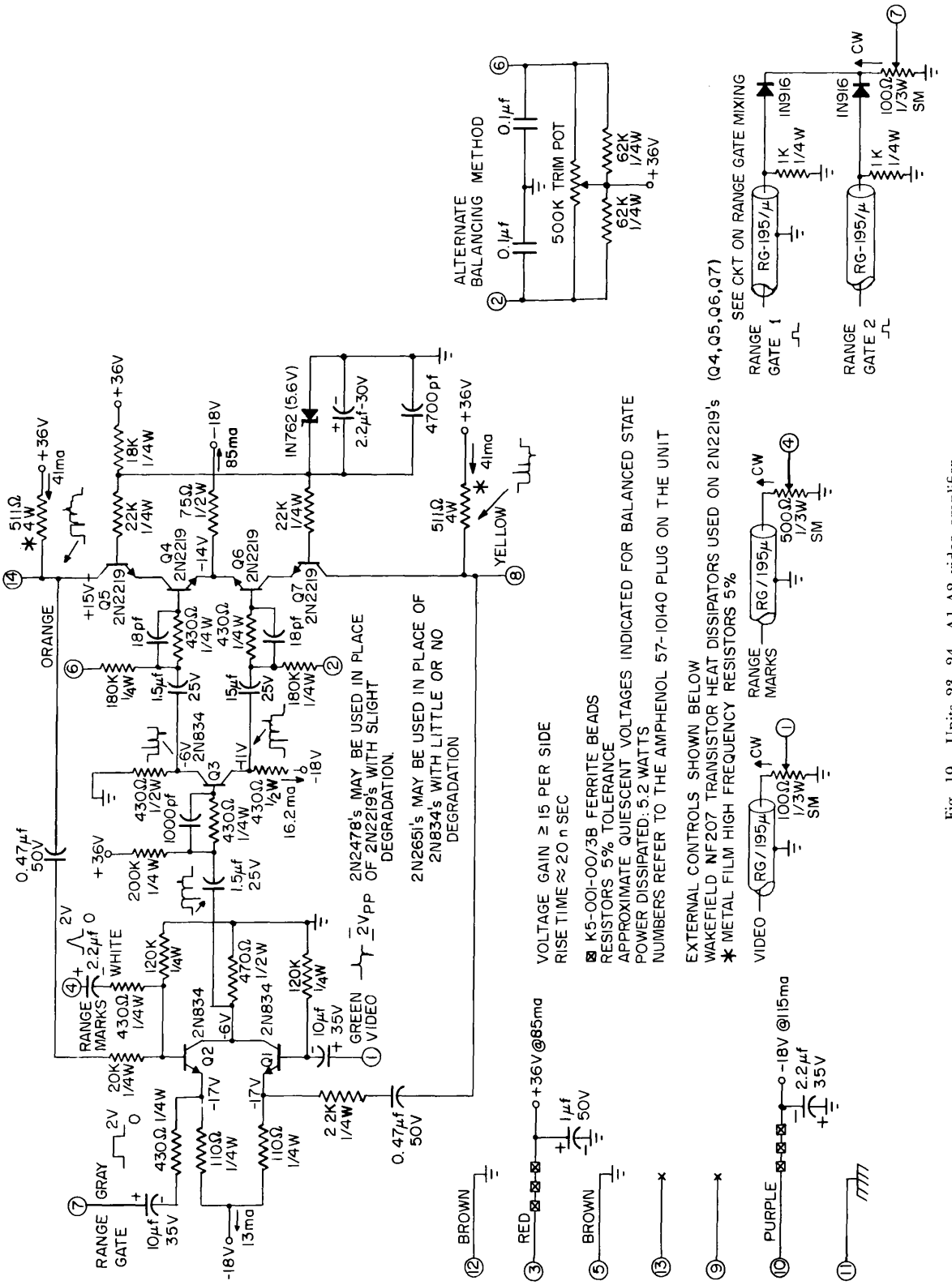


Fig. 19 - Units 23, 24 – A1-A2 video amplifier

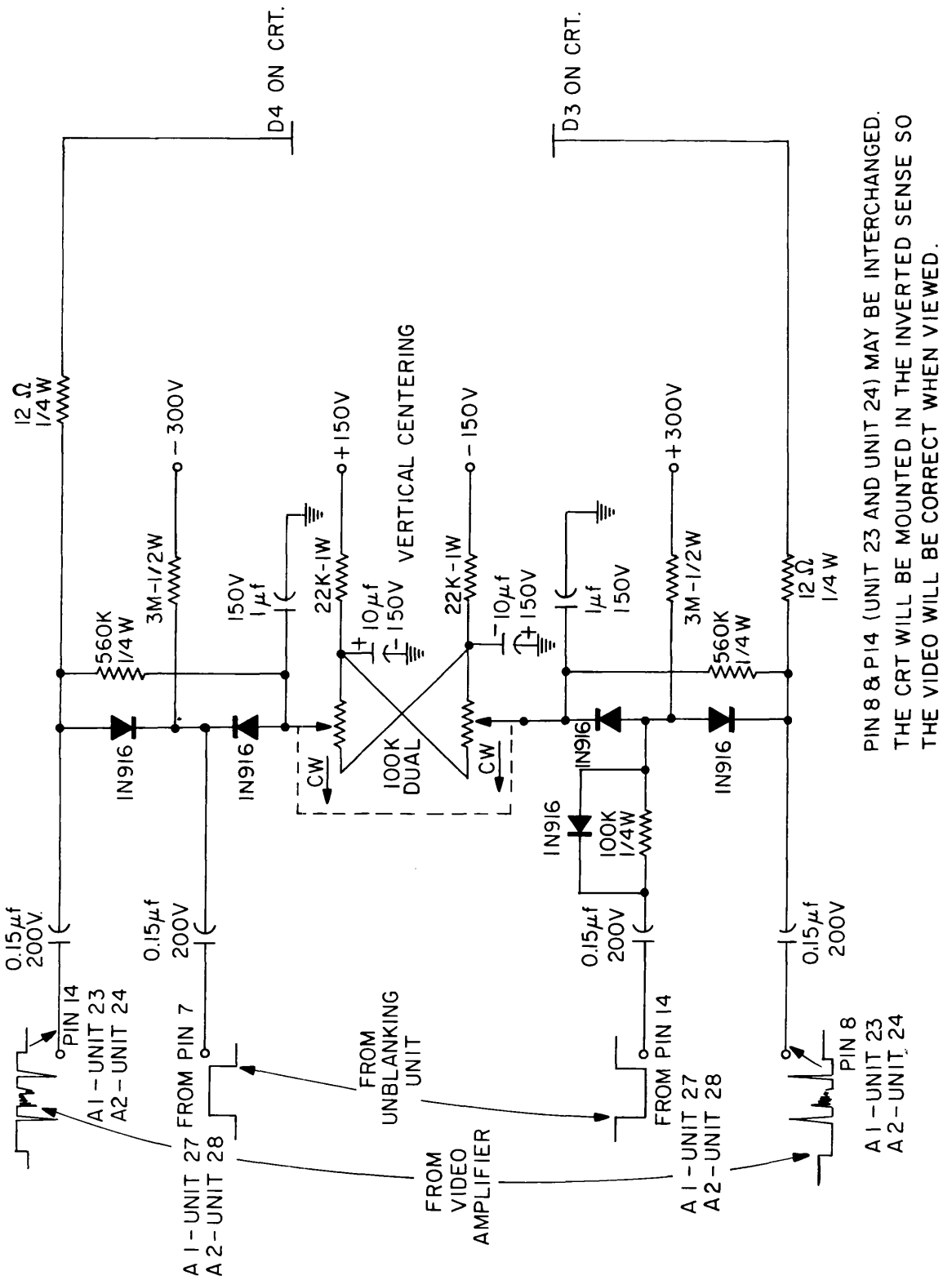


Fig. 20 - A1-A2 vertical centering, clamping and dc restoration

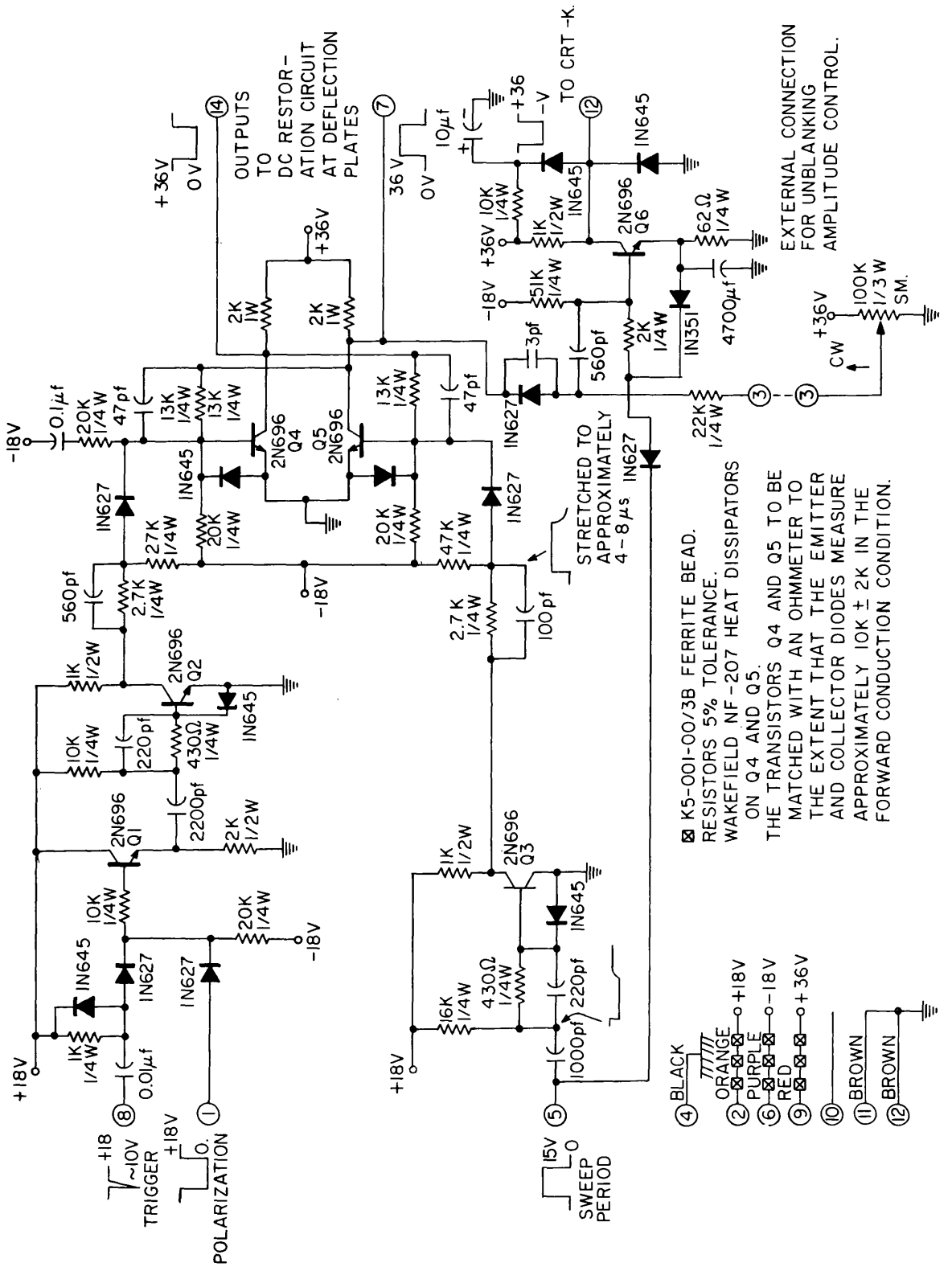


Fig. 21 - Units 26, 27, 28, 29—Unblanking circuit

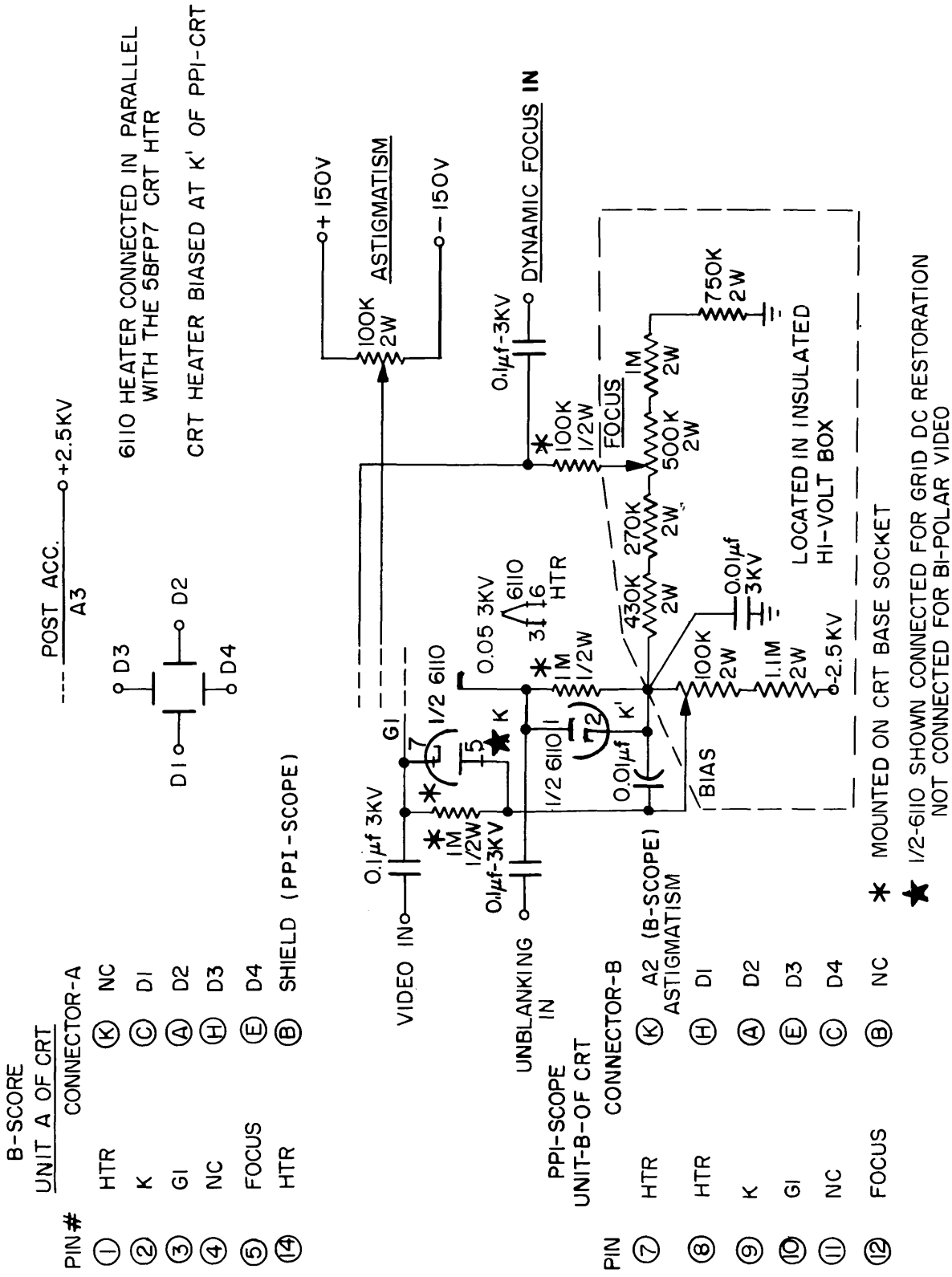
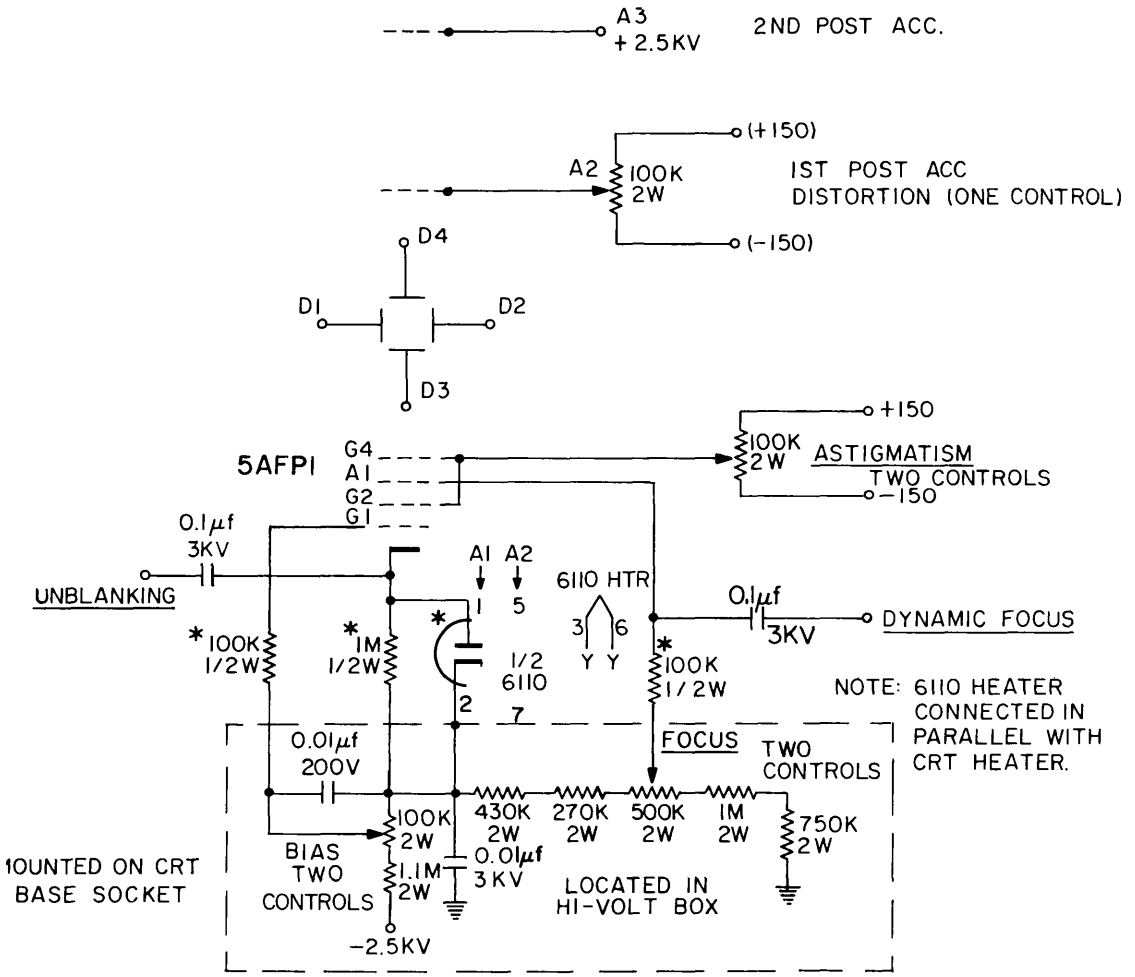


Fig. 22 - B and PPI crt circuit



A1 UNIT 1 SOCKET	A2 UNIT 2
① HTR	⑦ HTR
② K	⑧ HTR
③ G1	⑨ K
④ NC	⑩ G1
⑤ A1	⑪ NC
⑭ HTR	⑫ A1

	A1 UNIT 1 DEFLECTION RING	A2 UNIT 2
(ASTIG.) ACCELERATOR	① G2 TO G4	⑥ D1
	② D3	⑦ D2
	③ D4	⑧ G2 & G4
SHIELD ELECTRODE	④ A2 SHIELD	⑨ D4
	⑬ D2	⑩ D3
	⑭ D1	⑪ A2 SHIELD

HEATERS BIASED AT K' ON PPI-CRT

Fig. 23 - A1-A2 crt circuit

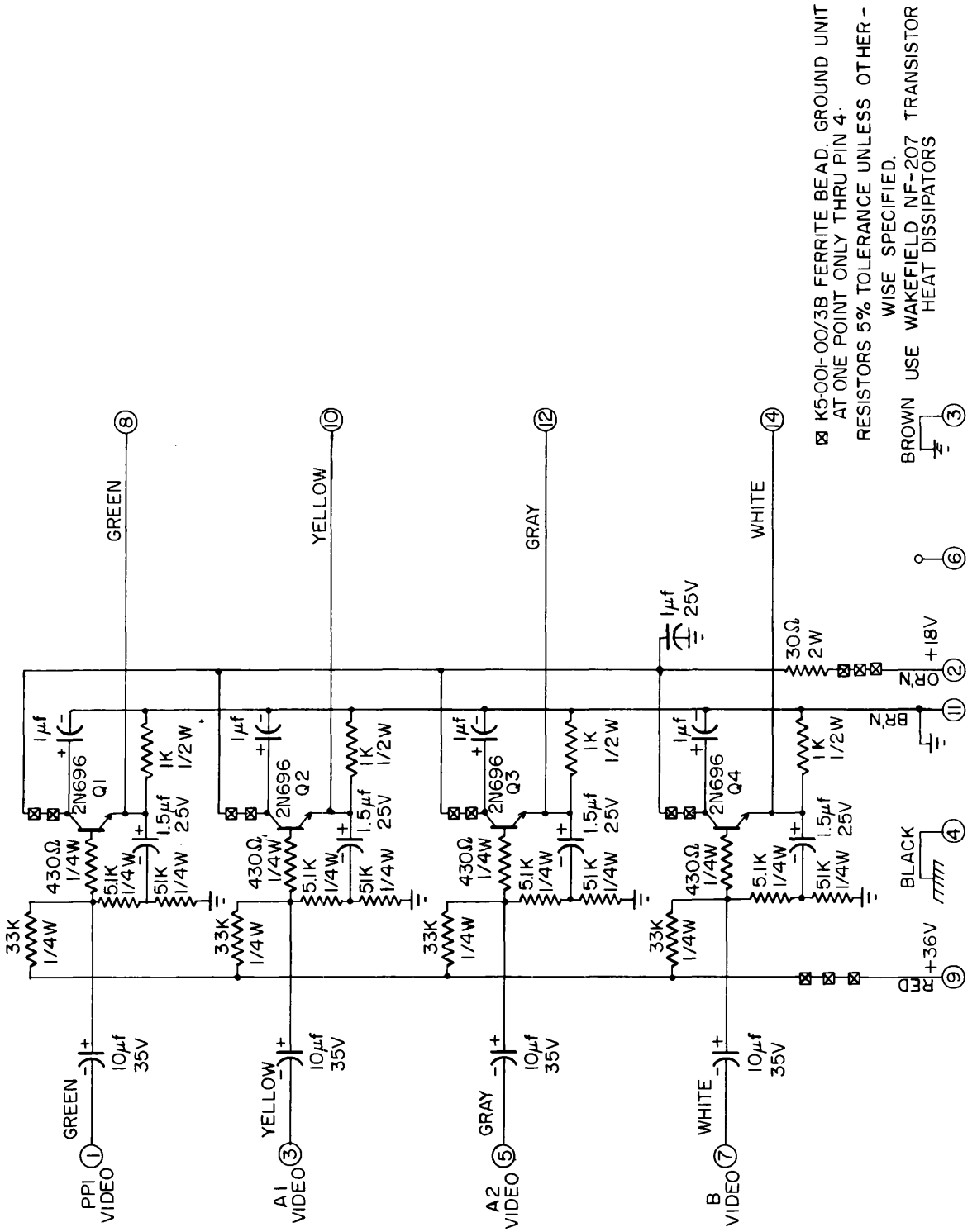


Fig. 24 - Unit 30 – Video buffer

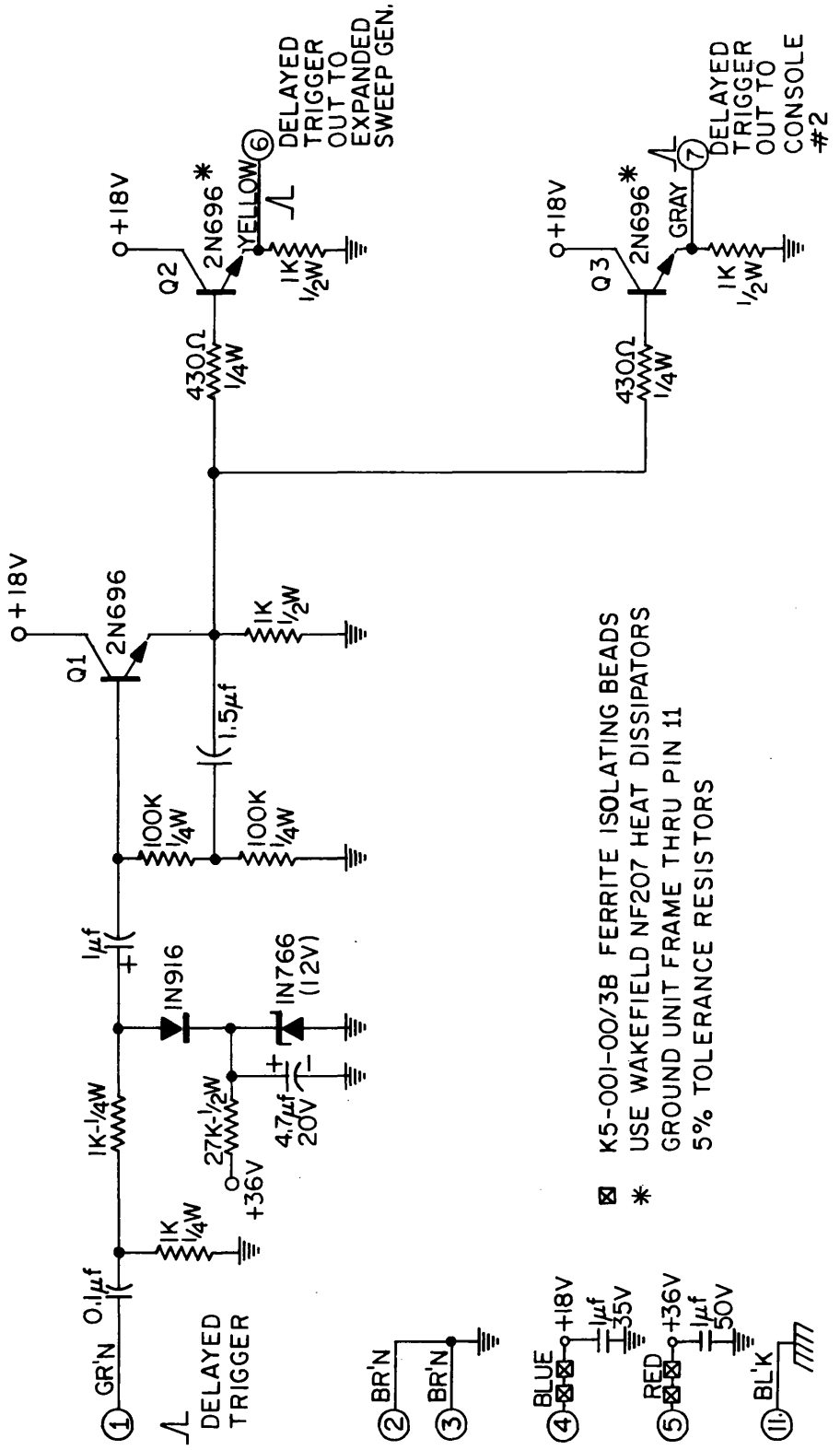


Fig. 25 - Unit 31 – Delayed trigger buffer

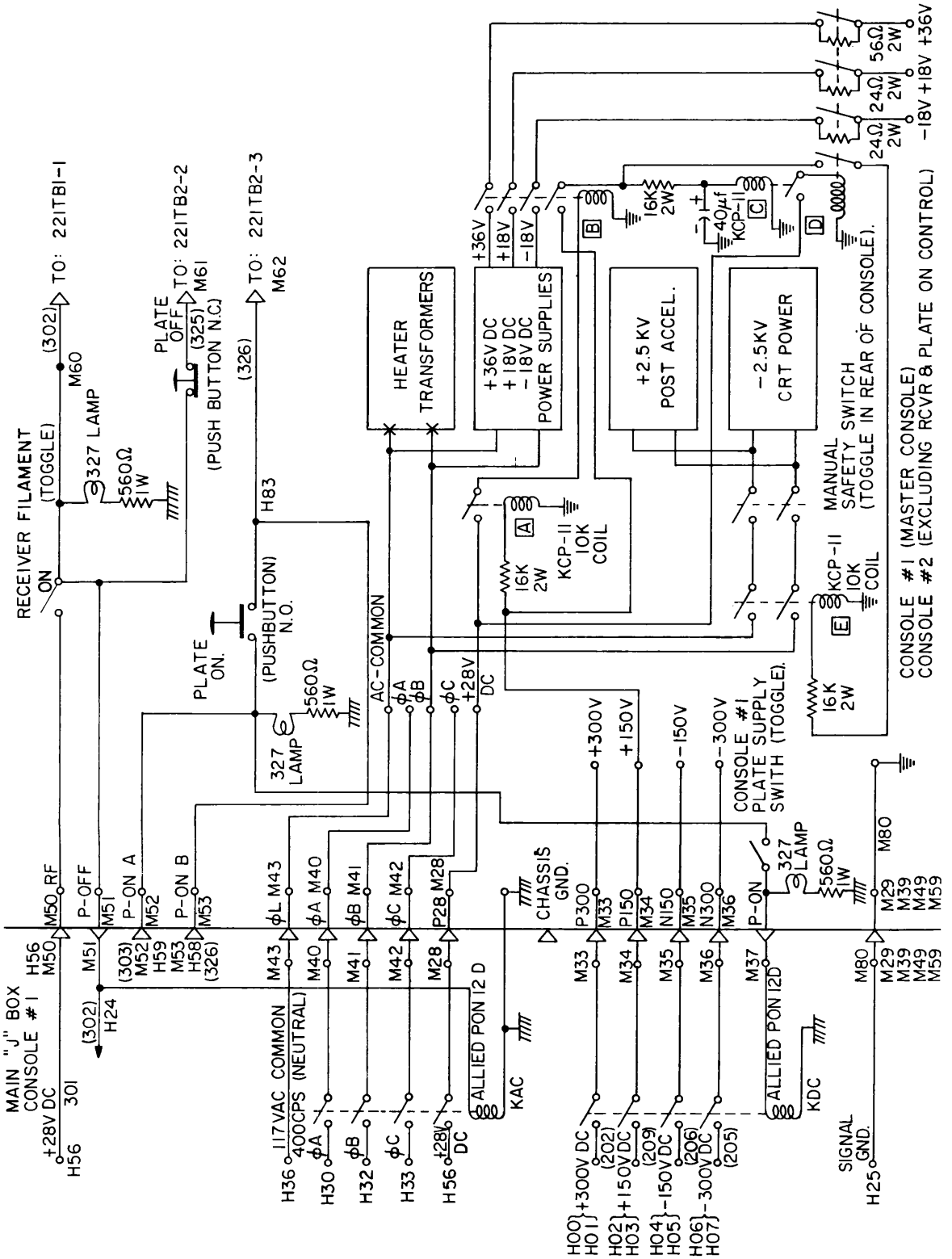


Fig. 26 - Console power-control switching

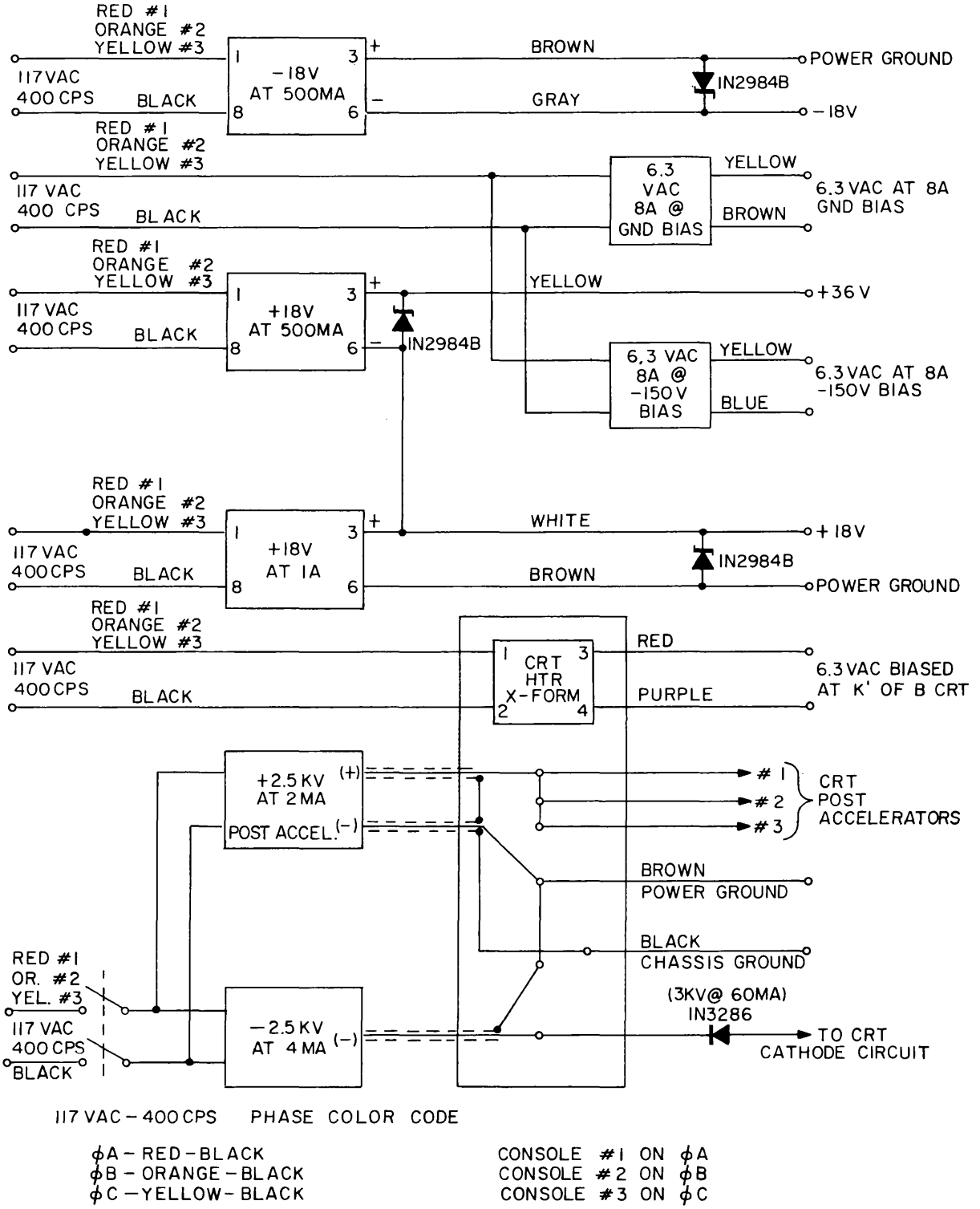


Fig. 27 - Power-supply circuit

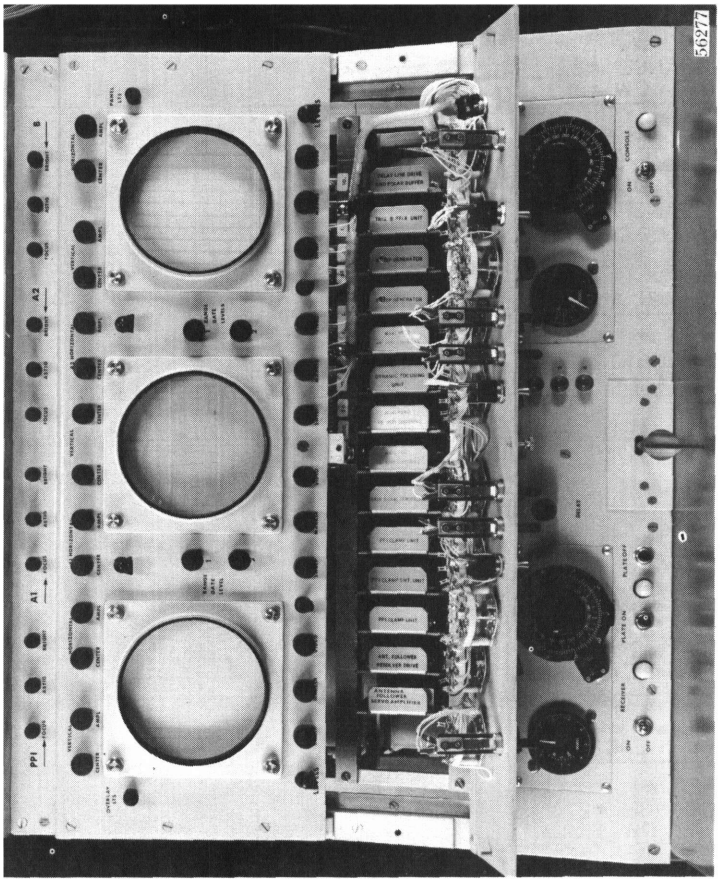


Fig. 29 - Front view of master console with front selector panel open

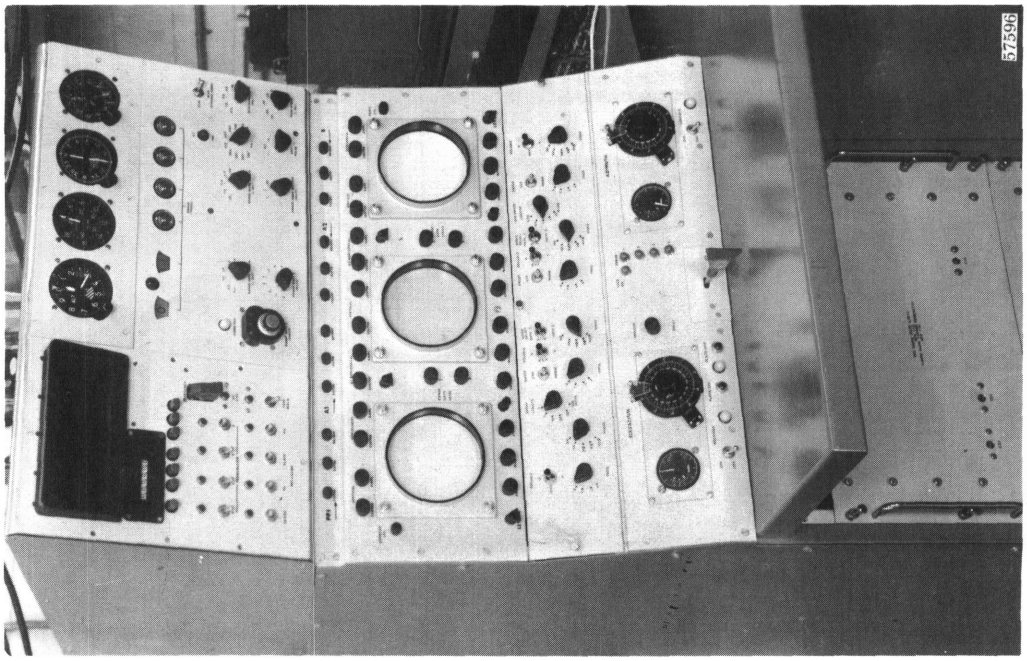


Fig. 28 - Front view of 4FR master console

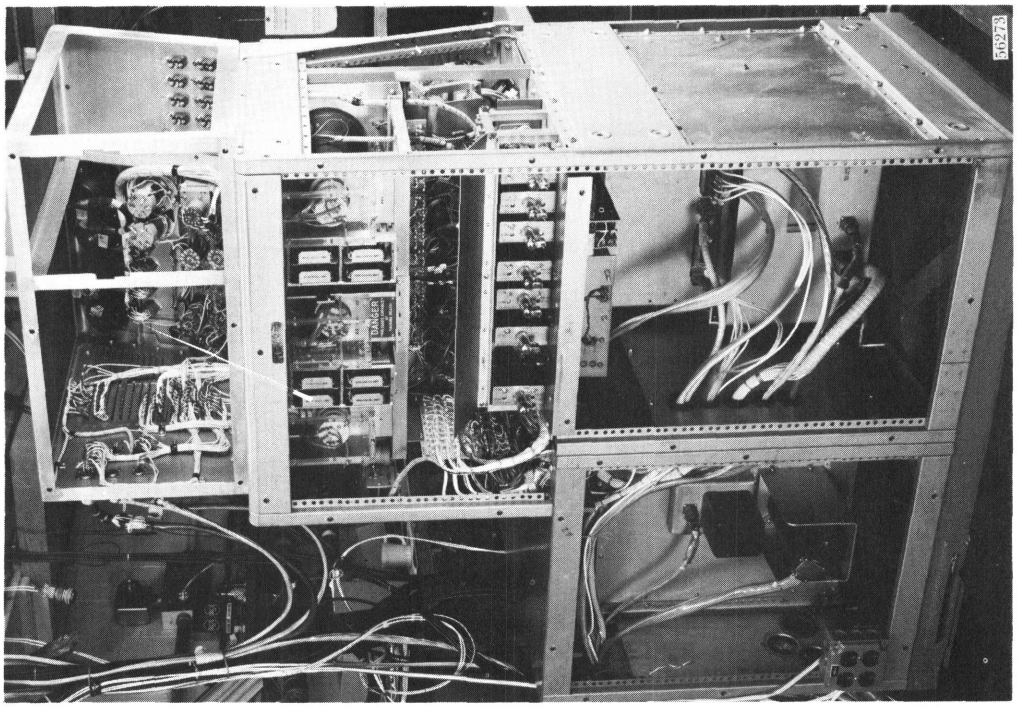


Fig. 31 - Overall rear view of master console

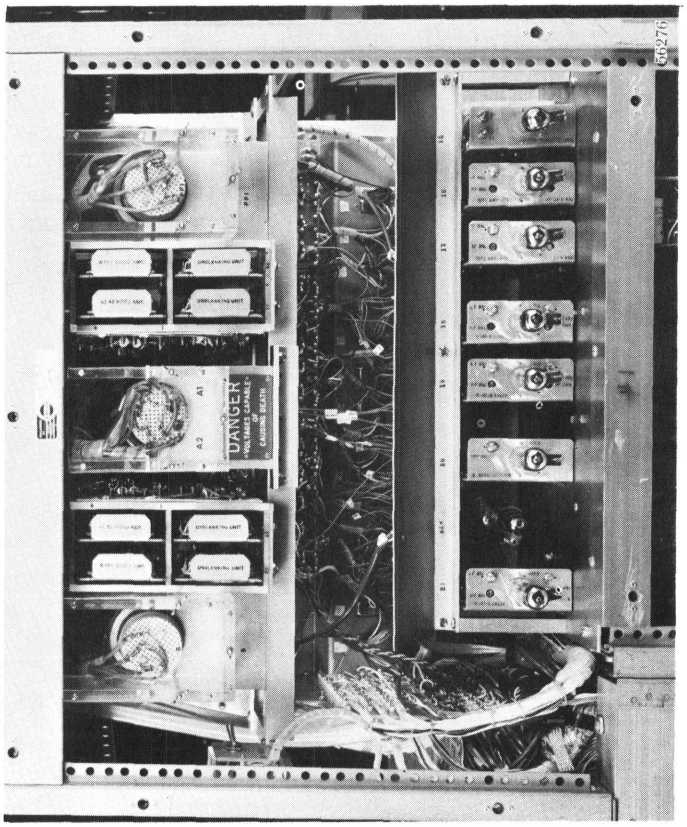


Fig. 30 - Rear view of master console

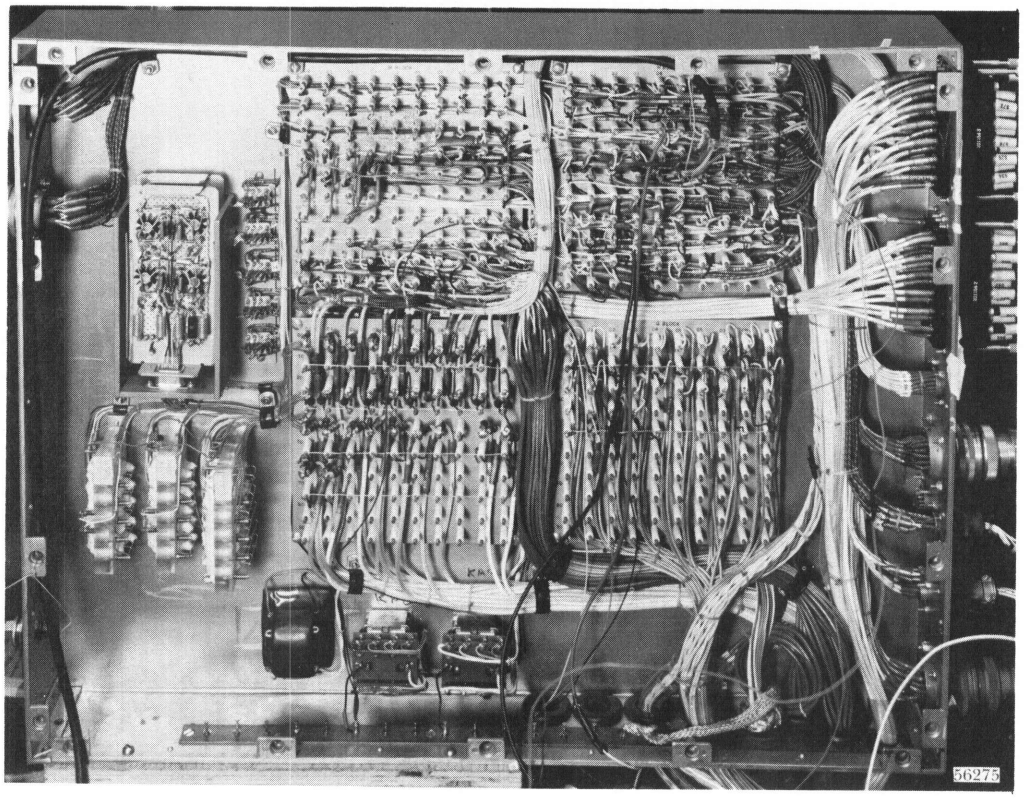


Fig. 32 - Front view of main junction box

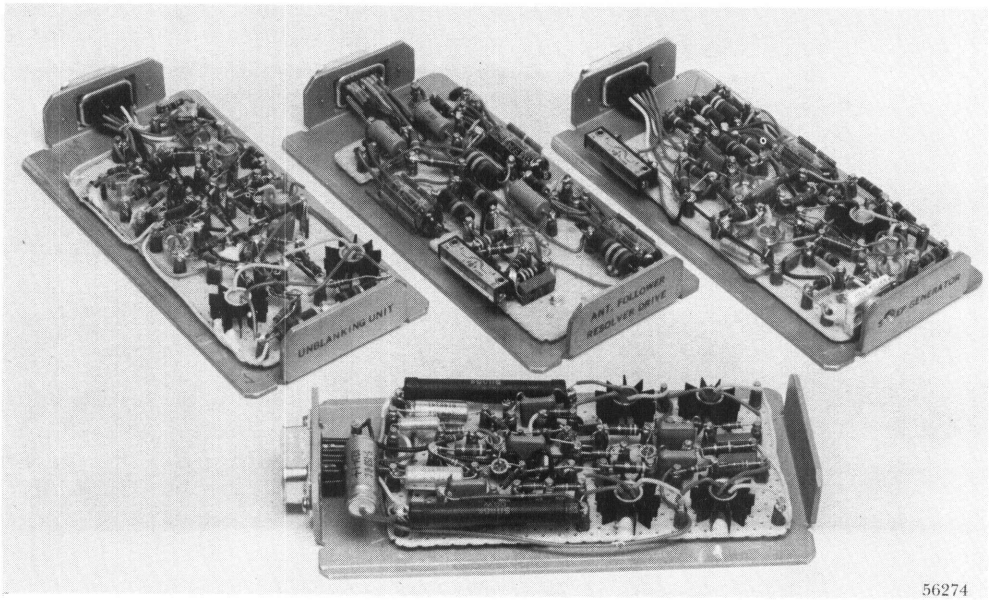


Fig. 33 - Representative modular units