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IFF Active Readout Control and Display System

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CONTENTS

ABSTRACT

An IFF active readout control and display system using majority logic and PPI position correlation techniques is being developed in the Data Processing Branch. Up to five target responses in each interrogated mode are stored, and majority-voting logic determines the confidence of the stored returns in each mode. So long as a gated target's interrogation responses are present during one scan, the numerical processing continually attempts to increase the confidence of the stored returns. The position correlation techniques point out the location of the responding target on the PPI. A true range and azimuth video gate technique, which can work with analog or digital PPI sweeps, has been devised. This video gate technique works in conjunction with the PPI retrace insertion method employed.

PROBLEM STATUS

This in an interim report; work on the problem is continuing.

AUTHORIZATION

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Project SF 001-10-01, Task 6106

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IFF ACTIVE READOUT CONTROL AND DISPLAY SYSTEM

INTRODUCTION

The IFF active readout system (Ref. 1), under development in the Data Processing Branch, takes a selected range and azimuth gated IFF target return, which has been decoded, and displays the numerical code on a readout display. Response confidence level, numerical display, PPI display, and position correlation are also performed in the active readout system. Procedures for selecting a target's coordinates and gating its decoded responses must be completed in order to control the information sent to the numerical display processor (NUDOR) section of the active readout. The NUDOR takes these IFF responses and stores them until sufficient numbers of returns in the responding modes are received. When a required minimum of agreeing responses are stored, the NUDOR converts the binary code to the octal code for turning on the proper lamps at the numerical readout. This would be binary-to-decimal conversion in the case of the mode C altitude responses. The NUDOR also determines the confidence level of the IFF returns in each mode, the resulting level being indicated by a background color illumination of the numerical readout. For example: a red background illumination appears for a level of three out of five, a yellow background illumination appears for a level of four out of five, and a green background illumination appears for a level of five out of five agreeing returns. The minimum confidence is determined by three agreeing responses out of five. The NUDOR also stores the coordinates at which the minimum confidence requirement has been met and then makes these coordinates available for display on the PPI, thus pointing out the target whose numerical response is being displayed.

ACTIVE READOUT

An IFF active readout control and display system for use with standard Navy PPI radar repeaters and IFF equipment is illustrated in Fig. 1. Because maximum use of radar/IFF signals with minimum interference on the PPI display is desired, retrace insertion techniques are used to present the hook gating markers. The hook control is shown implemented by a light pencil to permit rapid and easy control of the active readout system. "Bowling ball" or "joystick" hook marker control may also be implemented.

As shown in Fig. 1, the active readout control and display system is operated in conjunction with a standard PPI repeater. The functions, shown in separate blocks, would be packaged together. Gating, trigger, and sweep signals are taken from the PPI repeater in order to provide the timing and coordinate position value to the retrace-insertion unit and the correlation feedback stores. During the retrace period of the PPI, the retrace-insertion unit causes a marker to be displayed at the hook gate position. The hook position is controlled by the light pencil. When the operator positions the hook gate over a target whose IFF code is wanted, the parallel decoded signals from the IFF decoder are gated through to the numerical display processor (NUDOR). This occurs when the antenna sweeps through the gated area. The NUDOR stores all of the decoded modes received and, when the minimum confidence level is obtained, causes the follow and hold circuits to store the corresponding coordinates. These stored coordinate positions are available for display on the PPI. The decoded IFF signals are available for display on the numerical readout with a corresponding color indication of the confidence level. IFF systems being implemented will make use of mode interlace in the process of interrogation. The use of mode interlace requires the NUDOR to separate the returns by mode and store them. The first three modes of the IFF are stored and called up by the operator on demand for display on the upper row of the two lines comprising the numerical display. The mode 5 response is displayed, whenever present, on the second line of the numerical readout as shown in Fig. 2. The second line of numbers on the numerical readout is provided for mode 5 because altitude is one of the quantities that is most likely to be monitored and because the manual switching between the two types of decoders (binary-to-octal and binary-to-decimal) would be complex and expensive for a single line readout.

As shown in Fig. 2, provisions are made for indicating the modes being interrogated on the upper half of the push-button mode selector switches. The selected mode being displayed is indicated on the lower half of the illuminated switch. Provisions are also made for displaying the mode 4 responses and the emergency alarm signals.

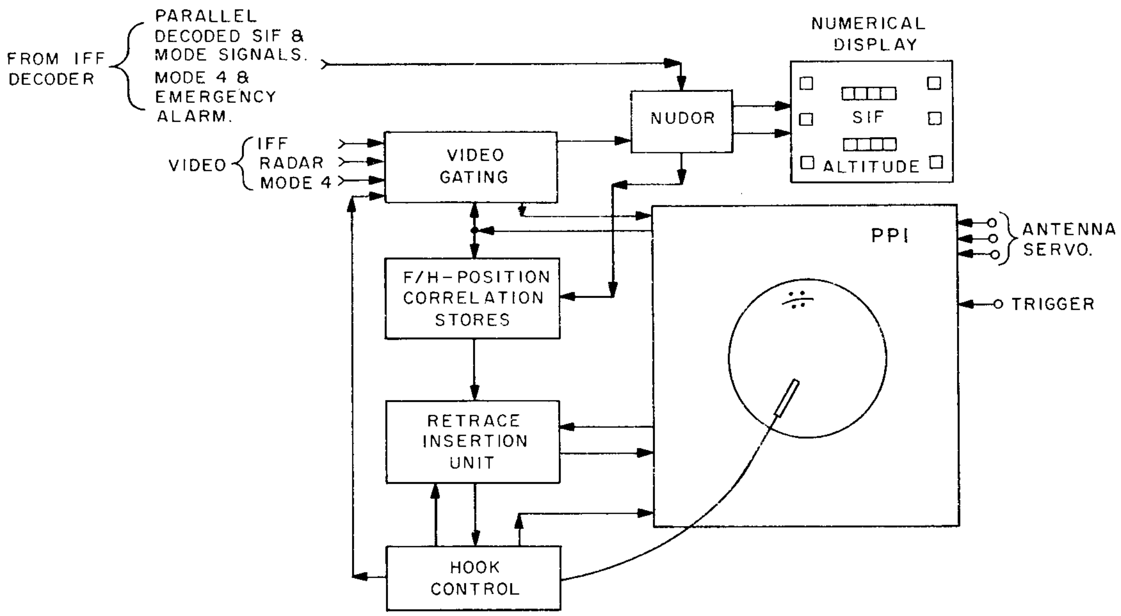


Fig. 1 - IFF active readout control and display

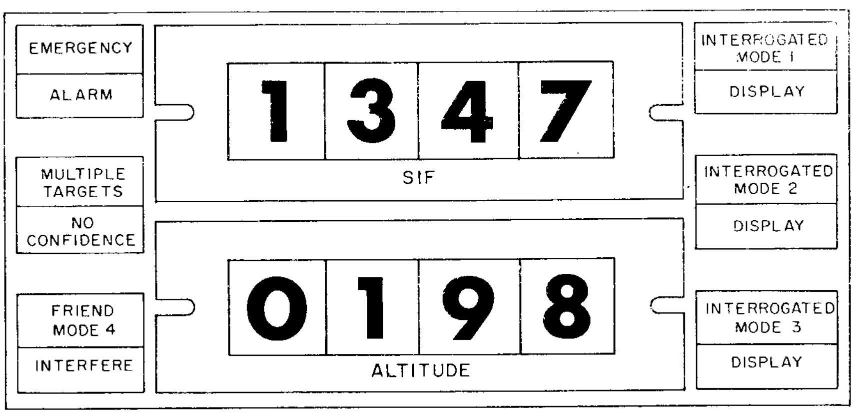


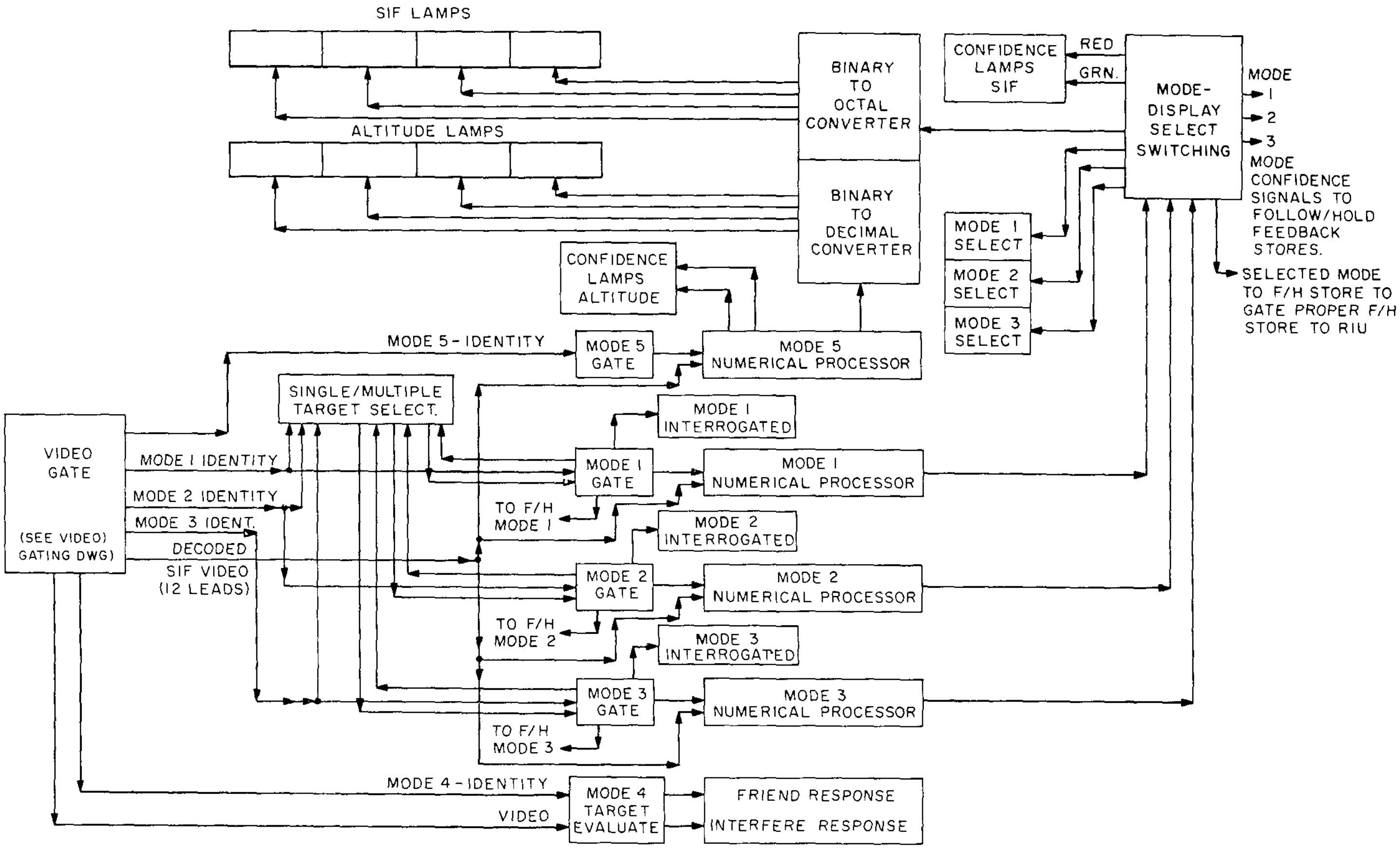
Fig. 2 - Numerical display processor front panel

As described to this point, the active display readout operates on all modes of the IFF returns emanating from a single target within the PPI gate. Because of the storage, switching, and correlation problems related to multiple target returns in the same gate, the complete processing of the multiple target data would be too cumbersome and costly if done with the same confidence as is done with single target returns. Since a warning indication of multiple target returns within the gate is desired, the operation of the NUDOR could be changed to store multiple targets in sequence as received from the IFF decoder. Means would then be provided for the operator to manually select the stores for the decoded IFF returns and display them in succession on the numerical readout. In this type of operation, no confidence evaluation or correlation indication would be performed and interrogation would be restricted to a single mode. Supermoding with mode 4 would not be affected by this decision, however, nor would this decision affect any other operations described here.

The confidence evaluation, based on the all-mode single-target case, requires at least three agreeing decoded responses out of a total of five responses stored. In the system shown, provisions are made to use a two out of three minimum confidence evaluation in order to reduce the complexity of the NUDOR. In many operational environments, the two out of three confidence evaluation may prove to be adequate. Two out of three logic is planned for the developmental model, but the NUDOR design could be expanded to the three out of five logic if operational experience indicates a need for the addition. Three out of five evaluation logic is shown, but the changes required to obtain the simpler two out of three logic are indicated. The method of retrace insertion is given in Ref. 2 and the method of the hook gate control is given in Ref. 3.

NUDOR OPERATION

The numerical display processor (NUDOR) section of the active display readout system is illustrated in block diagram form in Fig. 3. The mode identity signal from the decoder, which occurs at the time of the interrogation, activates the proper mode gate. For single target responses on all modes, the IFF video is gated through the video gate from the IFF decoder in parallel form. The video gate is opened at the proper time to pass the responses of the target appearing within the hook gate on the PPI. The decoded video is then stored in the numerical processor associated with the activated mode gate. The mode gate also activates the proper mode-interrogated lamp. At the end of the mode interrogation period, the mode gate is closed. If mode interrogation is being interlaced, the NUDOR will automatically gate the video to the corresponding numerical processor. For example: if there are four consecutive triggers in mode 1 and if the decoder puts out four returns from the gated target, then these four returns would be stored in sequence in the mode 1 numerical processor. If the next interrogation is in mode 2 for four triggers, then the four returns, if present, would be stored in the mode 2 numerical processor. Then, if the next set of interrogations is again mode 1, the returns, if present, would be gated through to the mode 1 numerical processor. The first return of this second group of four returns would be stored in the fifth position of the mode 1 numerical processor (using 3/5 minimum confidence). If all of the stored codes in the mode 1 numerical processor are the same, the remaining decoded returns are ignored. If at least three of the five SIF codes stored are in agreement, the remaining returns are placed sequentially into the disagreeing stores until agreement is obtained or until the returns cease. If after all the stores in the mode 1 numerical processor are filled and no 3/5 minimum confidence is obtained, the processor recycles to the store containing the oldest information and inserts the latest returns. If at any time during this process the three out of five confidence is reached, the numerical processor immediately routes the latest incoming returns to the disagreeing stores. The gating, storing, and evaluating continues in the NUDOR on all of the modes being received from the target in the hook gate. In the case of mode 5, the output of the numerical processor drives the binary-to-decimal converter which energizes



NOTE: FOR MULTIPLE TARGET ONE MODE (1,2 OR 3) IN ONE GATE, SWITCH ALL MODE IDENTITY LEADS TO THE ONE MODE DESIRED. MODE 5 WOULD CONTINUE TO BE ON FIRST TARGET. MODE SELECT SWITCHES WOULD THEN INDICATE TARGETS 1, 2 & 3

Fig. 3 - Numerical display processor (NUDOR)

the necessary lamps to indicate the target altitude. Simultaneously, the numerical processor causes the readout to be illuminated with the color indicating the confidence level of the stored altitude.

In the case of modes 1, 2, and 3, the outputs of the numerical processors go to the mode-display selector switches. When the operator pushes the switch corresponding to the mode he wishes displayed, the corresponding numerical processor drives the binary-to-octal converter, and the SIF lamps indicating the target code are energized. Again, the corresponding confidence lamps are simultaneously illuminated.

The mode 1, 2, and 3 gates, when activated, send signals to their respective follow and hold position-correlation stores in order to make them ready. When the corresponding numerical processor obtains a minimum confidence level, the follow and hold stores (Fig. 4) sample the values of the PPI X and Y sweeps, and hold these coordinate values. This action provides the coordinates at which the minimum confidence was obtained and makes them available to the retrace insertion unit when the operator has called that mode up on the numerical display. The resulting position correlation marker presented by the RIU on the PPI identifies the location of the target whose SIF code and/or altitude is showing on the numerical display.

When the Multiple Target button's “no confidence” lamp is lit, or when otherwise desired, multiple target operation can be initiated by engaging this button. This converts the mode 1, 2, and 3 numerical processors to single mode operation corresponding to the mode select switch engaged. The NUDOR puts the multiple target returns into the mode one, two and three processors in received sequence repeating for five interrogations of the single mode, but using the same logic and display as in the multiple mode confidence determination. Mode 5 remains as a single target mode processor acting only on the first return for each interrogation. Instead of mode selection, the mode selector now switches control target selection representing the first, second, and third targets in the gate, allowing the operator to select each one for display.

VIDEO GATING

Video gating, with a constant angular width and a constant range depth, centered on the hook location, is obtained as shown in Fig. 4. In order to obtain constant angular width (which can be set at any desired value), the early azimuth gate point X_{H1}, Y_{H1} is determined by a $\Delta X = ky$ subtracted from X_H and a $\Delta Y = kx$ added to Y_H. This operation is performed by the input compare circuits as shown. The compare circuits null when $(X_H - \Delta X) - X_{SW} = 0$ and $(Y_H + \Delta Y) - Y_{SW} = 0$. This action causes the differential amplifier to balance, which, in turn, causes the respective Schmitt circuit to trigger. When both of these circuits operate in time coincidence, their outputs cause the AND circuit to produce an output which passes through the steering gate and sets the flip-flop. The flip-flop drives a delay circuit, whose output sets the steering gate so that subsequent comparisons coincident at the AND circuit will reset the flip-flop, and reverses the arithmetic operation on the ΔX and ΔY signals. The X_H compare circuit then operates when $(X_H + \Delta X) - X_{SW} = 0$ and the Y_H compare circuit operates when $(Y_H - \Delta Y) - Y_{SW} = 0$. This operation sets the compare circuits to determine the X_{H2}, Y_{H2} or video gate cut off point.

The setting of the flip-flop also enables the follow and hold circuit. Activating the follow and hold circuit causes the range of X_H, Y_H minus an increment δR to be derived from the range sweep. This range value is compared with each succeeding range sweep by the Schmitt circuit which triggers the multivibrator whose output provides the $2\Delta R$ range depth signal. This signal is gated by the flip-flop and provides the video gate control. When the PPI sweeps reach the X_{H2}, Y_{H2} coordinate (gate end), the pulse generated by the compare circuit passes through the steering gate and causes the flip-flop to be reset. This action restores the video gate generator to its original state. The gating

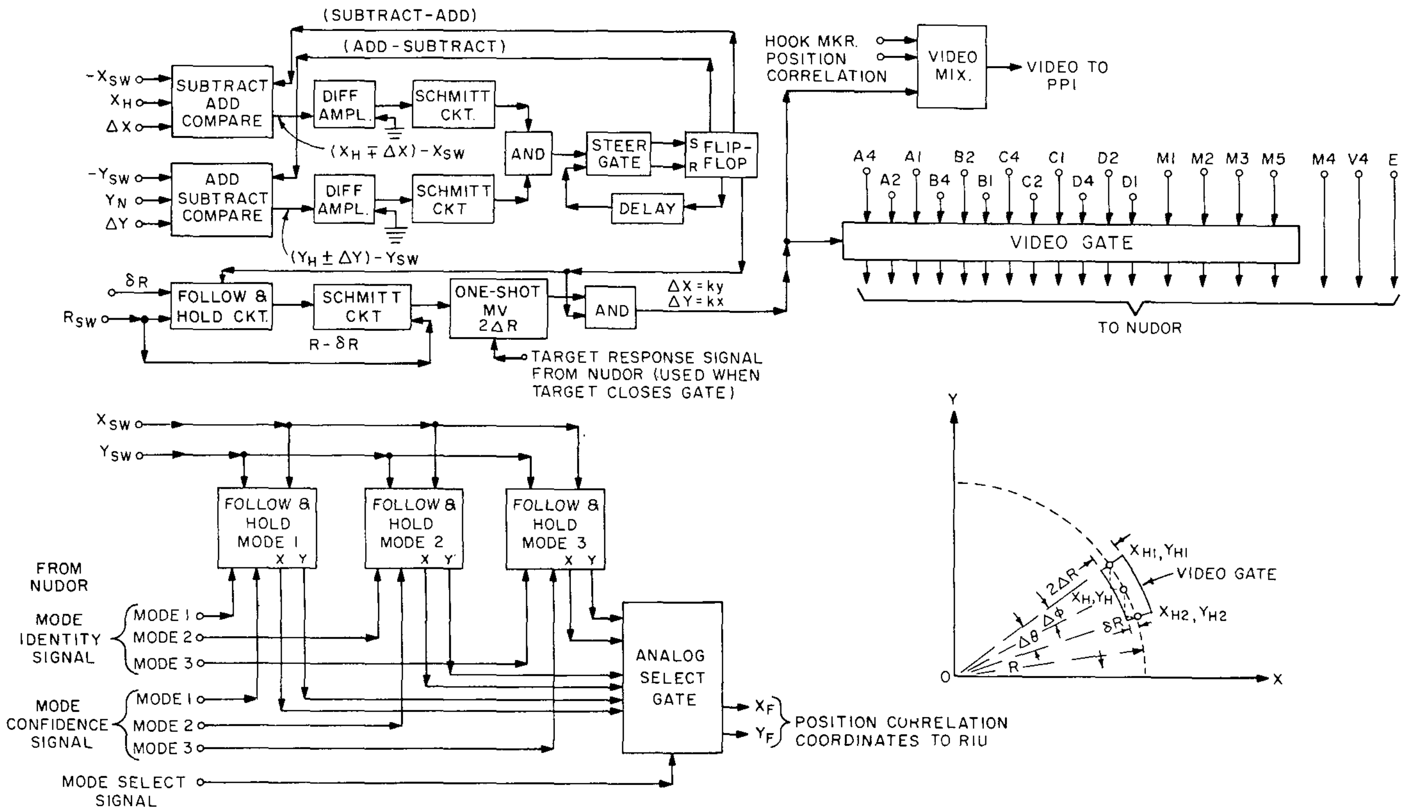


Fig. 4 - Video gate

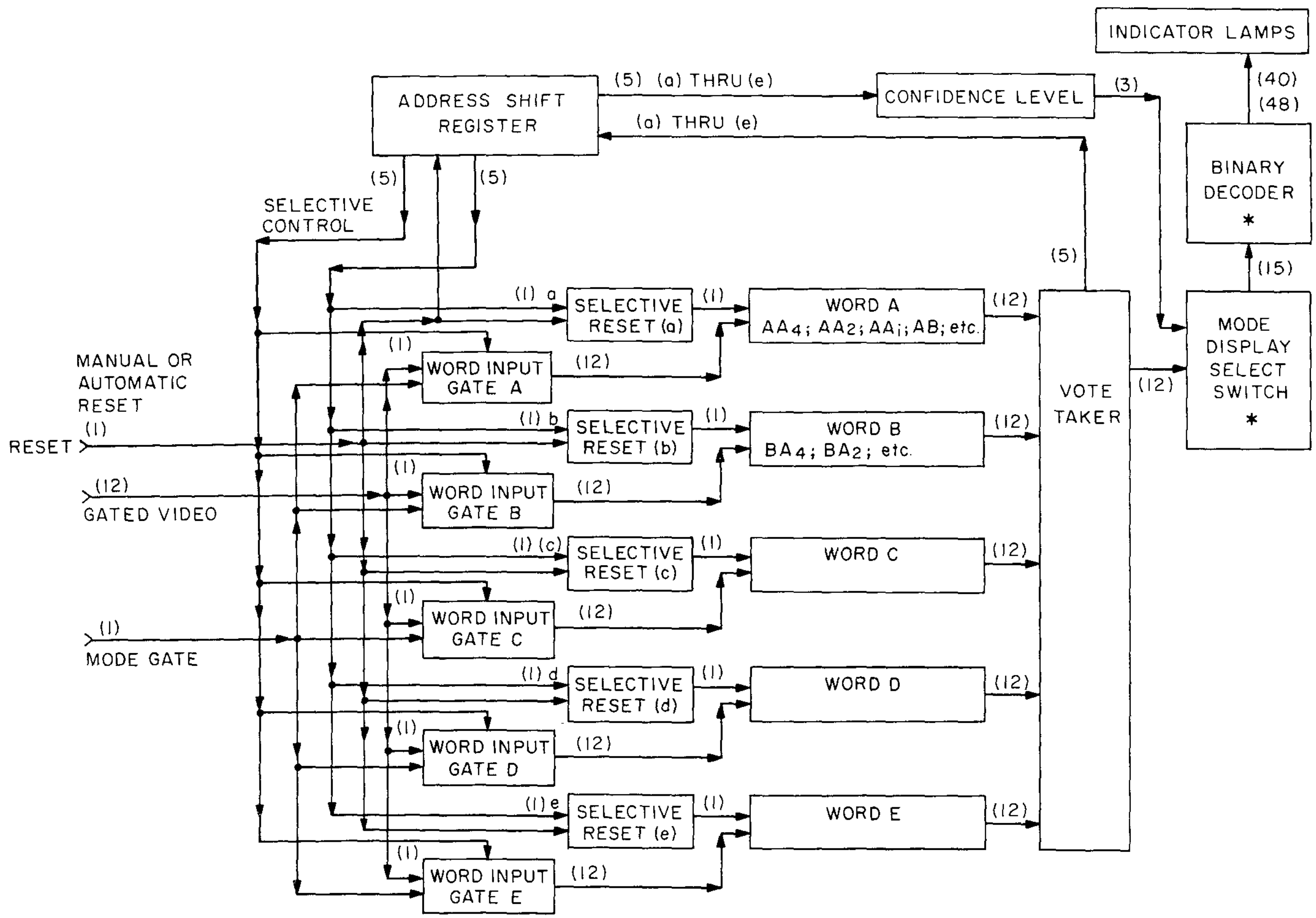
area is illustrated at the bottom right of Fig. 4. The depth of the range gate is controlled by changing the 2ΔR value. The distance the video gate opens ahead of the hook-gate range is controlled by δR, and the azimuth angle is controlled by the value k. Provisions are made for mixing the derivatives of the gating signals into the PPI video in order to provide a painted gate outline on the scope when desired. A target response signal from the NUDOR can be used to cut off the range gate after the receipt of the first decoded response appearing within the gate. This would virtually eliminate the processing of disagreeing responses in the NUDOR due to the presence of multiple targets within the gate. By this means, targets spaced as close as 4 microseconds in range can be resolved and properly identified. This technique is particularly suitable for "searchlighting" operation.

NUMERICAL PROCESSOR

The numerical processor for a single mode is shown in Fig. 5. The gated input video drives each word input gate. The presence of a mode interrogation from the mode gate is also applied to the word input gate. The third input to each word gate comes from the address shift register. The reset signal which clears the NUDOR can be generated manually by the operator during the hooking operation of a new target, or it can be generated by an automatic timer. When the mode gate signal is present, thereby indicating an interrogation, the address shift register releases the inhibiting signal on the word input gate A. Thus, when the IFF response appears from the video gate, it is stored in the word A position. When this storage is accomplished, the word input gate A is closed and the address shift register enables the word input gate B. When operating in the single target multiple mode manner, the next response in the numerical processor will occur when this same mode is again interrogated. The second video response in this mode will be stored in word B. This action will continue until the responses cease or until word E is filled. After the fifth return is stored, and if at least three out of five words agree, the vote taker acquires control of the address shift register and forces the shift register to the first disagreeing word position. Additional IFF responses are substituted into this word position until it comes into agreement with the majority or until the response cease. If the sixth response causes the first disagreeing word to come into agreement with the majority, the shift register is then forced to the second disagreeing word. This word position receives all additional responses until the responses cease or it comes into agreement. After the five words all agree, the shift register closes all the word input gates until the operator calls for a new set of data.

If after the first five responses are stored there is no three out of five confidence, the shift register recycles and causes the latest responses to be placed in the word positions containing the oldest information. That is, the sixth return would be placed in the word A position. This sequence will continue until a three of five agreement is obtained, at which time the vote taker takes control of the address shift register as before.

A minimum confidence level is possible after the shift register has advanced three steps and stored words A, B, and C agree. The numerical processor continues attempting to improve the confidence level as long as the target IFF decoder video is present. The target binary code meeting the minimum confidence level and the confidence level signal are then passed from the vote taker through the mode display select switch to the binary-to-octal converter. The converted signals are then used to energize the numerical readout lamps. In the case of mode 5, the vote taker outputs and the confidence level signals go directly to the binary-to-decimal converter and then to the proper numerical readout lamps.



FOR THREE LEVEL LOGIC WORDS D & E AND ASSOCIATED GATES NOT REQUIRED.
* MODE DISPLAY SWITCH FOR MODE 1, 2, & 3 ONLY.
BINARY TO OCTAL DECODER FOR MODES 1, 2, & 3.
BINARY TO DECIMAL DECODER FOR MODE 5.
( ) NUMBER OF LEADS

Fig. 5 - Numerical processor

ADDRESS SHIFT REGISTER

The address shift register is illustrated in Fig. 6 . The method illustrated was chosen so that several of the required gating functions which are common could be accomplished by a common circuit element. Each time a mode is interrogated, the mode pulse is present at the inputs to the flip-flops and their associated logic AND gates. In Fig. 6, after the reset signal occurs, all of the flip-flops are forced to the reset state. This causes all of the gates to be closed. On the first interrogation signal from the mode gate, FF-(a) is set. This causes the (a) output to go low and the ($\bar{a}$) output to go high (see diagram at lower right corner of Fig. 6). The output of gate N_a then goes low because (b) and ($\bar{a}$) are both high, thus allowing the word input gate A (see Fig. 7) to be opened. The second mode gate pulse sets FF-(b) through its associated input gate which was opened by the setting of FF-(a). The setting of FF-(b) causes N_b to go low and N_a to go high, thus causing the input word gate B to be opened. This action continues until the sixth mode gate pulse sets FF-(rc). All of the word input gates are then closed unless the signals from the vote takers (Fig. 8) indicate that one or more of the stored words are not in agreement with the others (less than five out of five confidence). The setting of FF-(rc) also provides an enable signal to the N_a-rc, N_b-rc, N_c-rc, N_d-rc and N_e-rc circuits. If any of the words (one or two) are in disagreement, the signals indicating disagreement from the vote taker are present on the corresponding leads (a) through (e). If for example (a) and (d) disagree, then N_a-rc provides a signal through the (a) OR circuit, opening the word input gate A. The N_a-rc circuit also inhibits all the following N gates as indicated in Fig. 6. If, after the seventh mode gate signal, word A agrees, the inhibiting signal on N_d-rc is released and the word input gate D is opened. Simultaneously, word input gate A is closed. If after the eighth mode gate signal word D agrees, all of the input word gates are closed. The numerical processor will hold these values until reset. The level of confidence does not need to be displayed until after the third mode gate period ends. Thus when FF-(d) is set, a signal from FF-(d) releases the inhibiting signal on the confidence level circuit (Fig. 8).

In case there is no three out of five agreement in the word stores after the first five inputs, a signal from the confidence level circuit resets just the address shift register. The sixth mode gate pulse will then allow the word-input gate A to be opened. Upon changing the content of word A and if a minimum confidence (three out of five) is obtained, a signal from the confidence level circuit will immediately set all of the flip-flops, and the address shift register will go through the process of steering the new IFF information to the disagreeing word stores as described previously. If the minimum confidence is not obtained after word A is changed, then the next mode gate will activate word B. This action will continue until the highest confidence level is obtained or until the IFF information input ceases.

WORD STORE

A single word store is shown in Fig. 7. The associated selective reset gate clears the storage flip-flops when the word is being readied for the receiving of new information. The word input gate includes the twelve NAND gates. By using a single AND circuit to combine the selected mode for display and address shift register signals, the word input gate can be changed to twelve dual input NAND gates. The decoded IFF video from the IFF decoder drives the twelve NAND gates in parallel. The outputs of the store flip-flops go to the vote taker circuit, one of which is illustrated in Fig. 9.

VOTE TAKER

One of twelve vote taker circuits for one mode store is shown in Fig. 9. The IFF-A_4 bit position for the words A through E is illustrated. When the address shift register

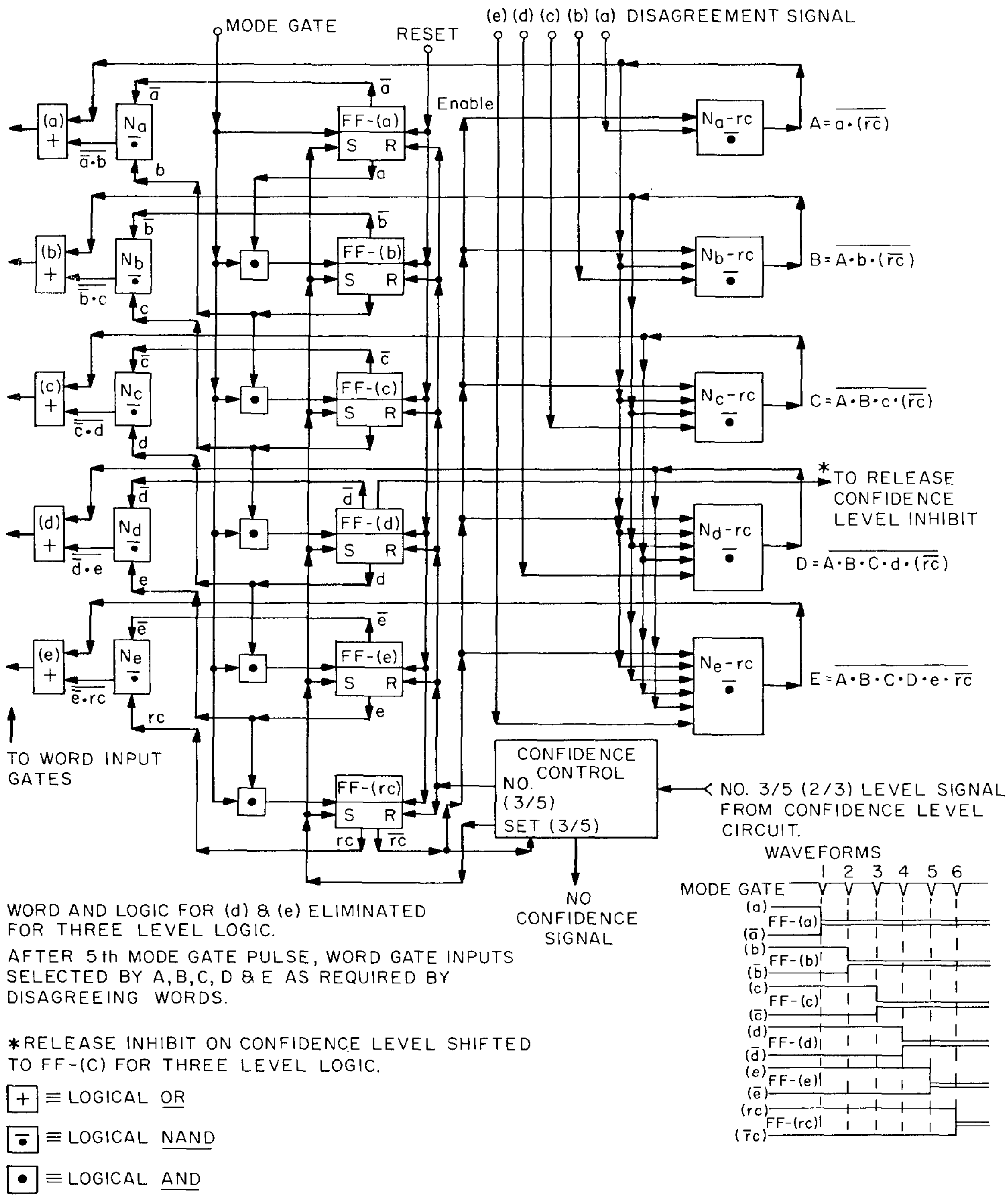
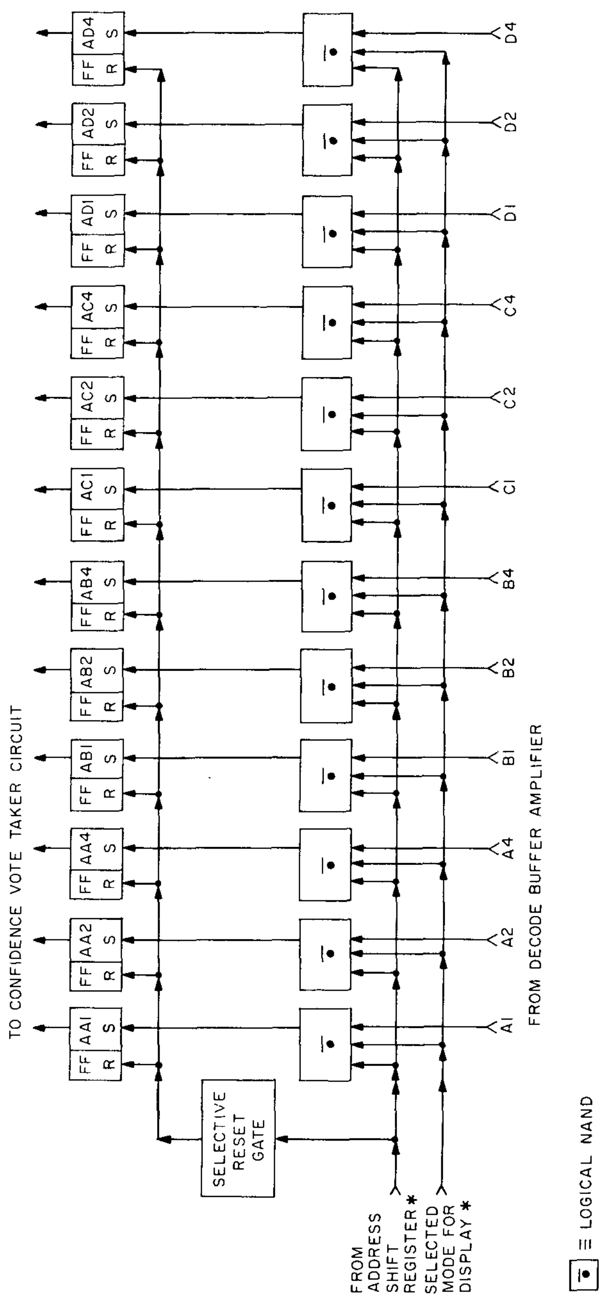


Fig. 6 - Address shift register



* NOTE: BY USING ONE AND CIRCUIT FOR THE ADDRESS REGISTER AND SELECTED MODE CIRCUIT INPUTS, THE NAND CIRCUITS CAN BE DUAL INPUT.
ONE WORD (WORDA) OF FIVE IN ONE MODE INDICATOR.
ONE WORD IN THREE FOR THREE LEVEL LOGIC.

Fig. 7 - Word store

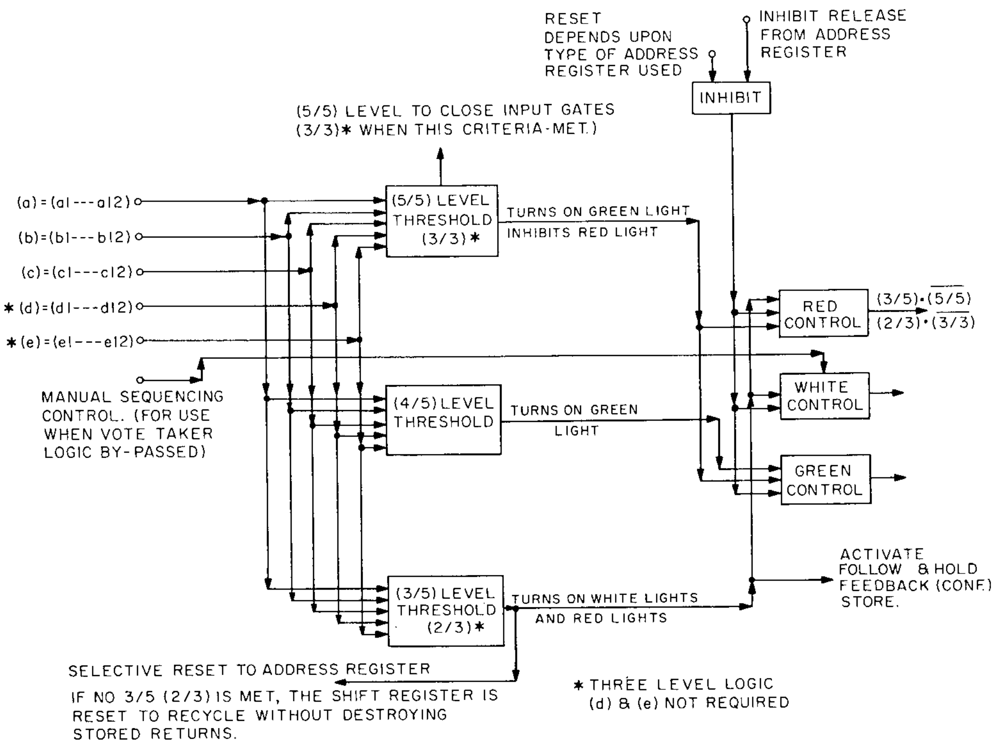


Fig. 8 - Confidence level

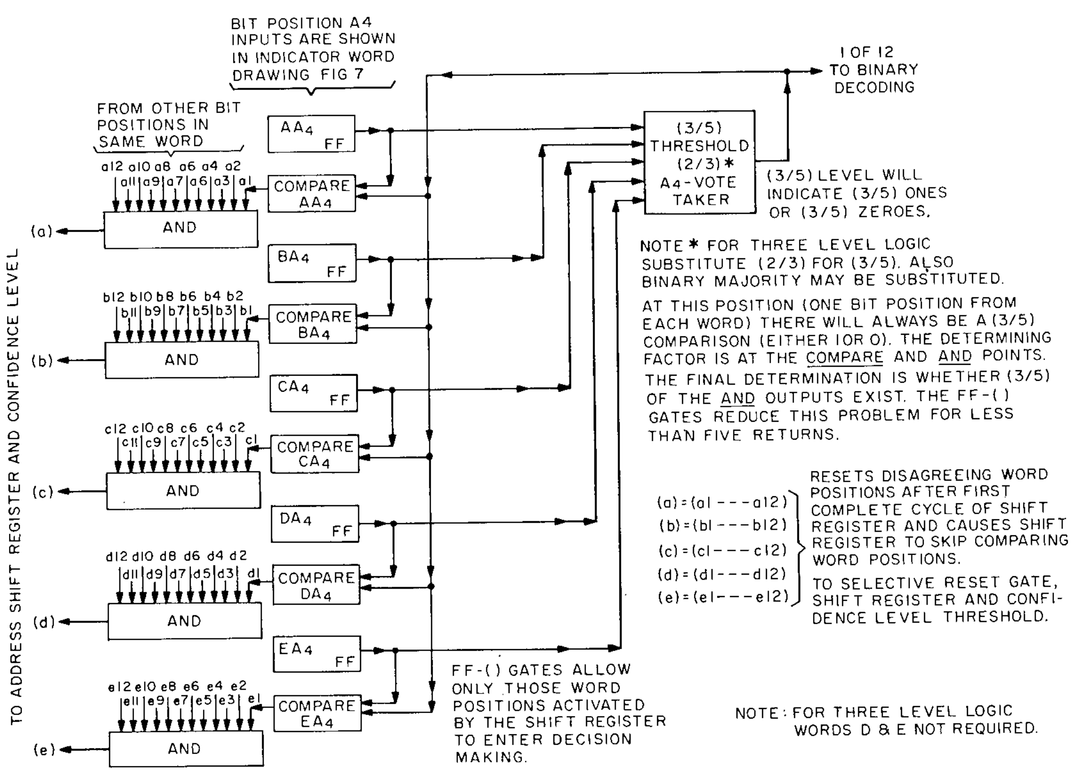


Fig. 9 - Vote taker

steps through the word positions, each bit position flip-flop output (AA_4, for example) is compared with the output of the threshold vote taker. If its output differs from the majority vote at that bit position, the output of the associated compare circuit (for example a_1) would be a logical zero. If the bit position is in agreement, the output is a logical one. In word A, for example, if each of the twelve a's is a logical one, then the output of the AND circuit would be a logical one. The outputs of the AND circuits go to the address shift register and the confidence level circuit. At each bit position a three out of five agreement will always exist, but for overall three out of five confidence this criterion must be met over all bit positions in at least three word positions. The outputs of the vote taker threshold go to the binary decoder in order to allow the correct numerical indicator to be selected when the minimum overall confidence level is obtained.

CONFIDENCE LEVEL

The confidence level control is performed by the logic shown in Figs. 8 and 10. After the third mode gate period at the address shift register, the inhibiting signal on the confidence level circuit is released. The (a) through (c) comparisons from the vote taker are then acted upon to derive the confidence level indication. If after three mode interrogations the first three vote taker outputs are logical ones, the three out of five level threshold turns on the white numeral light power and the red confidence lights. The three out of five level threshold also sends an activating signal to the follow and hold confidence feedback store. If during the next mode gate period vote taker (d) responds with a logical one, the four out of five threshold turns on the green lamps. This, in conjunction with the red lamp, causes a yellow confidence level to be indicated. If on the next interrogation period vote taker (e) responds with a logical one, then the five out of five level threshold inhibits the red lamp and the confidence indication becomes green. The confidence level circuit will not respond until at least three inputs are logical ones. If no minimum confidence is obtained after the first five responses, the three out of five level threshold sends a signal to the address shift register to recycle.

When the manual sequencing control is operating, the white light power is turned on so that the information stored in the word positions can be sequencially displayed. Additional details on the light control methods are shown in Fig. 10.

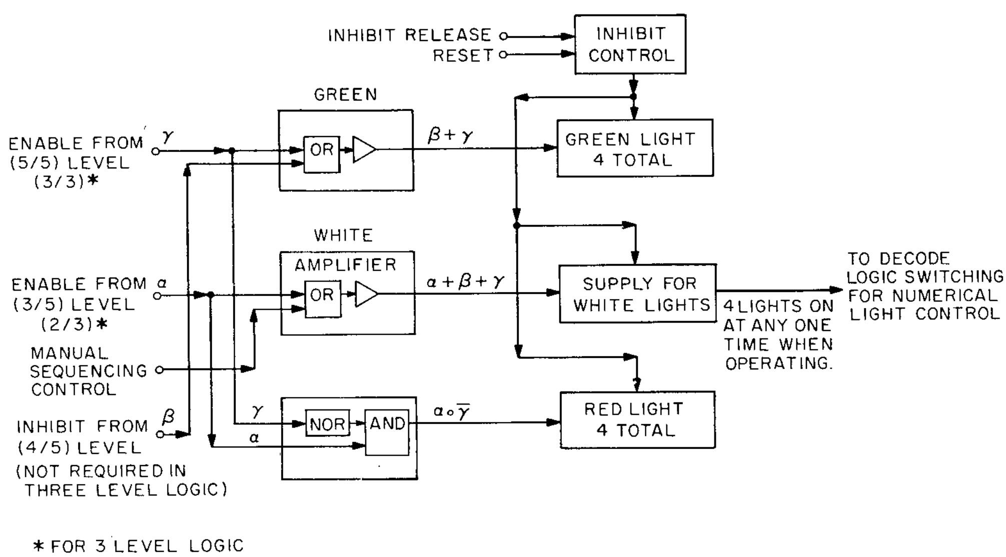


Fig. 10 - Light control

SUMMARY

An IFF active readout control and display system using majority logic and PPI position correlation techniques is being developed in the Data Processing Branch. The majority logic technique, in conjunction with the storing of up to five target responses in each IFF mode, indicates to the IFF operator the confidence level of the responses received. The position correlation techniques point out the location of the responding target on the PPI. A true range and azimuth video gate technique, which can work with analog or digital PPI sweeps, has been devised. This video gate works in conjunction with the retrace-insertion method employed with the PPI repeater.

Although the numerical display processor is described using five-level logic to determine confidence, the system can be easily shortened to a three-level logic without destroying the possibility of returning to the five-level logic. Threshold logic is used in the vote taker and in the confidence level in order to minimize the complexity of the decision-making circuits. Straight binary logic in these circuits becomes complex and awkward.

Retrace insertion techniques for controlling the hook gate do not interfere with the radar/IFF-PPI presentation.

One method for handling multiple targets in the hook gate is to allow the NUDOR to store each target in time sequence. The vote taker would by bypassed and the word stores would be manually sequenced out to the numerical readout.

In operation with single target multiple mode response, provisions are made for determining quality level (confidence) for the IFF responses in each mode. Mode five will be displayed whenever it is received. The first three modes will be stored when received and displayed on demand by the operator. A feedback correlation marker to the PPI display will indicate where the target responses reached the required minimum confidence level. This feedback marker will also indicate which target responses are stored in NUDOR when several targets are in proximity to each other.

The first NUDOR will be implemented for three-level logic in order to minimize cost, complexity and development time. If experience indicates that higher confidence levels are required, the NUDOR portion of the Active Readout System can be expanded to the five levels described in this report.

ACKNOWLEDGMENT

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DOCUMENT CONTROL DATA - R&D

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13. ABSTRACT

An IFF active readout control and display system using majority logic and PPI position correlation techniques is being developed in the Data Processing Branch. Up to five target responses in each interrogated mode are stored, and majority-voting logic determines the confidence of the stored returns in each mode. So long as a gated target's interrogation responses are present during one scan, the numerical processing continually attempts to increase the confidence of the stored returns. The position correlation techniques point out the location of the responding target on the PPI. A true range and azimuth video gate technique, which can work with analog or digital PPI sweeps, has been devised. This video gate technique works in conjunction with the PPI retrace insertion method employed.

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Security Classification

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
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Radar Range Computers						
Identification Systems						
Plan-Position Indicator						
Radar						
Azimuth Gating						
Range Gating						
Computer Logic						

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